

MC74LCX74

Low-Voltage CMOS Dual D-Type Flip-Flop

With 5 V-Tolerant Inputs

The MC74LCX74 is a high performance, dual D-type flip-flop with asynchronous clear and set inputs and complementary (O, $\bar{O}$) outputs. It operates from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX74 inputs to be safely driven from 5 V devices.

The MC74LCX74 consists of 2 edge-triggered flip-flops with individual D-type inputs. The flip-flop will store the state of individual D inputs, that meet the setup and hold time requirements, on the LOW-to-HIGH Clock (CP) transition.

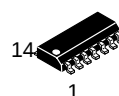
- Designed for 2.3 V to 3.6 V V_{CC} Operation
- 5 V Tolerant Inputs – Interface Capability With 5 V TTL Logic
- LVTTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V



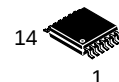
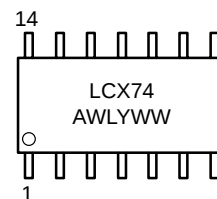
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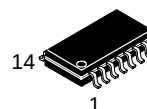
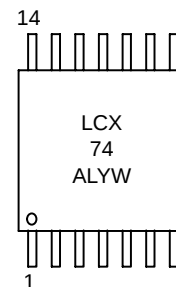
MARKING DIAGRAMS



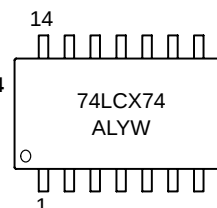
SO-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



EIAJ SO-14
M SUFFIX
CASE 965



A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74LCX74D	SO-14	55 Units/Rail
MC74LCX74DR2	SO-14	2500 Units/Reel
MC74LCX74DT	TSSOP-14	96 Untis/Rail
MC74LCX74DTR2	TSSOP-14	2500 Units/Reel
MC74LCX74M	EIAJ SO-14	50 Units/Rail
MC74LCX74MEL	EIAJ So-14	2000 Units/Reel

MC74LCX74

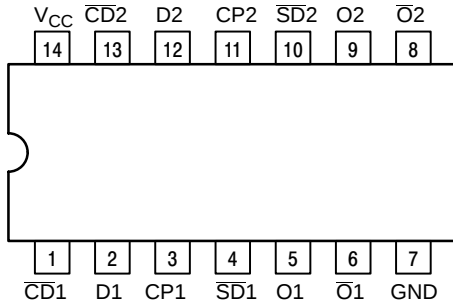


Figure 1. Pinout: 14-Lead (Top View)

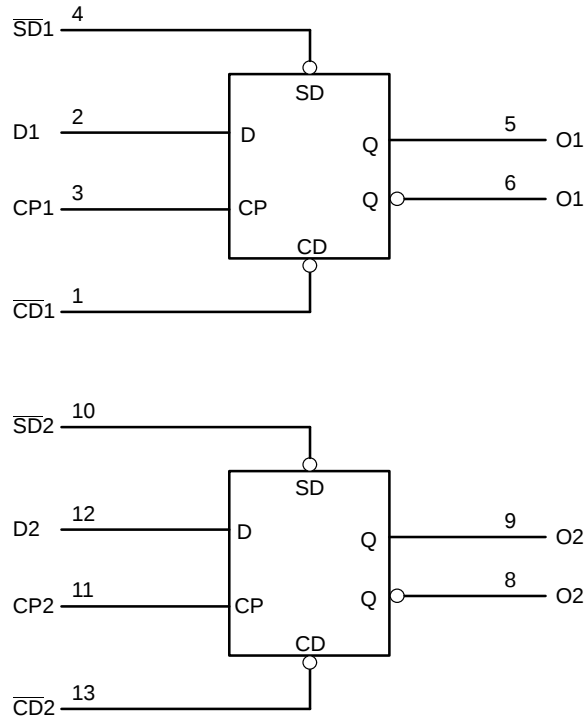


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
CP1, CP2	Clock Pulse Inputs
D1–D2	Data Inputs
$\overline{CD}1$, $\overline{CD}2$	Direct Clear Inputs
$\overline{SD}1$, $\overline{SD}2$	Direct Set Inputs
O _n – $\overline{O}n$	Outputs

TRUTH TABLE

Inputs				Outputs		Operating Mode
$\overline{SD}n$	$\overline{CD}n$	CPn	Dn	O _n	$\overline{O}n$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	↑	h	H	L	Load and Read Register
H	H	↑	l	L	H	
H	H	↯	X	NC	NC	Hold

H = High Voltage Level

h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition

L = Low Voltage Level

l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition

NC = No Change

X = High or Low Voltage Level and Transitions are Acceptable

↑ = Low-to-High Transition

↯ = Not a Low-to-High Transition

For I_{CC} reasons, DO NOT FLOAT Inputs

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MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 ≤ V_I ≤ +7.0		V
V_O	DC Output Voltage	−0.5 ≤ V_O ≤ $V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1.)	V
I_{IK}	DC Input Diode Current	−50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	−50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Type	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3–State)	0		V_{CC}	V
I_{OH}	HIGH Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ $V_{CC} = 2.3\text{ V} - 2.7\text{ V}$			−24 −12 −8	mA
I_{OL}	LOW Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ $V_{CC} = 2.3\text{ V} - 2.7\text{ V}$			+24 +12 +8	mA
T_A	Operating Free–Air Temperature	−40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, $V_{CC} = 3.0\text{ V}$	0		10	ns/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Unit
			Min	Max	
V _{IH}	HIGH Level Input Voltage (Note 2.)	2.3 V ≤ V _{CC} ≤ 2.7 V	1.7		V
		2.7 V ≤ V _{CC} ≤ 3.6 V	2.0		
V _{IL}	LOW Level Input Voltage (Note 2.)	2.3 V ≤ V _{CC} ≤ 2.7 V		0.7	V
		2.7 V ≤ V _{CC} ≤ 3.6 V		0.8	
V _{OH}	HIGH Level Output Voltage	2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OH} = -100 μA	V _{CC} - 0.2		V
		V _{CC} = 2.3 V; I _{OH} = -8 mA	1.8		
		V _{CC} = 2.7 V; I _{OH} = -12 mA	2.2		
		V _{CC} = 3.0 V; I _{OH} = -18 mA	2.4		
		V _{CC} = 3.0 V; I _{OH} = -24 mA	2.2		
V _{OL}	LOW Level Output Voltage	2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA		0.2	V
		V _{CC} = 2.3 V; I _{OL} = 8 mA		0.6	
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 16 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 24 mA		0.55	
I _I	Input Leakage Current	2.3 V ≤ V _{CC} ≤ 3.6 V; 0 V ≤ V _I ≤ 5.5 V		±5	μA
I _{CC}	Quiescent Supply Current	2.3 ≤ V _{CC} ≤ 3.6 V; V _I = GND or V _{CC}		10	μA
		2.3 ≤ V _{CC} ≤ 3.6 V; 3.6 ≤ V _I or V _O ≤ 5.5 V		±10	
ΔI _{CC}	Increase in I _{CC} per Input	2.3 ≤ V _{CC} ≤ 3.6 V; V _{IH} = V _{CC} - 0.6 V		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS t_R = t_F = 2.5 ns; R_L = 500 Ω

Symbol	Parameter	Waveform	Limits						Unit
			T _A = −40°C to +85°C						
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 2.5 V ± 0.2 V		
			C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
			Min	Max	Min	Max	Min	Max	
f _{max}	Clock Pulse Frequency	1	150		150		150		MHz
t _{PLH}	Propagation Delay	1	1.5	7.0	1.5	8.0	1.5	8.4	ns
t _{PHL}	CPn to On or $\overline{\text{On}}$		1.5	7.0	1.5	8.0	1.5	8.4	
t _{PLH}	Propagation Delay	2	1.5	7.0	1.5	8.0	1.5	8.4	ns
t _{PHL}	$\overline{\text{SDn}}$ or $\overline{\text{CDn}}$ to On or $\overline{\text{On}}$		1.5	7.0	1.5	8.0	1.5	8.4	
t _s	Setup Time, HIGH or LOW Dn to CPn	1	2.5		2.5		4.0		ns
t _h	Hold Time, HIGH or LOW Dn to CPn	1	1.5		1.5		2.0		ns
t _w	CPn Pulse Width, HIGH or LOW	4	3.3		3.3		4.0		ns
	$\overline{\text{SDn}}$ or $\overline{\text{CDn}}$ Pulse Width, LOW		3.3		3.6		4.0		ns
t _{rec}	Recovery Time $\overline{\text{SDn}}$ or $\overline{\text{CDn}}$ to CPn	3	2.5		3.0		4.5		ns
t _{OSHL}	Output-to-Output Skew			1.0					ns
t _{OSLH}	(Note 3.)			1.0					

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

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DYNAMIC SWITCHING CHARACTERISTICS

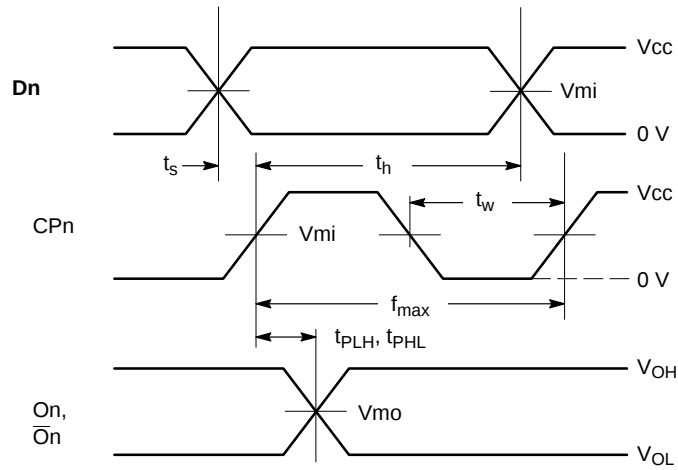
Symbol	Characteristic	Condition	T _A = +25°C			Unit
			Min	Typ	Max	
V _{OLP}	Dynamic LOW Peak Voltage (Note 4.)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V		0.8		V
		V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		0.6		V
V _{OLV}	Dynamic LOW Valley Voltage (Note 4.)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V		−0.8		V
		V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		−0.6		V

4. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

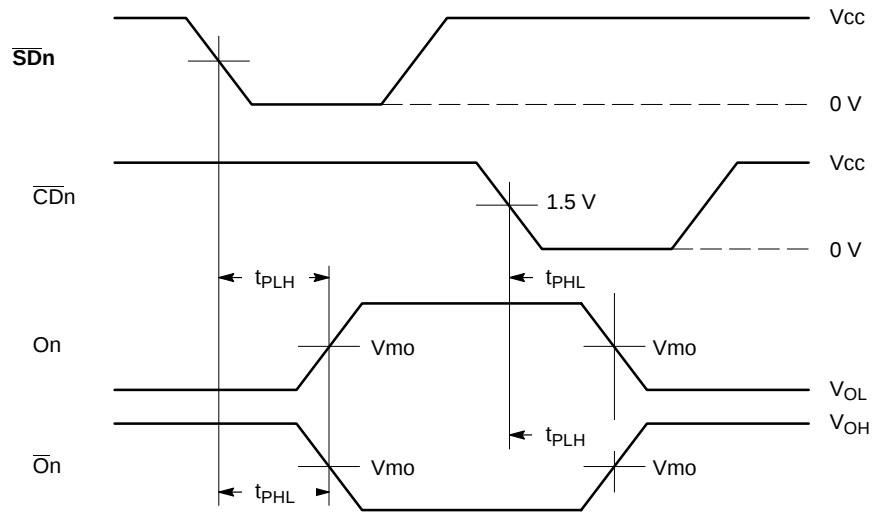
Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	25	pF

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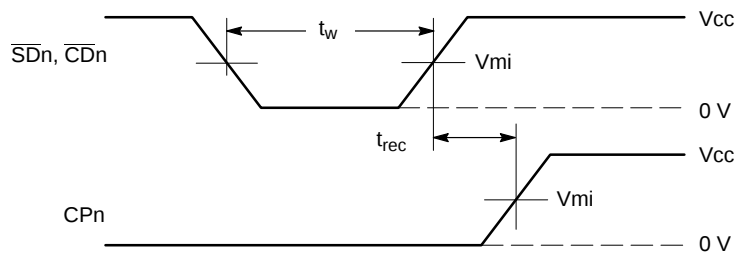
WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES

$t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$



WAVEFORM 2 – PROPAGATION DELAYS

$t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$

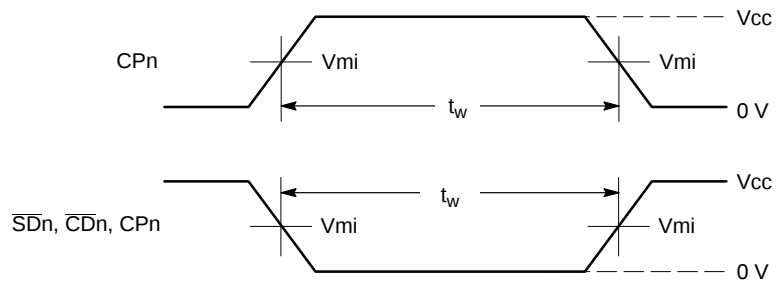


WAVEFORM 3 – RECOVERY TIME

$t_R = t_F = 2.5 \text{ ns}$ from 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$

Figure 3. AC Waveforms

MC74LCX74

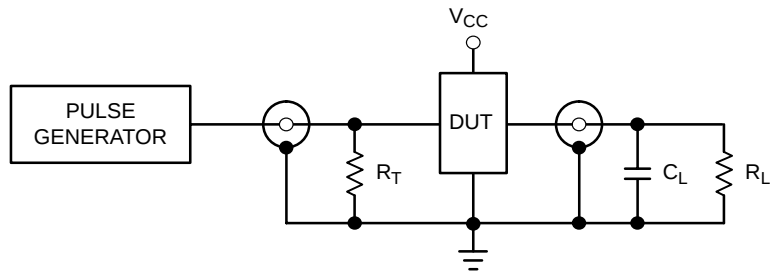


WAVEFORM 4 – PULSE WIDTH

$t_R = t_F = 2.5$ ns (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \leq 0.8$ V, $V_{OH} \geq 2.0$ V

Symbol	Vcc		
	3.3 V $\pm$ 0.3 V	2.7 V	2.5 V $\pm$ 0.2 V
Vmi	1.5 V	1.5 V	Vcc/2
Vmo	1.5 V	1.5 V	Vcc/2

Figure 3. AC Waveforms (Continued)



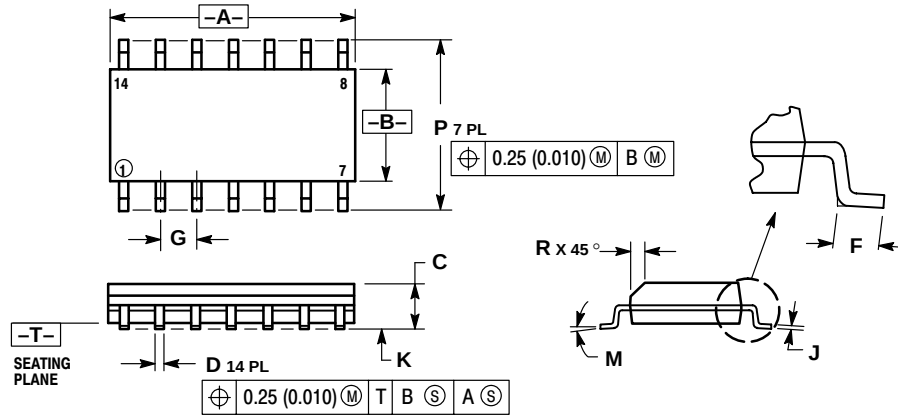
$C_L = 50$ pF at $V_{CC} = 3.3 \pm 0.3$ V or equivalent (includes jig and probe capacitance)
 $C_L = 30$ pF at $V_{CC} = 2.5 \pm 0.2$ V or equivalent (includes jig and probe capacitance)
 $R_L = R_1 = 500 \Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 4. Test Circuit

MC74LCX74

PACKAGE DIMENSIONS

SO-14 D SUFFIX CASE 751A-03 ISSUE F

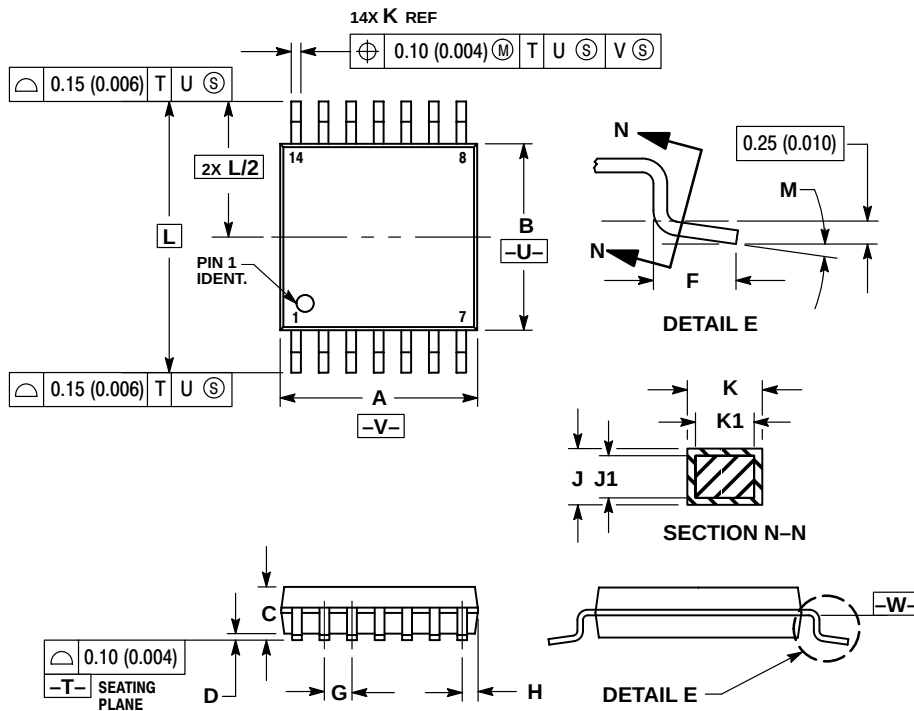


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP-14 DT SUFFIX CASE 948G-01 ISSUE O



NOTES:

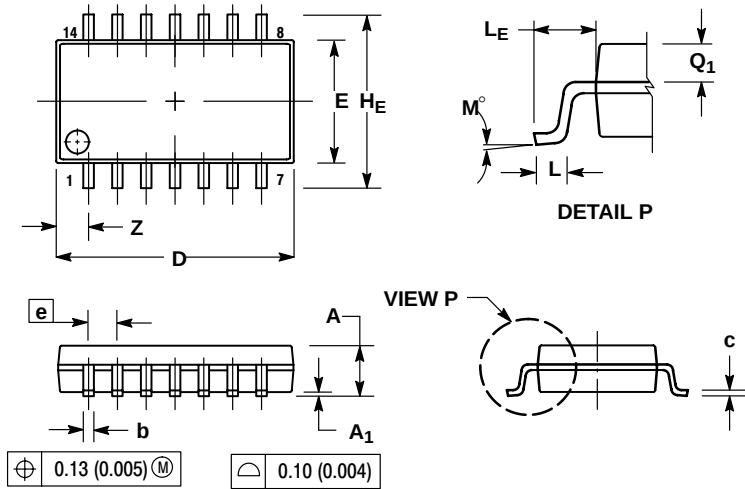
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74LCX74

PACKAGE DIMENSIONS

EIAJ SO-14
M SUFFIX
CASE 965-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

Notes

Notes

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