# Low-Voltage CMOS Quad 2-Input NOR Gate

## With 5V-Tolerant Inputs

The MC74LCX02 is a high performance, quad 2–input NOR gate operating from a 2.3 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_{\rm I}$  specification of 5.5V allows MC74LCX02 inputs to be safely driven from 5V devices.

Current drive capability is 24mA at the outputs.

- Designed for 2.3 to 3.6V V<sub>CC</sub> Operation
- 5V Tolerant Inputs Interface Capability With 5V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

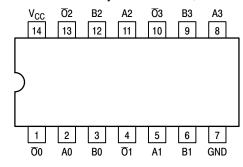


Figure 1. Pinout: 14-Lead (Top View)

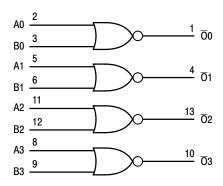
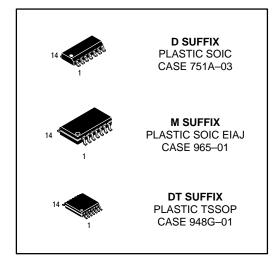


Figure 2. LOGIC DIAGRAM

## MC74LCX02



LOW-VOLTAGE CMOS QUAD 2-INPUT NOR GATE



#### **PIN NAMES**

Pins	Function
An, Bn	Data Inputs
On	Outputs

#### **FUNCTION TABLE**

INP	UTS	OUTPUTS
An	Bn	Ōn
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

#### **ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	$-0.5 \le V_1 \le +7.0$		V
Vo	DC Output Voltage	$-0.5 \le V_O \le V_{CC} + 0.5$	Note 1.	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	mA
Io	DC Output Source/Sink Current	±50		mA
Icc	DC Supply Current Per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150		°C

<sup>\*</sup> Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute—maximum—rated conditions is not implied.

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Тур	Max	Unit
V <sub>CC</sub>	Supply Voltage Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
VI	Input Voltage	0		5.5	V
Vo	Output Voltage (HIGH or LOW State)	0		V <sub>CC</sub>	V
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			-24	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			24	mA
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			-12	mA
l <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			12	mA
T <sub>A</sub>	Operating Free–Air Temperature	-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8V to 2.0V, $V_{CC} = 3.0V$	0		10	ns/V

#### DC ELECTRICAL CHARACTERISTICS

			T <sub>A</sub> = -40°C	to +85°C	
Symbol	Characteristic	Condition	Min	Max	Unit
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2.)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage (Note 2.)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V; I_{OH} = -100\mu A$	V <sub>CC</sub> – 0.2		V
		$V_{CC} = 2.7V; I_{OH} = -12mA$	2.2		
		$V_{CC} = 3.0V; I_{OH} = -18mA$	2.4		
		$V_{CC} = 3.0V; I_{OH} = -24mA$	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V; I_{OL} = 100\mu A$		0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 12mA		0.4	]
		$V_{CC} = 3.0V; I_{OL} = 16mA$		0.4	]
		$V_{CC} = 3.0V; I_{OL} = 24mA$		0.55	

<sup>2.</sup> These values of  $V_I$  are used to test DC electrical characteristics only.

<sup>1.</sup> Output in HIGH or LOW State. I<sub>O</sub> absolute maximum rating must be observed.

#### DC ELECTRICAL CHARACTERISTICS (continued)

			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		
Symbol	Characteristic	Condition	Min	Max	Unit
I <sub>I</sub>	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$ ; $0V \le V_I \le 5.5V$		±5.0	μΑ
Icc	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$ ; $V_I = GND$ or $V_{CC}$		10	μΑ
		$2.7 \le V_{CC} \le 3.6V; 3.6 \le V_I \le 5.5V$		±10	μΑ
Δl <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	$2.7 \le V_{CC} \le 3.6V; V_{IH} = V_{CC} - 0.6V$		500	μΑ

#### AC CHARACTERISTICS ( $t_R = t_F = 2.5 \text{ns}$ ; $C_L = 50 \text{pF}$ ; $R_L = 500 \Omega$ )

				Limits		
			TA	, = −40°C to +	-85°C	
			V <sub>CC</sub> = 3.0	V to 3.6V	V <sub>CC</sub> = 2.7V	
Symbol	Parameter	Waveform	Min	Max	Max	Unit
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Input to Output	1	1.5 1.5	5.2 5.2	6.0 6.0	ns
toshl toslh	Output-to-Output Skew (Note 3.)			1.0 1.0		ns

Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.
 The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

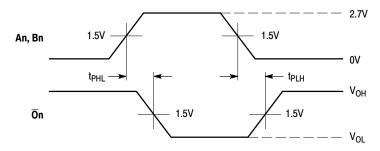
#### **DYNAMIC SWITCHING CHARACTERISTICS**

			T <sub>A</sub> = +25°C			
Symbol	Characteristic	Condition	Min	Тур	Max	Unit
V <sub>OLP</sub>	Dynamic LOW Peak Voltage (Note 4.)	$V_{CC} = 3.3V$ , $C_L = 50pF$ , $V_{IH} = 3.3V$ , $V_{IL} = 0V$		0.8		V
V <sub>OLV</sub>	Dynamic LOW Valley Voltage (Note 4.)	$V_{CC} = 3.3V$ , $C_L = 50pF$ , $V_{IH} = 3.3V$ , $V_{IL} = 0V$		0.8		V

<sup>4.</sup> Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

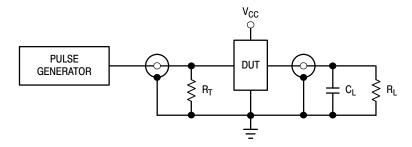
### **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	$V_{CC} = 3.3V$ , $V_{I} = 0V$ or $V_{CC}$	7	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC} = 3.3V$ , $V_I = 0V$ or $V_{CC}$	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$ , $V_I = 0V$ or $V_{CC}$	25	pF



 $\label{eq:propagation} \begin{array}{c} \textbf{PROPAGATION DELAYS} \\ t_R = t_F = 2.5 ns, \, 10\% \ to \ 90\%; \ f = 1 MHz; \, t_W = 500 ns \end{array}$ 

Figure 3. AC Waveforms



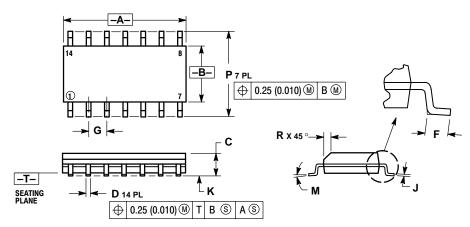
 $C_L=50 pF$  or equivalent (Includes jig and probe capacitance)  $R_L=R_1=500\Omega$  or equivalent  $R_T=Z_{OUT}$  of pulse generator (typically  $50\Omega)$ 

Figure 4. Test Circuit

#### **OUTLINE DIMENSIONS**

#### **D SUFFIX**

PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



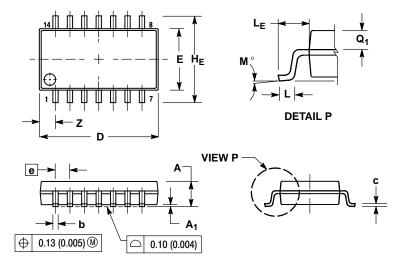
#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- F. EN SIDE.

  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS INCHES		HES	
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7°	0 °	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

#### **M SUFFIX** PLASTIC SOIC EIAJ PACKAGE CASE 965-01 ISSUE O



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 114.5M, 1962.

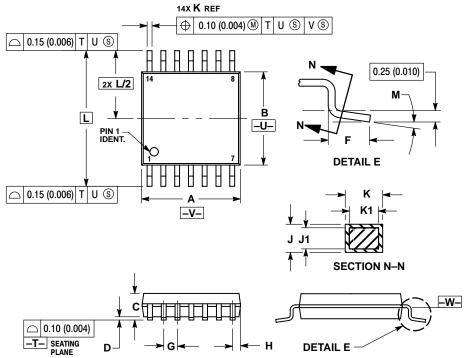
  C CONTROLLING DIMENSION: MILLIMETER.

  DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE
- 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003)
  TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	METERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α		2.05		0.081	
A <sub>1</sub>	0.05	0.20	0.002	0.008	
b	0.35	0.50	0.014	0.020	
С	0.18	0.27	0.007	0.011	
D	9.90	10.50	0.390	0.413	
E	5.10	5.45	0.201	0.215	
е	1.27	BSC	0.050	BSC	
HE	7.40	8.20	0.291	0.323	
0.50	0.50	0.85	0.020	0.033	
LE	1.10	1.50	0.043	0.059	
M	0 °	10°	0 °	10°	
$Q_1$	0.70	0.90	0.028	0.035	
Z		1.42		0.056	

#### **OUTLINE DIMENSIONS**

#### **DT SUFFIX** PLASTIC TSSOP PACKAGE CASE 948G-01 **ISSUE O**



#### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.

  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.03) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.

  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE —W-.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40	BSC	0.252 BSC		
М	0°	8°	0°	8°	

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