

MC10LVEP11, MC100LVEP11

2.5V / 3.3V ECL 1:2 Differential Fanout Buffer

The MC10/100LVEP11 is a differential 1:2 fanout buffer. The device is pin and functionally equivalent to the EP11 device. With AC performance the same as the EP11 device, the LVEP11 is ideal for applications requiring lower voltage. Single-ended CLK input operation is limited to a $V_{CC} \geq 3.0$ V in PECL mode, or $V_{EE} \leq -3.0$ V in NECL mode.

The 100 Series contains temperature compensation.

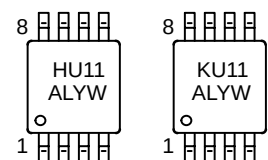
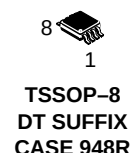
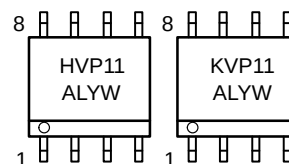
- 240 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: $V_{CC} = 2.375$ V to 3.8 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.8 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- LVDS Input Compatible



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MARKING DIAGRAMS*



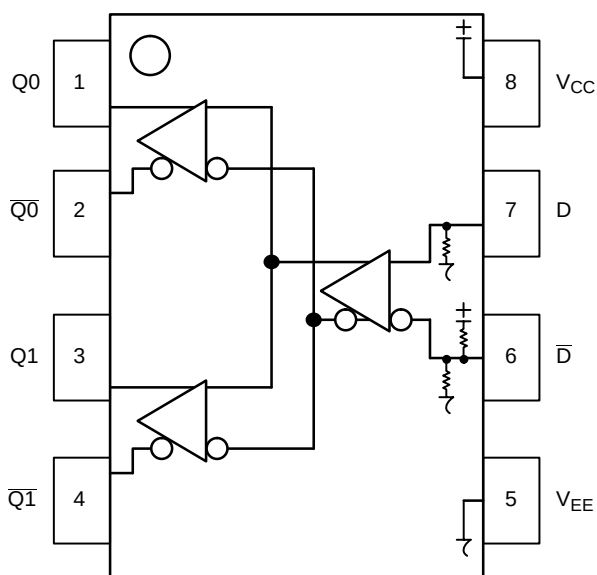
H = MC10 L = Wafer Lot
K = MC100 Y = Year
A = Assembly Location W = Work Week

*For additional information, see Application Note
AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10LVEP11D	SO-8	98 Units/Rail
MC10LVEP11DR2	SO-8	2500 Tape & Reel
MC100LVEP11D	SO-8	98 Units/Rail
MC100LVEP11DR2	SO-8	2500 Tape & Reel
MC10LVEP11DT	TSSOP-8	100 Units/Rail
MC10LVEP11DTR2	TSSOP-8	2500 Tape & Reel
MC100LVEP11DT	TSSOP-8	100 Units/Rail
MC100LVEP11DTR2	TSSOP-8	2500 Tape & Reel

MC10LVEP11, MC100LVEP11



PIN DESCRIPTION

PIN	FUNCTION
D*, $\bar{D}^{**}$	ECL Data Inputs
Q0, $\bar{Q}0$, Q1, $\bar{Q}1$	ECL Data Outputs
V _{CC}	Positive Supply
V _{EE}	Negative Supply

* Pins will default LOW when left open.

** Pins will default to V_{CC}/2 when left open.

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1.)	Level 1
Flammability Rating Oxygen Index	UL-94 code V-0 A 1/8" 28 to 34
Transistor Count	110 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		6	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-6	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 -6	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

MC10LVEP11, MC100LVEP11

10LVEP DC CHARACTERISTICS, PECL $V_{CC} = 2.5\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 3.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	24	30	36	24	30	36	25	31	38	mA
V_{OH}	Output HIGH Voltage (Note 4.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{OL}	Output LOW Voltage (Note 4.)	565	690	815	630	755	880	690	815	940	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 5.)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	$\frac{D}{D}$ 0.5 -150			0.5 -150			0.5 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.125 V to -1.3 V.

4. All loading with 50 ohms to V_{CC} -2.0 volts.

5. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0\text{ V}$ in PECL mode.

10LVEP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 6.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	24	30	36	24	30	36	25	31	38	mA
V_{OH}	Output HIGH Voltage (Note 7.)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 7.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single Ended) (Note 8.)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single Ended) (Note 8.)	1365		1690	1430		1755	1490		1815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 9.)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	$\frac{D}{D}$ 0.5 -150			0.5 -150			0.5 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925 V to -0.5 V.

7. All loading with 50 ohms to V_{CC} -2.0 volts.

8. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0\text{ V}$ in PECL mode.

9. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC10LVEP11, MC100LVEP11

10LVEP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.8\text{ V}$ to -2.375 V (Note 10.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	24	30	36	24	30	36	25	31	38	mA
V_{OH}	Output HIGH Voltage (Note 11.)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
V_{OL}	Output LOW Voltage (Note 11.)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
V_{IH}	Input HIGH Voltage (Single Ended) (Note 12.)	-1210		-885	-1145		-820	-1085		-760	mV
V_{IL}	Input LOW Voltage (Single Ended) (Note 12.)	-1935		-1610	-1870		-1545	-1810		-1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 13.)	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	D D	0.5 -150		0.5 -150			0.5 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

10. Input and output parameters vary 1:1 with V_{CC} .

11. All loading with 50 ohms to $V_{CC}-2.0$ volts.

12. Single ended input CLK pin operation is limited to $V_{EE} \leq -3.0\text{ V}$ in NECL mode.

13. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100LVEP DC CHARACTERISTICS, PECL $V_{CC} = 2.5\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 14.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	25	31	37	29	35	41	32	38	45	mA
V_{OH}	Output HIGH Voltage (Note 15.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 15.)	555	680	805	555	680	805	555	680	805	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 16.)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	D D	0.5 -150		0.5 -150			0.5 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

14. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.125 V to -1.3 V.

15. All loading with 50 ohms to $V_{CC}-2.0$ volts.

16. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0\text{ V}$ in PECL mode.

MC10LVEP11, MC100LVEP11

100LVEP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 17.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	25	31	37	29	35	41	32	38	45	mA
V_{OH}	Output HIGH Voltage (Note 18.)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 18.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single Ended) (Note 19.)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single Ended) (Note 19.)	1355		1675	1355		1675	1355		1675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 20.)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current $\frac{D}{\bar{D}}$	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

17. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925 V to -0.5 V.

18. All loading with 50 ohms to V_{CC} -2.0 volts.

19. Single ended input CLK pin operation is limited to $V_{CC} \geq 3.0\text{ V}$ in PECL mode.

20. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100LVEP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$; $V_{EE} = -3.8\text{ V}$ to -2.375 V (Note 21.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	25	31	37	29	35	41	32	38	45	mA
V_{OH}	Output HIGH Voltage (Note 22.)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 22.)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
V_{IH}	Input HIGH Voltage (Single Ended) (Note 23.)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single Ended) (Note 23.)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 24.)	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current $\frac{D}{\bar{D}}$	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

21. Input and output parameters vary 1:1 with V_{CC} .

22. All loading with 50 ohms to V_{CC} -2.0 volts.

23. Single ended input CLK pin operation is limited to $V_{EE} \leq -3.0\text{ V}$ in NECL mode.

24. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.8\text{ V}$ to -2.375 V or $V_{CC} = 2.375\text{ V}$ to 3.8 V; $V_{EE} = 0\text{ V}$ (Note 25.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Frequency (See Figure 2. $F_{\max}/\text{JITTER}$)		> 3			> 3			> 3		GHz
t_{PLH} , t_{PHL}	Propagation Delay (Differential) CLK to Q, $\bar{Q}$	170	230	300	180	240	310	210	270	360	ps
t_{SKEW}	Within Device Skew Q, $\bar{Q}$ Device to Device Skew (Note 26.)		5.0	20 130		5.0	20 130		5.0	20 150	ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 2. $F_{\max}/\text{JITTER}$)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
t_r , t_f	Output Rise/Fall Times Q, $\bar{Q}$ (20% - 80%)	70	110	170	80	120	180	100	140	200	ps

25. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to V_{CC} -2.0 V.

26. Skew is measured between outputs under identical transitions.

MC10LVEP11, MC100LVEP11

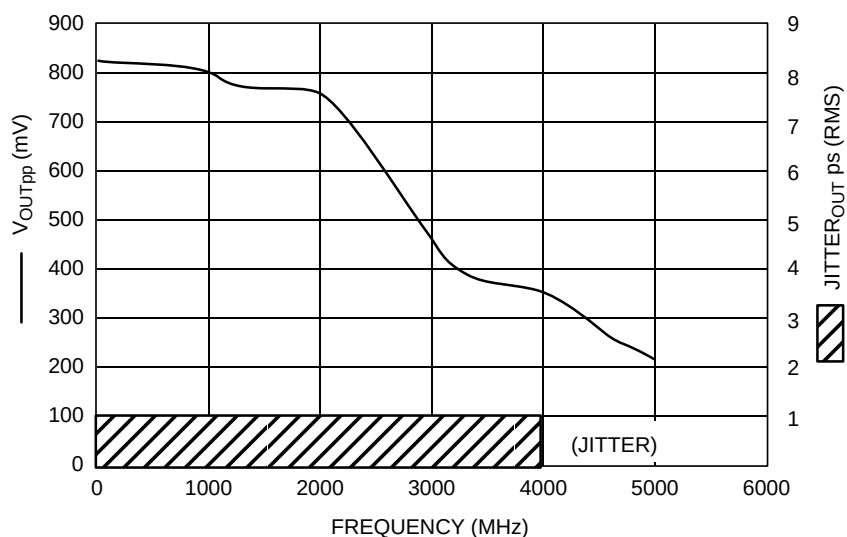


Figure 2. F_{max} /Jitter

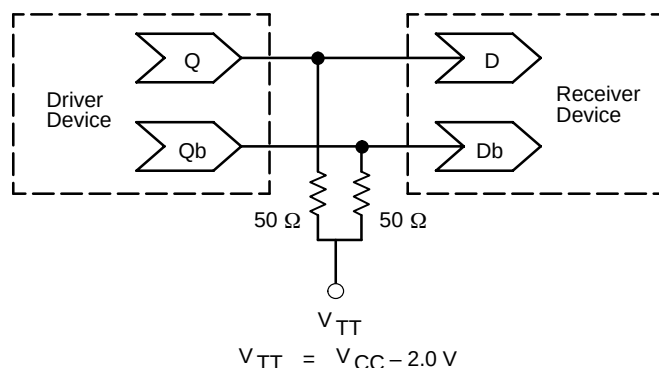


Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

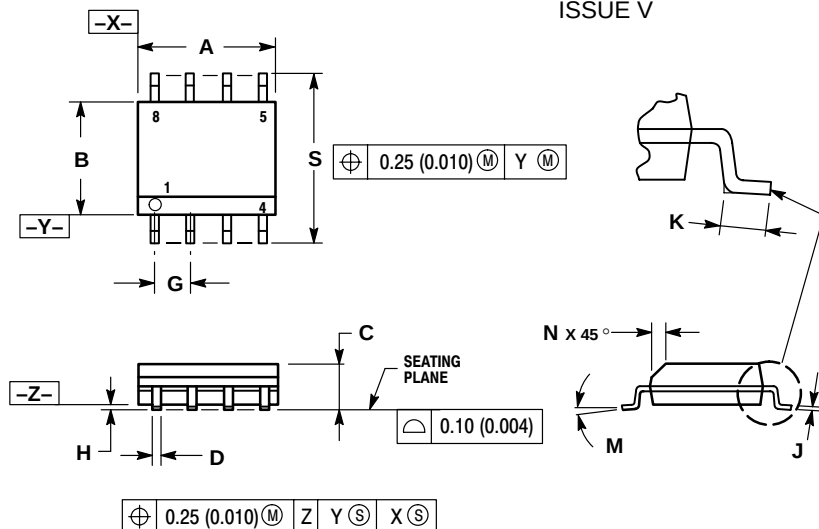
- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

MC10LVEP11, MC100LVEP11

PACKAGE DIMENSIONS

SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE V

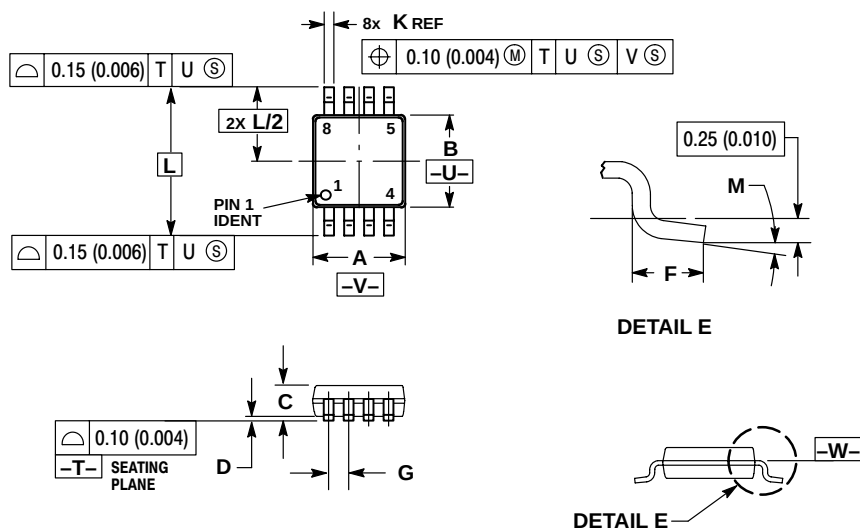


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

TSSOP-8 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948R-02 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

MC10LVEP11, MC100LVEP11

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