

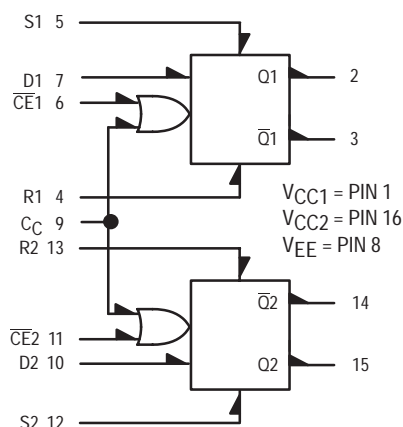
# MC10H131

## Dual D Type Master-Slave Flip-Flop

The MC10H131 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 235 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

### LOGIC DIAGRAM



### RS TRUTH TABLE

R	S	Q <sub>n+1</sub>
L	L	Q <sub>n</sub>
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

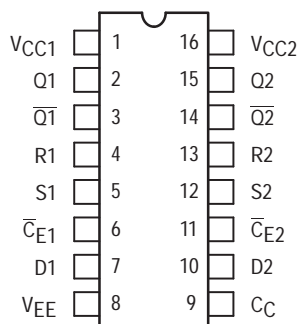
### CLOCKED TRUTH TABLE

C	D	Q <sub>n+1</sub>
L	X	Q <sub>n</sub>
H	L	L
H	H	H

$$C = \overline{CE} + C_C$$

A clock H is a clock transition from a low to a high state.

### DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.

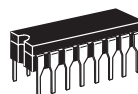
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



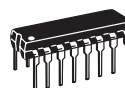
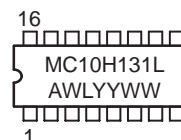
ON Semiconductor

<http://onsemi.com>

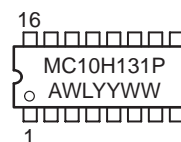
### MARKING DIAGRAMS



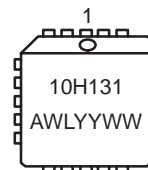
CDIP-16  
L SUFFIX  
CASE 620



PDIP-16  
P SUFFIX  
CASE 648



PLCC-20  
FN SUFFIX  
CASE 775



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC10H131L	CDIP-16	25 Units/Rail
MC10H131P	PDIP-16	25 Units/Rail
MC10H131FN	PLCC-20	46 Units/Rail

# MC10H131

## MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
$V_{EE}$	Power Supply ( $V_{CC} = 0$ )	-8.0 to 0	Vdc
$V_I$	Input Voltage ( $V_{CC} = 0$ )	0 to $V_{EE}$	Vdc
$I_{out}$	Output Current – Continuous – Surge	50 100	mA
$T_A$	Operating Temperature Range	0 to +75	°C
$T_{stg}$	Storage Temperature Range – Plastic – Ceramic	-55 to +150 -55 to +165	°C °C

## ELECTRICAL CHARACTERISTICS ( $V_{EE} = -5.2\text{ V} \pm 5\%$ ) (See Note 1.)

Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
$I_E$	Power Supply Current	–	62	–	56	–	62	mA
$I_{inH}$	Input Current High Pins 6, 11 Pin 9 Pins 7, 10 Pins 4, 5, 12, 13	– – – –	530 660 485 790	– – – –	310 390 285 465	– – – –	310 390 285 465	$\mu\text{A}$
$I_{inL}$	Input Current Low	0.5	–	0.5	–	0.3	–	$\mu\text{A}$
$V_{OH}$	High Output Voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
$V_{OL}$	Low Output Voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
$V_{IH}$	High Input Voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
$V_{IL}$	Low Input Voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

## AC PARAMETERS

$t_{pd}$	Propagation Delay Clock, $\overline{CE}$ Set, Reset	0.8 0.6	1.6 1.6	0.8 0.7	1.7 1.7	0.8 0.7	1.8 1.8	ns
$t_r$	Rise Time	0.6	2.0	0.6	2.0	0.6	2.2	ns
$t_f$	Fall Time	0.6	2.0	0.6	2.0	0.6	2.2	ns
$t_{set}$	Set-up Time	0.7	–	0.7	–	0.7	–	ns
$t_{hold}$	Hold Time	0.8	–	0.8	–	0.8	–	ns
$f_{tog}$	Toggle Frequency	250	–	250	–	250	–	MHz

- Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

## APPLICATION INFORMATION

The MC10H131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock ( $C_C$ ) and Clock Enable ( $\overline{CE}$ ) inputs. Each flip-flop may be clocked separately by holding the common clock in the new low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state.

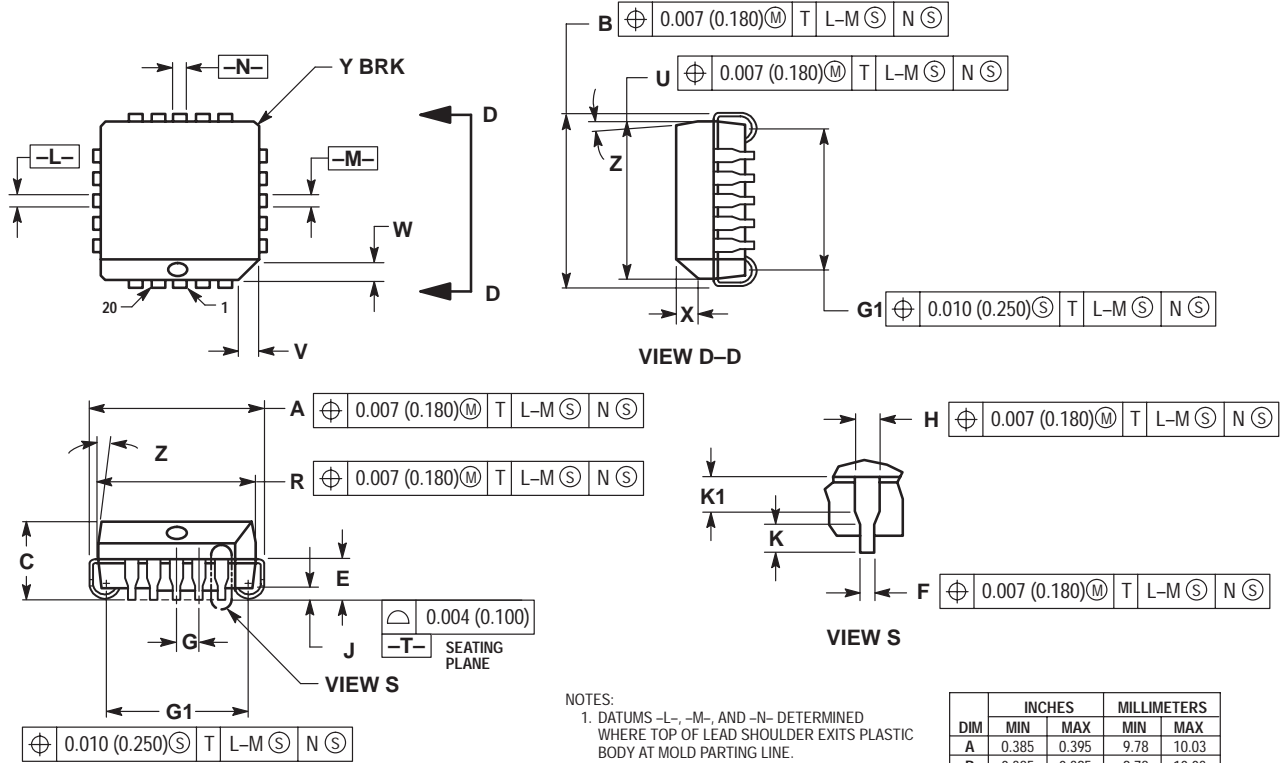
In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

# MC10H131

## PACKAGE DIMENSIONS

PLCC-20  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 775-02  
ISSUE C



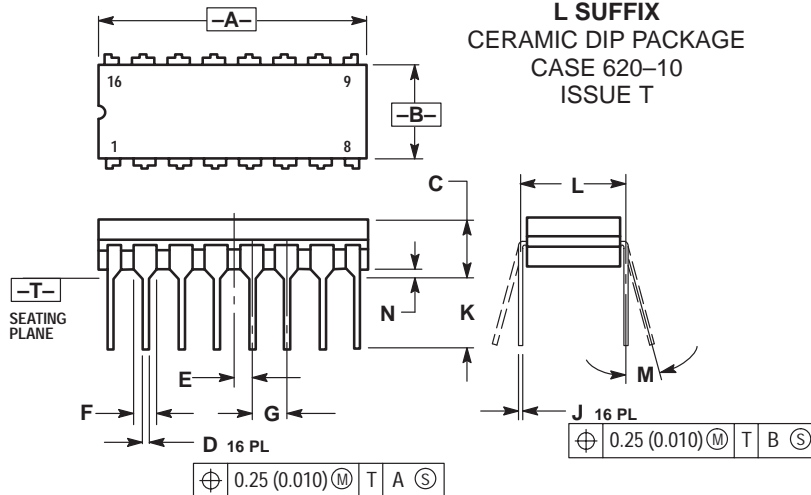
### NOTES:

1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

# MC10H131

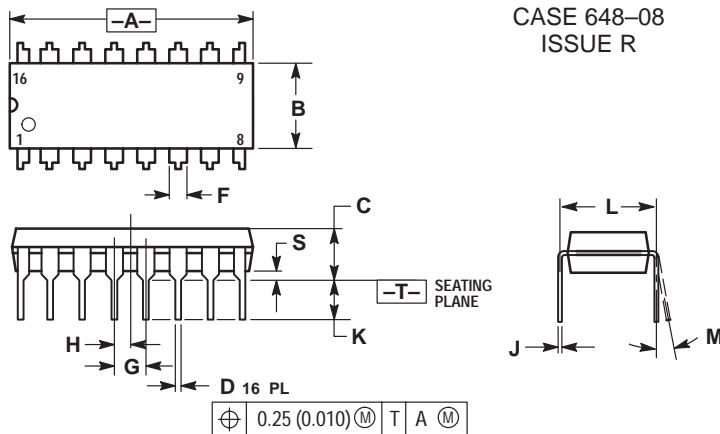
## CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

## PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### North America Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

### EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (M-F 2:30pm to 5:00pm Munich Time)  
Email: ONlit-german@hibbertco.com  
French Phone: (+1) 303-308-7141 (M-F 2:30pm to 5:00pm Toulouse Time)  
Email: ONlit-french@hibbertco.com  
English Phone: (+1) 303-308-7142 (M-F 1:30pm to 5:00pm UK Time)  
Email: ONlit@hibbertco.com

### ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
Toll Free from Hong Kong 800-4422-3781  
Email: ONlit-asia@hibbertco.com

### JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549  
Phone: 81-3-5740-2745  
Email: r14525@onsemi.com

Fax Response Line: 303-675-2167

800-344-3810 Toll Free USA/Canada

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.