MC10EP195, MC100EP195

3.3V ECL Programmable Delay Chip

The MC10/100EP195 is a programmable delay chip (PDC) designed primarily for clock deskewing and timing adjustment. It provides variable delay of a differential NECL/PECL input transition.

The delay section consists of a programmable matrix of gates and multiplexers as shown in the logic diagram, Figure 2. The delay increment of the EP195 has a digitally selectable resolution of about 10 ps and a net range of up to 10.2 ns. The required delay is selected by the 10 data select inputs D[0:9] values and controlled by the LEN (pin 10). A LOW level on LEN allows a transparent LOAD mode of real time delay values by D[0:9]. A LOW to HIGH transition on LEN will LOCK and HOLD current values present against any subsequent changes in D[0:9]. The approximate delay values for varying tap numbers correlating to D0 (LSB) through D9 (MSB) are shown in Table 5 and Figure 3.

Because the EP195 is designed using a chain of multiplexers it has a fixed minimum delay of 2.2 ns. An additional pin D10 is provided for cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs.

Select input pins D0−D10 may be threshold controlled by combinations of interconnects between V_{EF} (pin 7) and V_{CF} (pin 8) for LVCMOS, ECL, or LVTTL level signals. For LVCMOS input levels, leave V_{CF} and V_{EF} open. For ECL operation, short V_{CF} and V_{EF} (pins 7 and 8). For LVTTL level operation, connect a 1.5 V supply reference to V_{CF} and leave open V_{EF} pin. The 1.5 V reference voltage to V_{CF} pin can be accomplished by placing a 2.2 kΩ resistor between V_{CF} and V_{EE} for a 3.3 V power supply.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- Maximum Input Clock Frequency >1.2 GHz Typical
- Programmable Range: 0 ns to 10 ns
- Delay Range: 2.2 ns to 12.2 ns
- 10 ps Increments
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.6 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −3.0 V to −3.6 V
- Open Input Default State
- Safety Clamp on Inputs
- A Logic High on the $\overline{EN}$ Pin Will Force Q to Logic Low
- D[0:10] Can Accept Either ECL, LVCMOS, or LVTTL Inputs
- V_{BB} Output Reference Voltage

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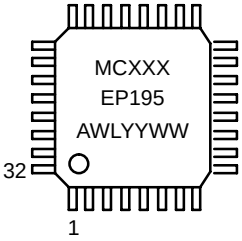
MARKING DIAGRAM*

LQFP−32
FA SUFFIX
CASE 873A



XXX = 10 OR 100
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP195FA	LQFP−32	250 Units/Tray
MC10EP195FAR2	LQFP−32	2000 Tape & Reel
MC100EP195FA	LQFP−32	250 Units/Tray
MC100EP195FAR2	LQFP−32	2000 Tape & Reel

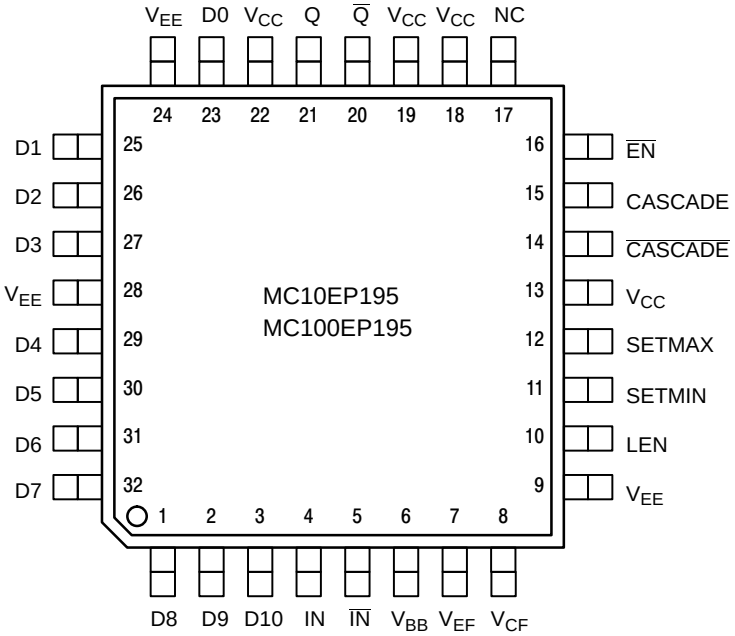


Figure 1. 32−Lead LQFP Pinout (Top View)

Table 1. Pin Description

Pin	Name	I/O	Default State	Description
23,25,26,27,29, 30,31,32,1,2,3	D[0:10]	LVCMOS, LVTTL, ECL Input	Low	Single Ended Parallel Data Inputs [0:10]. Internal 75 kΩ to V_{EE}. (Note 1)
4	IN	ECL Input	Low	Noninverted Differential Input. Internal 75 kΩ to V_{EE}.
5	$\overline{IN}$	ECL Input	High	Inverted Differential Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
6	V_{BB}	−	−	ECL Reference Voltage Output
7	V_{EF}	−	−	Reference Voltage for ECL Mode Connection
8	V_{CF}	−	−	LVCMOS, ECL, OR LVTTL Input Mode Select
9,28	V_{EE}	−	−	Negative Supply Voltage. All V_{EE} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. (Note 2)
13,18,19,22	V_{CC}	−	−	Positive Supply Voltage. All V_{CC} Pins must be externally Connected to Power Supply to Guarantee Proper Operation. (Note 2)
10	LEN	ECL Input	Low	Single−ended D pins LOAD / HOLD input. Internal 75 kΩ to V_{EE}.
11	SETMIN	ECL Input	Low	Single−ended Minimum Delay Set Logic Input. Internal 75 kΩ to V_{EE}. (Note 1)
12	SETMAX	ECL Input	Low	Single−ended Maximum Delay Set Logic Input. Internal 75 kΩ to V_{EE}. (Note 1)
14	$\overline{CASCADE}$	ECL Output	−	Inverted Differential Cascade Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V.
15	CASCADE	ECL Output	−	Noninverted Differential Cascade Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V.
16	$\overline{EN}$	ECL Input	Low	Single−ended Output Enable Pin. Internal 75 kΩ to V_{EE}.
17	NC	−	−	No Connect. The NC Pin is Electrically Connected to the Die and ”MUST BE” Left Open
21	Q	ECL Output	−	Noninverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V.
20	$\overline{Q}$	ECL Output	−	Inverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V.

1. SETMIN will override SETMAX if both are high. SETMAX and SETMIN will override all D[0:10] inputs.
2. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Table 2. Control Pin

EN	LOW (Note 3)	Input Signal is Propagated to the Output
	HIGH	Output Holds Logic Low State
LEN	LOW (Note 3)	Transparent or LOAD mode for real time delay values present on D[0:10].
	HIGH	LOCK and HOLD mode for delay values on D[0:10]; further changes on D[0:10] are not recognized and do not affect delay.
SETMIN	LOW (Note 3)	Output Delay set by D[0:10]
	HIGH	Set Minimum Output Delay
SETMAX	LOW (Note 3)	Output Delay set by D[0:10]
	HIGH	Set Maximum Output Delay

3. Internal pull−down resistor will provide a logic LOW if pin is left unconnected.

Table 3. Control D[0:10] Interface

V_{CF}	V_{EF} Pin (Note 4)	ECL Mode
V_{CF}	No Connect	LVCMOS Mode
V_{CF}	1.5 V ± 100 mV	LVTTL Mode (Note 5)

4. Short VCF (pin 8) and VEF (pin 7).
5. When Operating in LVTTL Mode, the reference voltage can be provided by connecting an external resistor, R_{CF} (suggested resistor value is 2.2 kΩ ±5%), between V_{CF} and V_{EE} pins.

Table 4. DATA INPUT OPERATING VOLTAGE TABLE

	CONTROL DATA SELECT INPUTS PINS (D [0:10])			
POWER SUPPLY	**LVCMOS**	**LVTTL**	**PECL**	**NECL**
Positive Mode ($V_{CC} - V_{EE} > 0$)	✓	✓	✓	N/A
Negative Mode ($V_{CC} - V_{EE} < 0$)	N/A	N/A	N/A	✓

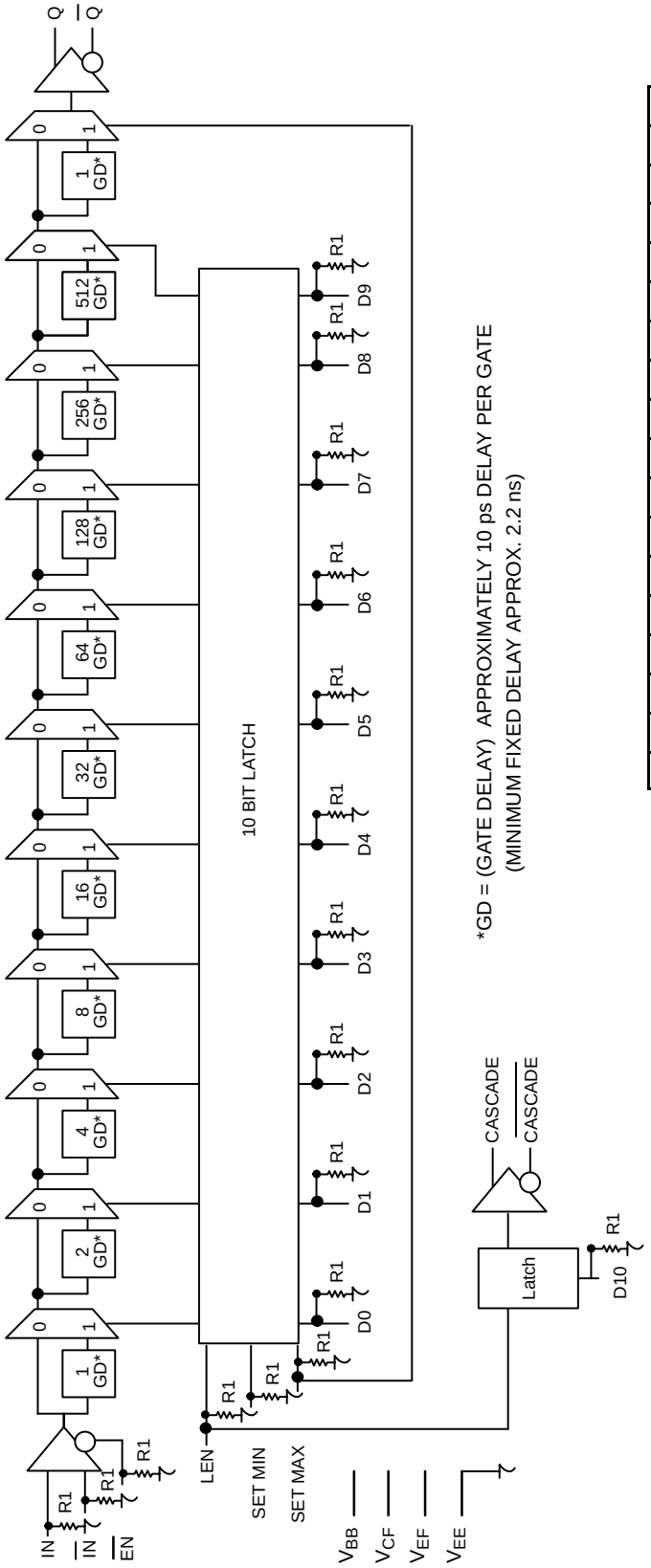


Figure 2. Logic Diagram

Table 5. THEORETICAL DELAY VALUES

D10	D(9:0) Value	Delay Value	Comment
	0000000000	0 ps	(SET MIN)
	0000000001	10 ps	
	0000000010	20 ps	
	0000000011	30 ps	
	0000000100	40 ps	
	0000000101	50 ps	
	0000000110	60 ps	
	0000000111	70 ps	
	0000001000	80 ps	
	0000010000	160 ps	
	0000100000	320 ps	
	0001000000	640 ps	
	0010000000	1280 ps	
	0100000000	2560 ps	
	1000000000	5120 ps	
	1111111111	10230 ps	
1	XXXXXXXXXX	10240 ps	(SET MAX)

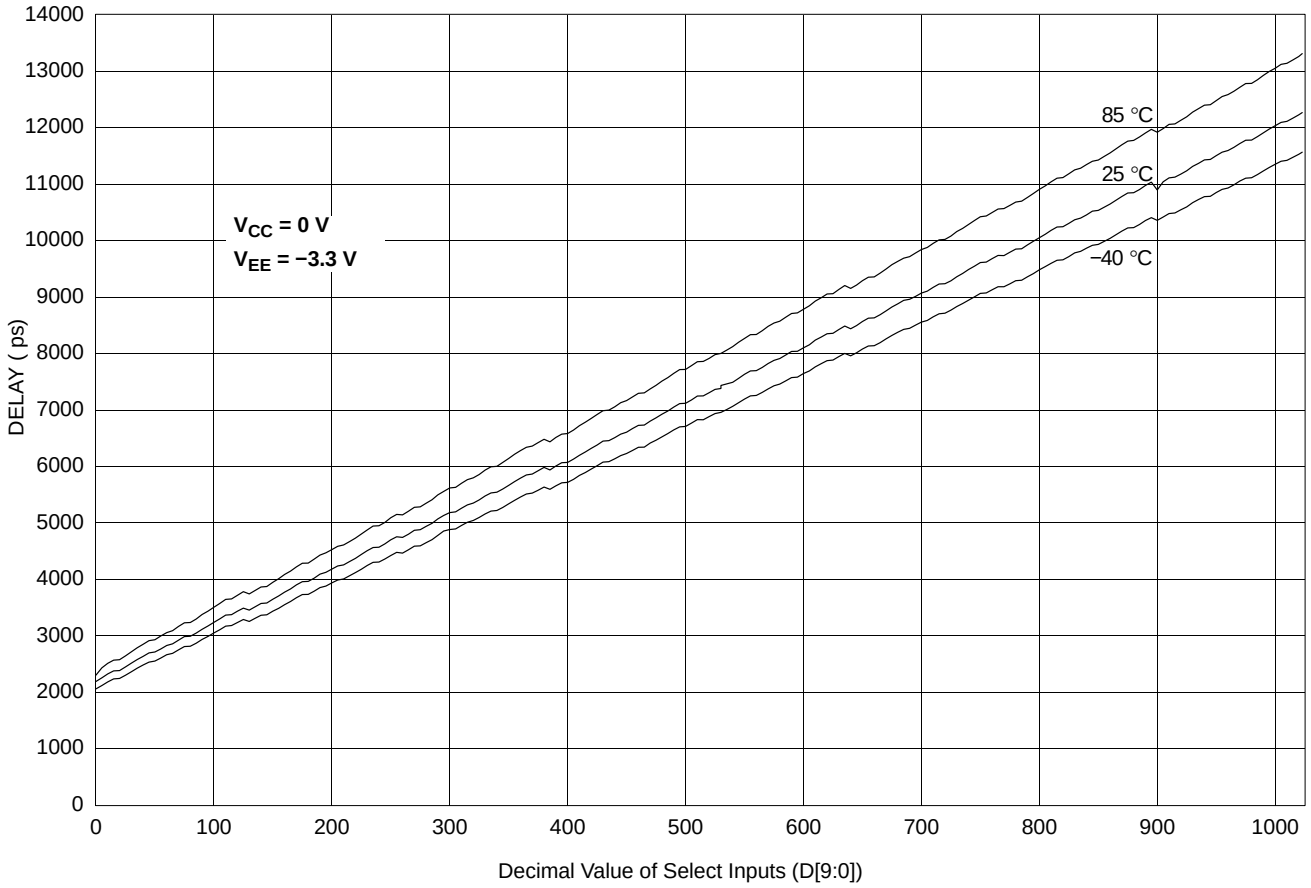


Figure 3. Measured Delay vs. Select Inputs

Table 6. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor	(R1)	75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV
Moisture Sensitivity (Note 6)		Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		1217 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

6. For additional information, see Application Note AND8003/D.

Table 7. MAXIMUM RATINGS (Note 7)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	Negative Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	Positive Mode Input Voltage Negative Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 LFPM 500 LFPM	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	std bd	32 LQFP	12 to 17	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

7. Maximum Ratings are those values beyond which device damage may occur.

Table 8. 10EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 8)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Negative Power Supply Current	110	145	175	120	150	180	120	150	180	mA
V_{OH}	Output HIGH Voltage (Note 9)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 9)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single−Ended) PECL LVCMOS LVTTL	 2090 2000 2000		 2415 3300 3300	 2155 2000 2000		 2480 3300 3300	 2215 2000 2000		 2540 3300 3300	mV
V_{IL}	Input LOW Voltage (Single−Ended) PECL LVCMOS LVTTL	 1365 0 0		 1690 800 800	 1430 0 0		 1755 800 800	 1490 0 0		 1815 800 800	mV
V_{BB}	ECL Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{CF}	LVTTL Mode Input Detect Voltage	1.4	1.5	1.6	1.4	1.5	1.6	1.4	1.5	1.6	V
V_{EF}	Reference Voltage for ECL Mode Connection	1915	2020	2120	1940	2080	2190	1985	2130	2265	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current (@ V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@ V_{IL}) IN $\overline{IN}$	0.5 −150			0.5 −150			0.5 −150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

8. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −0.3 V.
9. All loading with 50 Ω to V_{CC}−2.0 V.
10. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 9. 10EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = −3.3 V to −3.0 V (Note 11)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	110	145	175	120	150	180	120	150	180	mA
V_{OH}	Output HIGH Voltage (Note 12)	−1135	−1010	−885	−1070	−945	−820	−1010	−885	−760	mV
V_{OL}	Output LOW Voltage (Note 12)	−1935	−1810	−1685	−1870	−1745	−1620	−1810	−1685	−1560	mV
V_{IH}	Input HIGH Voltage (Single−Ended) NECL	−1210		−885	−1145		−820	−1085		−760	mV
V_{IL}	Input LOW Voltage (Single−Ended) NECL	−1935		−1610	−1870		−1545	−1810		−1485	mV
V_{BB}	ECL Output Voltage Reference	−1510	−1410	−1310	−1445	−1345	−1245	−1385	−1285	−1185	mV
V_{EF}	Reference Voltage for ECL Mode Connection	−1385	−1280	−1180	−1360	−1220	−1110	−1315	−1170	−1035	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current (@ V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@ V_{IL}) IN	0.5			0.5			0.5			μA
	$\overline{IN}$	−150			−150			−150			

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

11. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −0.3 V.
12. All loading with 50 Ω to V_{CC} − 2.0 V.
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 10. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 14)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	100	135	160	110	140	170	110	145	175	mA
V_{OH}	Output HIGH Voltage (Note 15)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 15)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single−Ended) PECL CMOS TTL	 2075 2000 2000		 2420 3300 3300	 2075 2000 2000		 2420 3300 3300	 2075 2000 2000		 2420 3300 3300	mV
V_{IL}	Input LOW Voltage (Single−Ended) PECL CMOS TTL	 1355 0 0		 1675 800 800	 1490 0 0		 1675 800 800	 1490 0 0		 1675 800 800	mV
V_{BB}	ECL Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{CF}	LVTTL Mode Input Detect Voltage	1.4	1.5	1.6	1.4	1.5	1.6	1.4	1.5	1.6	V
V_{EF}	Reference Voltage for ECL Mode Connection	1915	2020	2120	1940	2080	2190	1985	2130	2265	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 16)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current (@ V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@ V_{IL}) IN $\overline{IN}$	 0.5 −150			 0.5 −150			 0.5 −150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

14. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −0.3 V.
15. All loading with 50 Ω to V_{CC}−2.0 V.
16. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 11. 100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = −3.3 V (Note 17)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current (Note 18)	100	135	160	110	140	170	110	145	175	mA
V_{OH}	Output HIGH Voltage (Note 19)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 19)	−1945	−1820	−1695	−1945	−1820	−1695	−1945	−1820	−1695	mV
V_{IH}	Input HIGH Voltage (Single−Ended) NECL	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended) NECL	−1945		−1625	−1945		−1625	−1945		−1625	mV
V_{BB}	ECL Output Voltage Reference	−1525	−1425	−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
V_{EF}	Reference Voltage for ECL Mode Connection	−1385	−1280	−1180	−1360	−1220	−1110	−1315	−1170	−1035	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 20)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current (@ V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@ V_{IL}) IN $\overline{IN}$	0.5 −150			0.5 −150			0.5 −150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

17. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −0.3 V.
18. Required 500 lfpm air flow when using +5 V power supply. For (V_{CC} − V_{EE}) > 3.3 V, 5 Ω to 10 Ω in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend V_{CC}−V_{EE} operation at ≤ 3.8 V.
19. All loading with 50 Ω to V_{CC}−2.0 V.
20. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 12. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.0 V to −3.6 V or V_{CC} = 3.0 V to 3.6 V; V_{EE} = 0 V (Note 21)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency		1.2			1.2			1.2		GHz
t_{PLH} t_{PHL}	Propagation Delay IN to Q; D(0−10) = 0 IN to Q; D(0−10) = 1023 $\overline{EN}$ to Q; D(0−10) = 0 D0 to CASCADE	 1650 9500 1600 300	 2050 11500 2150 420	 2450 13500 2600 500	 1800 10000 1800 350	 2200 12200 2300 450	 2600 14000 2800 550	 1950 10800 2000 425	 2350 13300 2500 525	 2750 15800 3000 625	ps
t_{RANGE}	Programmable Range t_{PD} (max) − t_{PD} (min)	7850	9450		8200	10000		8850	10950		ps
Δt	Step Delay (Note 22) D0 High D1 High D2 High D3 High D4 High D5 High D6 High D7 High D8 High D9 High		 13 27 44 90 130 312 590 1100 2250 4500			 14 30 47 97 140 335 650 1180 2400 4800			 41 100 145 360 690 1300 2650 5300		ps
mono	Monotonicity (Note 28)					TBD					
t_{SKEW}	Duty Cycle Skew (Note 23) $\lvert t_{PHL} - t_{PLH} \rvert$		25			25			25		ps
t_s	Setup Time D to LEN D to IN (Note 24) $\overline{EN}$ to IN (Note 25)	 200 300 300	 0 140 150		 200 300 300	 0 160 170		 200 300 300	 0 180 180		ps
t_h	Hold Time LEN to D IN to $\overline{EN}$ (Note 26)	 200 400	 60 250		 200 400	 100 280		 200 400	 80 300		ps
t_R	Release Time $\overline{EN}$ to IN (Note 27) SET MAX to LEN SET MIN to LEN	 150 400 350	 −25 200 275		 150 400 350	 −75 250 200		 150 400 350	 −50 300 225		ps
t_{jitter}	RMS Random Clock Jitter @ 1.25 GHz		3			3			3		ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Time @ 50 MHz 20−80% (Q) 20−80% (CASCADE)	 85 100	 100 140	 135 200	 85 110	 110 150	 135 200	 95 130	 125 170	 155 220	ps

21. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}−2.0 V.
22. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
23. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
24. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
25. This setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition.
26. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/IN transition.
27. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
28. The monotonicity indicates the increasing delay value for each binary count increment on the control inputs D[0:9].

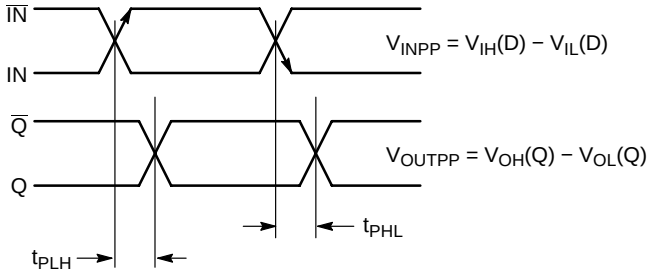


Figure 4. AC Reference Measurement

Cascading Multiple EP195s

To increase the programmable range of the EP195, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple EP195s without the need for any external gating. Furthermore, this capability requires only one more address line per added E195. Obviously, cascading multiple programmable delay chips will result in a larger programmable range: however, this increase is at the expense of a longer minimum delay.

Figure 5 illustrates the interconnect scheme for cascading two EP195s. As can be seen, this scheme can easily be expanded for larger EP195 chains. The D10 input of the EP195 is the cascade control pin. With the interconnect scheme of Figure 5 when D10 is asserted, it signals the need for a larger programmable range than is achievable with a single device. The A11 address can be added to generate a cascade output for the next EP195. For a 2−device configuration, A11 is not required.

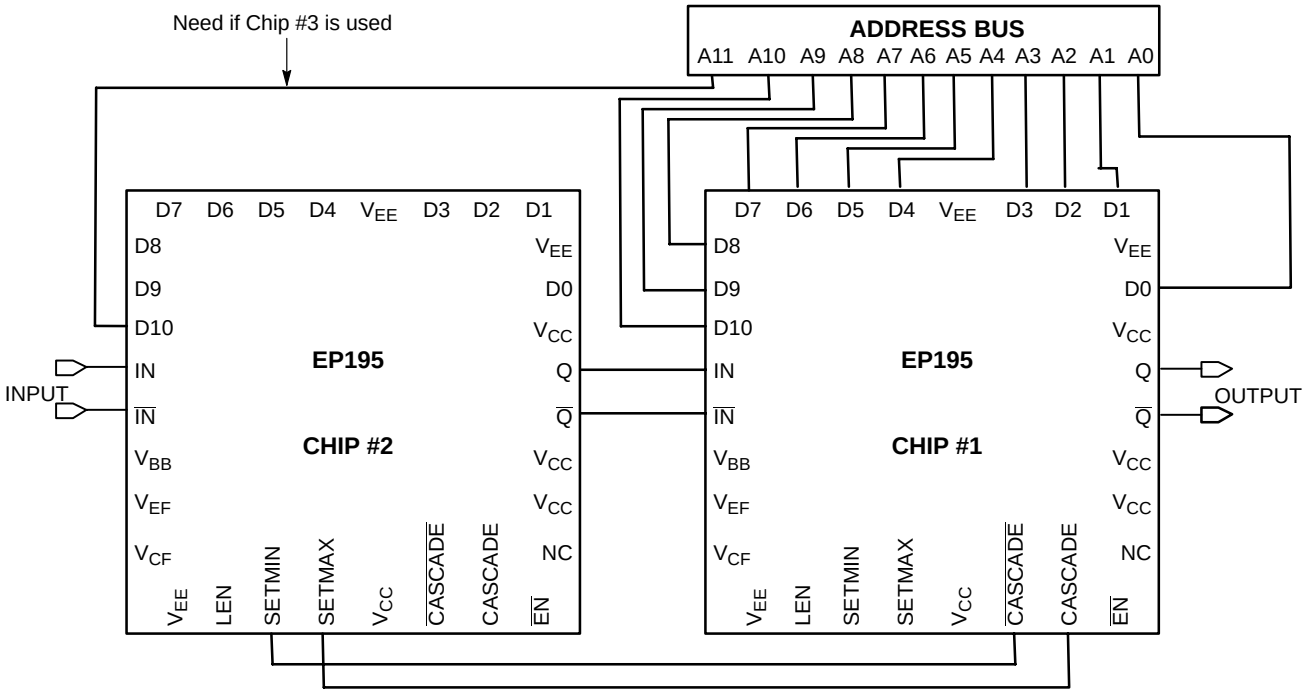


Figure 5. Cascading Interconnect Architecture

An expansion of the latch section of the block diagram is pictured in Figure 6. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D10 of chip #1 in Figure 5 is low the cascade output will also be low while the cascade bar output will be a logical high. In this condition the SET MIN pin of chip #2 will be asserted and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay.

Chip #1, on the other hand, will have both SET MIN and SET MAX deasserted so that its delay will be controlled entirely by the address bus A0—A9. If the delay needed is greater than can be achieved with 1023 gate delays (1111111111 on the A0—A9 address bus) D10 will be asserted to signal the need to cascade the delay to the next EP195 device. When D10 is asserted, the SET MIN pin of chip #2 will be deasserted and SET MAX pin asserted resulting in the device delay to be the maximum delay. Figure 7 shows the delay time of two EP195 chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 5. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.

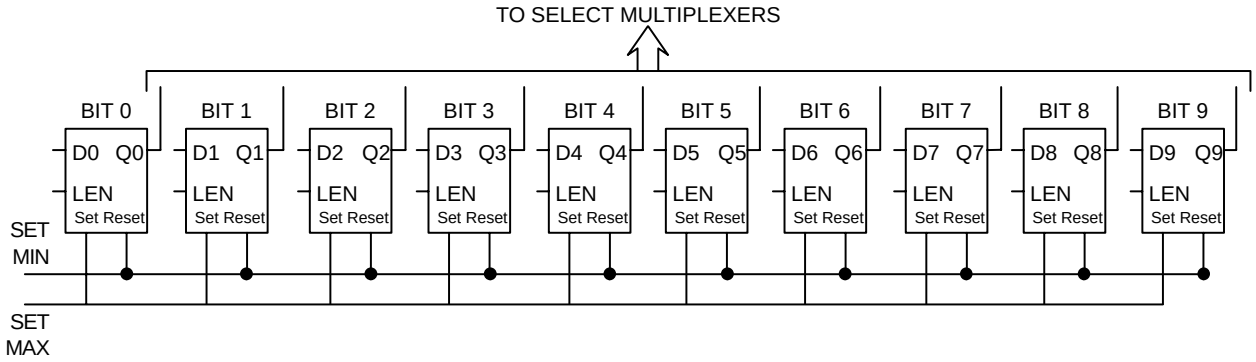


Figure 6. Expansion of the Latch Section of the EP195 Block Diagram

VARIABLE INPUT TO CHIP #1 AND *SETMIN* FOR CHIP #2												
INPUT FOR CHIP #1												Total
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Delay Value	Delay Value
0	0	0	0	0	0	0	0	0	0	0	0 ps	4400 ps
0	0	0	0	0	0	0	0	0	0	1	10 ps	4410 ps
0	0	0	0	0	0	0	0	0	1	0	20 ps	4420 ps
0	0	0	0	0	0	0	0	0	1	1	30 ps	4430 ps
0	0	0	0	0	0	0	0	1	0	0	40 ps	4440 ps
0	0	0	0	0	0	0	0	1	0	1	50 ps	4450 ps
0	0	0	0	0	0	0	0	1	1	0	60 ps	4460 ps
0	0	0	0	0	0	0	0	1	1	1	70 ps	4470 ps
0	0	0	0	0	0	0	1	0	0	0	80 ps	4480 ps
0	0	0	0	0	0	1	0	0	0	0	160 ps	4560 ps
0	0	0	0	0	1	0	0	0	0	0	220 ps	4720 ps
0	0	0	0	1	0	0	0	0	0	0	640 ps	5040 ps
0	0	0	1	0	0	0	0	0	0	0	1280 ps	5680 ps
0	0	1	0	0	0	0	0	0	0	0	2560 ps	6960 ps
0	1	0	0	0	0	0	0	0	0	0	5120 ps	9520 ps
0	1	1	1	1	1	1	1	1	1	1	10230 ps	14630 ps

VARIABLE INPUT TO CHIP #1 AND *SETMAX* FOR CHIP #2												
INPUT FOR CHIP #1												Total
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Delay Value	Delay Value
1	0	0	0	0	0	0	0	0	0	0	10240 ps	14640 ps
1	0	0	0	0	0	0	0	0	0	1	10250 ps	14650 ps
1	0	0	0	0	0	0	0	0	1	0	10260 ps	14660 ps
1	0	0	0	0	0	0	0	0	1	1	10270 ps	14670 ps
1	0	0	0	0	0	0	0	1	0	0	10280 ps	14680 ps
1	0	0	0	0	0	0	0	1	0	1	10290 ps	14690 ps
1	0	0	0	0	0	0	0	1	1	0	10300 ps	14700 ps
1	0	0	0	0	0	0	0	1	1	1	10310 ps	14710 ps
1	0	0	0	0	0	0	1	0	0	0	10320 ps	14720 ps
1	0	0	0	0	0	1	0	0	0	0	10400 ps	14800 ps
1	0	0	0	0	1	0	0	0	0	0	10560 ps	14960 ps
1	0	0	0	1	0	0	0	0	0	0	10880 ps	15280 ps
1	0	0	1	0	0	0	0	0	0	0	11520 ps	15920 ps
1	0	1	0	0	0	0	0	0	0	0	12800 ps	17200 ps
1	1	0	0	0	0	0	0	0	0	0	15360 ps	19760 ps
1	1	1	1	1	1	1	1	1	1	1	20470 ps	24870 ps

Figure 7. Delay Value of Two EP195 Cascaded

Multi−Channel Deskewing

The most practical application for EP195 is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high−speed system. To deskew multiple signal channels, each channel can be sent through each EP195 as shown in Figure 8. One signal channel can be used as reference and the other EP195s can be used to adjust the delay to eliminate the timing skews. Nearly any high−speed system can be fine−tuned (as small as 10 ps) to reduce the skew to extremely tight tolerances.

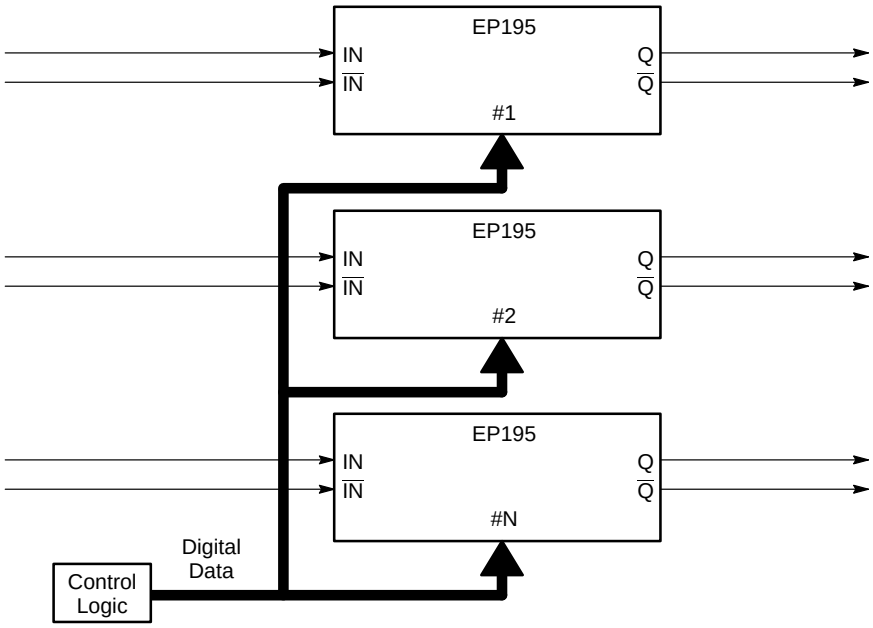


Figure 8. Multiple Channel Deskewing Diagram

Measure Unknown High Speed Device Delays

EP195s provide a possible solution to measure the unknown delay of a device with a high degree of precision. By combining two EP195s and EP31 as shown in Figure 9, the delay can be measured. The first EP195 can be set to SETMIN and its output is used to drive the unknown delay device, which in turn drives the input of a D flip−flop of EP31. The second EP195 is triggered along with the first EP195 and its output provides a clock signal for EP31. The programmed delay of the second EP195 is varied to detect the output edge from the unknown delay device.

If the programmed delay through the second EP195 is too long, the flip−flop output will be at logic high. On the other hand, if the programmed delay through the second EP195 is too short, the flip−flop output will be at a logic low. If the programmed delay is correctly fine−tuned in the second EP195, the flip−flop will bounce between logic high and logic low. The digital code in the second EP195 can be directly correlated into an accurate device delay.

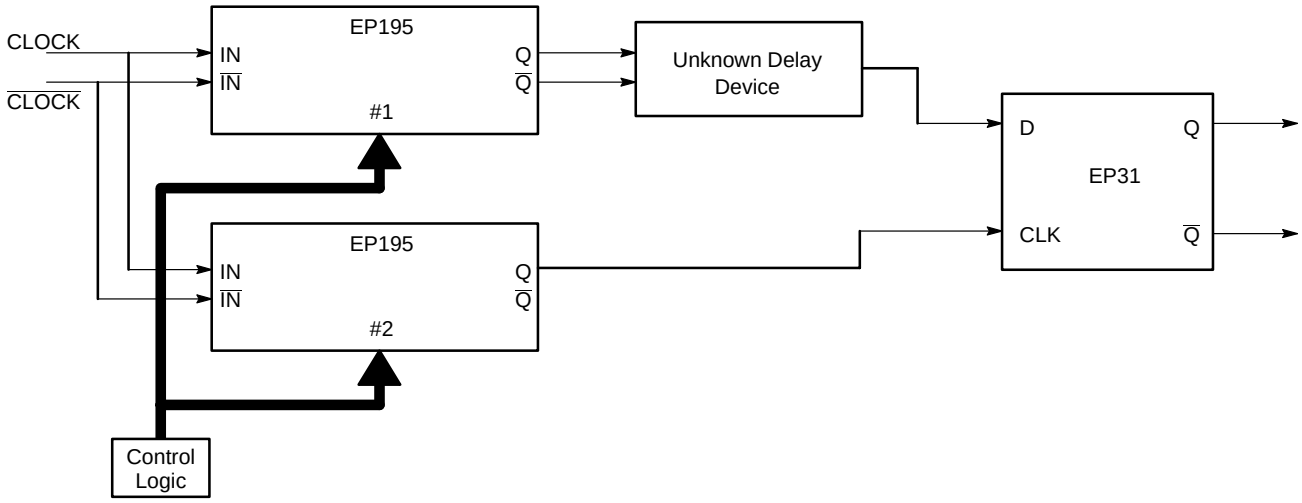


Figure 9. Multiple Channel Deskewing Diagram

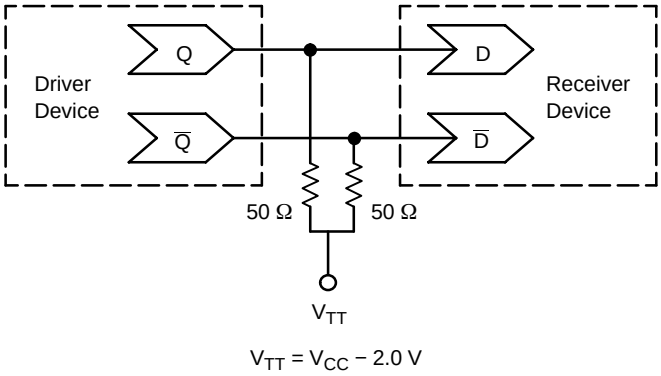


Figure 10. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 − Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 − ECLinPS Circuit Performance at Non−Standard V_{IH} Levels

AN1405 − ECL Clock Distribution Techniques

AN1406 − Designing with PECL (ECL at +5.0 V)

AN1504 − Metastability and the ECLinPS Family

AN1568 − Interfacing Between LVDS and ECL

AN1650 − Using Wire−OR Ties in ECLinPS Designs

AN1672 − The ECL Translator Guide

AND8001 − Odd Number Counters Design

AND8002 − Marking and Date Codes

AND8009 − ECLinPS Plus Spice I/O Model Kit

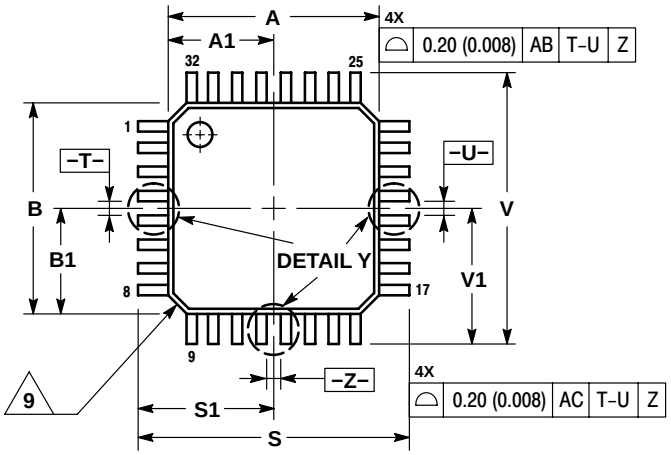
AND8020 − Termination of ECL Logic Devices

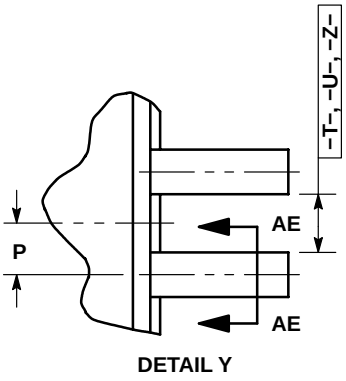
AND8090 − AC Characteristics of ECL Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

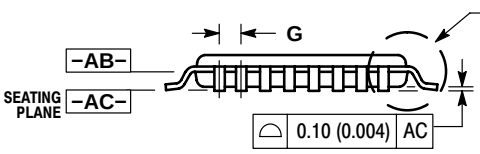
PACKAGE DIMENSIONS

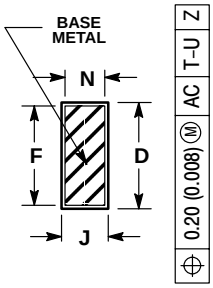
LQFP
FA SUFFIX
32−LEAD PLASTIC PACKAGE
CASE 873A−02
ISSUE A



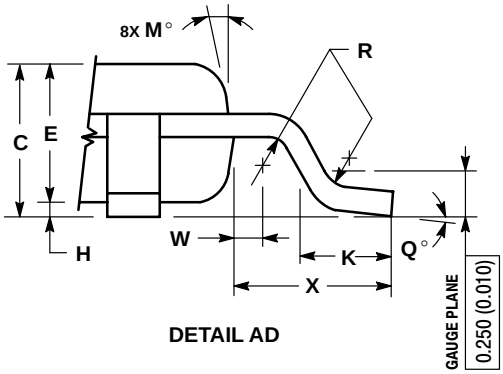


DETAIL Y





SECTION AE−AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −AB− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS −T−, −U−, AND −Z− TO BE DETERMINED AT DATUM PLANE −AB−.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE −AC−.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −AB−.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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