

MC10EP139, MC100EP139

3.3V / 5V ECL $\div 2/4$, $\div 4/5/6$ Clock Generation Chip

The MC10/100EP139 is a low skew $\div 2/4$, $\div 4/5/6$ clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device. If a single-ended input is to be used, the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01 μF capacitor.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple EP139s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EP139, the MR pin need not be exercised as the internal divider design ensures synchronization between the $\div 2/4$ and the $\div 4/5/6$ outputs of a single device. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

The 100 Series contains temperature compensation.

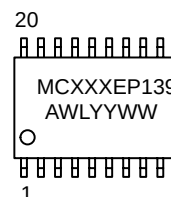
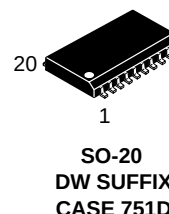
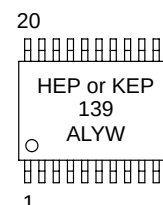
- Maximum Frequency >1.0 GHz Typical
- 50 ps Output-to-Output Skew
- PECL Mode Operating Range: $V_{CC} = 3.0 V$ to $5.5 V$ with $V_{EE} = 0 V$
- NECL Mode Operating Range: $V_{CC} = 0 V$ with $V_{EE} = -3.0 V$ to $-5.5 V$
- Open Input Default State
- Safety Clamp on Inputs
- Synchronous Enable/Disable
- Master Reset for Synchronization of Multiple Chips
- V_{BB} Output



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MARKING DIAGRAMS*



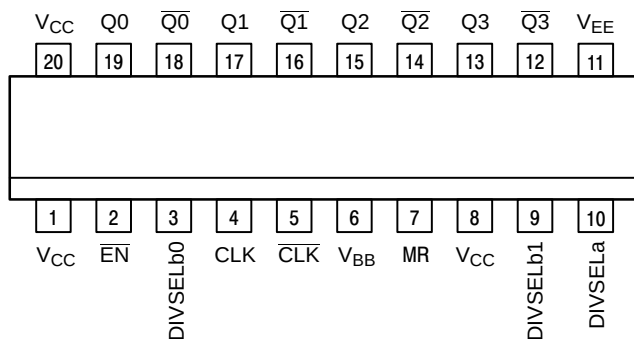
HEP = MC10EP
KEP = MC100EP
XXX = 10 or 100
A = Assembly Location
L,WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP139DT	TSSOP-20	75 Units/Rail
MC10EP139DTR2	TSSOP-20	2500 Tape & Reel
MC100EP139DT	TSSOP-20	75 Units/Rail
MC100EP139DTR2	TSSOP-20	2500 Tape & Reel
MC10EP139DW	SO-20	38 Units/Rail
MC10EP139DWR2	SO-20	1000 Tape & Reel
MC100EP139DW	SO-20	38 Units/Rail
MC100EP139DWR2	SO-20	1000 Tape & Reel

MC10EP139, MC100EP139



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
CLK*, CLK*	ECL Diff Clock Inputs
EN*	ECL Sync Enable
MR*	ECL Master Reset
V _{BB}	ECL Reference Output
Q0, Q1, Q0, Q1	ECL Diff ÷2/4 Outputs
Q2, Q3, Q2, Q3	ECL Diff ÷4/5/6 Outputs
DIVSELa*	ECL Freq. Select Input ÷ 2/4
DIVSELb0*	ECL Freq. Select Input ÷ 4/5/6
DIVSELb1*	ECL Freq. Select Input ÷ 4/5/6
V _{CC}	ECL Positive Supply
V _{EE}	ECL Negative Supply

* Pins will default low when left open.

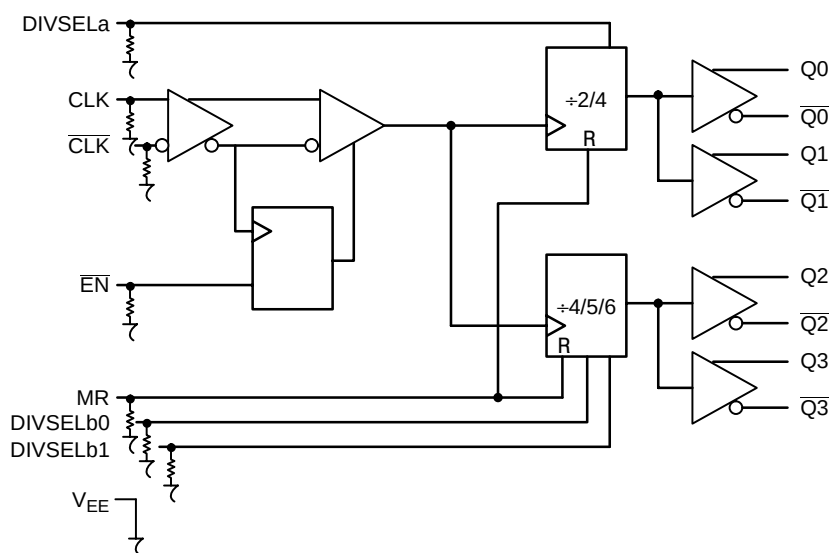


Figure 2. Logic Diagram

FUNCTION TABLES

CLK	EN	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q0:3
X	X	H	Reset Q0:3

Z = Low-to-High Transition
ZZ = High-to-Low Transition

DIVSELa	Q0:1 OUTPUTS	
L	Divide by 2	
H	Divide by 4	
DIVSELb0	DIVSELb1	Q2:3 OUTPUTS
L	L	Divide by 4
H	L	Divide by 6
L	H	Divide by 5
H	H	Divide by 5

MC10EP139, MC100EP139

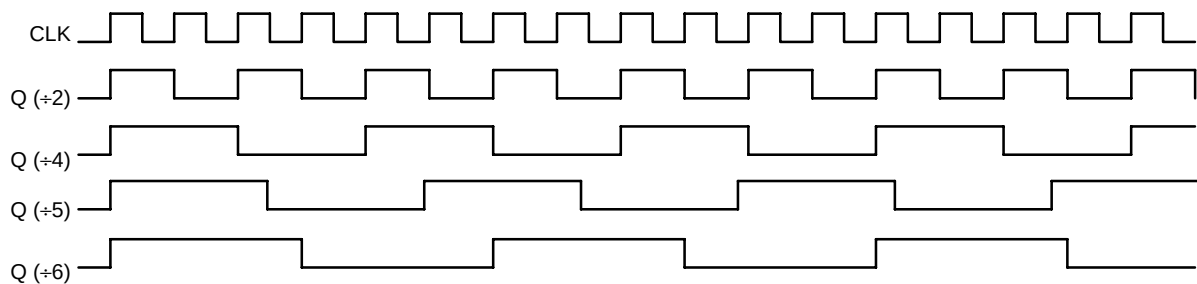


Figure 3. Timing Diagram

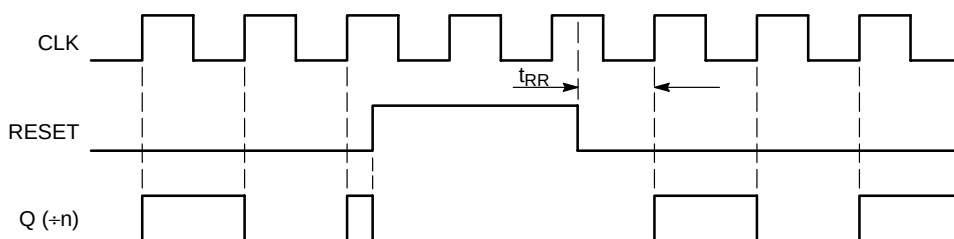


Figure 4. Timing Diagram

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 k Ω
Internal Input Pullup Resistor		N/A
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 100 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating Oxygen Index: 28 to 34		UL 94 V-0 @ 0.125 in
Transistor Count		758 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0 \text{ V}$		6	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0 \text{ V}$		-6	V
V_I	PECL Mode Input Voltage	$V_{EE} = 0 \text{ V}$	$V_I \leq V_{CC}$	6	V
	NECL Mode Input Voltage	$V_{CC} = 0 \text{ V}$	$V_I \geq V_{EE}$	-6	V
I_{out}	Output Current	Continuous Surge		50	mA
				100	mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM	20 TSSOP	140	$^{\circ}\text{C/W}$
		500 LFPM	20 TSSOP	100	$^{\circ}\text{C/W}$
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	20 TSSOP	23 to 41	$^{\circ}\text{C/W}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM	20 SOIC	90	$^{\circ}\text{C/W}$
		500 LFPM	20 SOIC	60	$^{\circ}\text{C/W}$
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	20 SOIC	33 to 35	$^{\circ}\text{C/W}$
T_{sol}	Wave Solder	<2 to 3 sec @ 248 $^{\circ}\text{C}$		265	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which device damage may occur.

MC10EP139, MC100EP139

10EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 3)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	65	82	105	65	83	105	65	84	105	mA
V_{OH}	Output HIGH Voltage (Note 4)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 4)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1365		1690	1460		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

3. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -2.2 V.

4. All loading with 50 Ω to V_{CC} -2.0 volts.

5. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

10EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 6)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	65	82	105	65	83	105	65	84	105	mA
V_{OH}	Output HIGH Voltage (Note 7)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 7)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 8)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +2.0 V to -0.5 V.

7. All loading with 50 Ω to V_{CC} -2.0 volts.

8. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

10EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 9)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	65	82	105	65	83	105	65	84	105	mA
V_{OH}	Output HIGH Voltage (Note 10)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
V_{OL}	Output LOW Voltage (Note 10)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
V_{BB}	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 11)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

9. Input and output parameters vary 1:1 with V_{CC} .

10. All loading with 50 Ω to V_{CC} -2.0 volts.

11. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC10EP139, MC100EP139

100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 12)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	70	83	100	70	87	105	75	90	110	mA
V_{OH}	Output HIGH Voltage (Note 13)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 13)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 14)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

12. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -2.2 V.

13. All loading with 50 Ω to V_{CC} -2.0 volts.

14. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 15)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	70	85	100	70	90	105	75	95	110	mA
V_{OH}	Output HIGH Voltage (Note 16)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 16)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
V_{BB}	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 17)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

15. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +2.0 V to -0.5 V.

16. All loading with 50 Ω to V_{CC} -2.0 volts.

17. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 18)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	70	85	100	70	90	105	75	95	110	mA
V_{OH}	Output HIGH Voltage (Note 19)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 19)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{BB}	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 20)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

18. Input and output parameters vary 1:1 with V_{CC} .

19. All loading with 50 Ω to V_{CC} -2.0 volts.

20. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC10EP139, MC100EP139

AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V}$ to -5.5 V or $V_{CC} = 3.0\text{ V}$ to 5.5 V ; $V_{EE} = 0\text{ V}$ (Note 21)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Frequency (See Figure 5 $F_{\max}/\text{JITTER}$)		> 1			> 1			> 1		GHz
t_{PLH} , t_{PHL}	Propagation Delay CLK, Q (Diff) MR, Q	550 700	700 800	800 900	600 700	750 850	900 1000	675 800	825 950	975 1100	ps
t_{RR}	Reset Recovery	200	100		200	100		165	100		ps
t_{s}	Setup Time $\overline{\text{EN}}$, CLK DIVSEL, CLK	200 400	120 180		200 400	120 180		200 400	120 180		ps
t_{h}	Hold Time CLK, $\overline{\text{EN}}$ CLK, DIVSEL	100 200	50 140		100 200	50 140		100 200	50 140		ps
t_{PW}	Minimum Pulse Width MR	550	450		550	450		550	450		ps
t_{SKEW}	Within Device Skew Q, $\overline{\text{Q}}$ Device-to-Device Skew (Note 22)		50 200	100 300		50 200	100 300		50 200	100 300	ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 5 $F_{\max}/\text{JITTER}$)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
t_{r} t_{f}	Output Rise/Fall Times Q, $\overline{\text{Q}}$ (20% - 80%)	110	180	250	125	190	275	150	215	300	ps

21. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC}-2.0\text{ V}$.

22. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

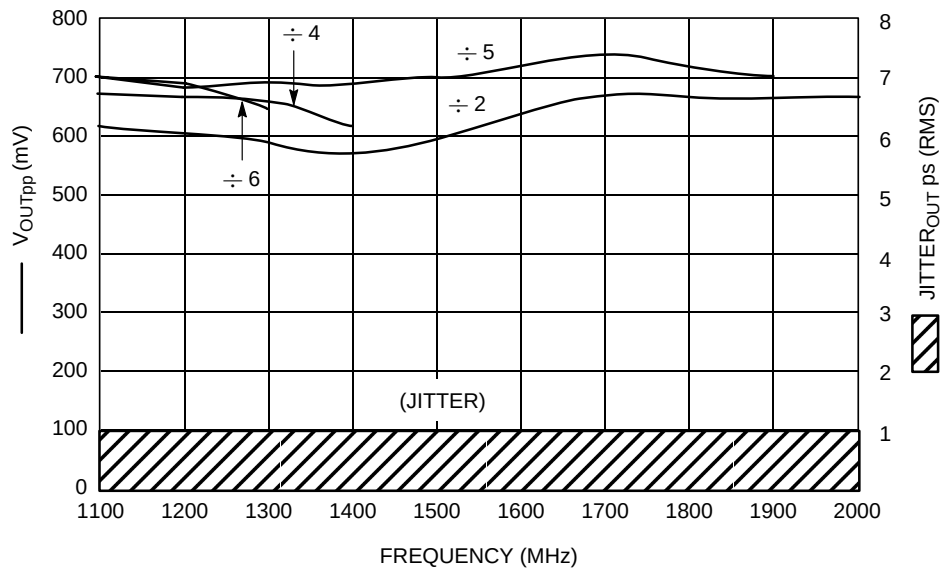


Figure 5. $F_{\max}/\text{Jitter}$

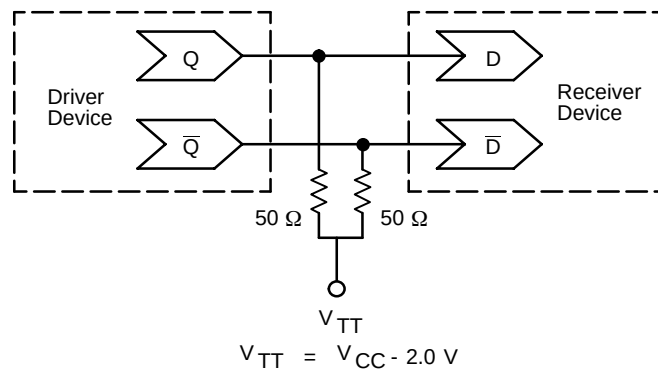


Figure 6. Typical Termination for Output Driver and Device Evaluation
 (See Application Note AND8020 - Termination of ECL Logic Devices.)

Resource Reference of Application Notes

- AN1404** - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** - ECL Clock Distribution Techniques
- AN1406** - Designing with PECL (ECL at +5.0 V)
- AN1504** - Metastability and the ECLinPS Family
- AN1568** - Interfacing Between LVDS and ECL
- AN1650** - Using Wire-OR Ties in ECLinPS Designs
- AN1672** - The ECL Translator Guide
- AND8001** - Odd Number Counters Design
- AND8002** - Marking and Date Codes
- AND8009** - ECLinPS Plus Spice I/O Model Kit
- AND8020** - Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

MC10EP139, MC100EP139

PACKAGE DIMENSIONS

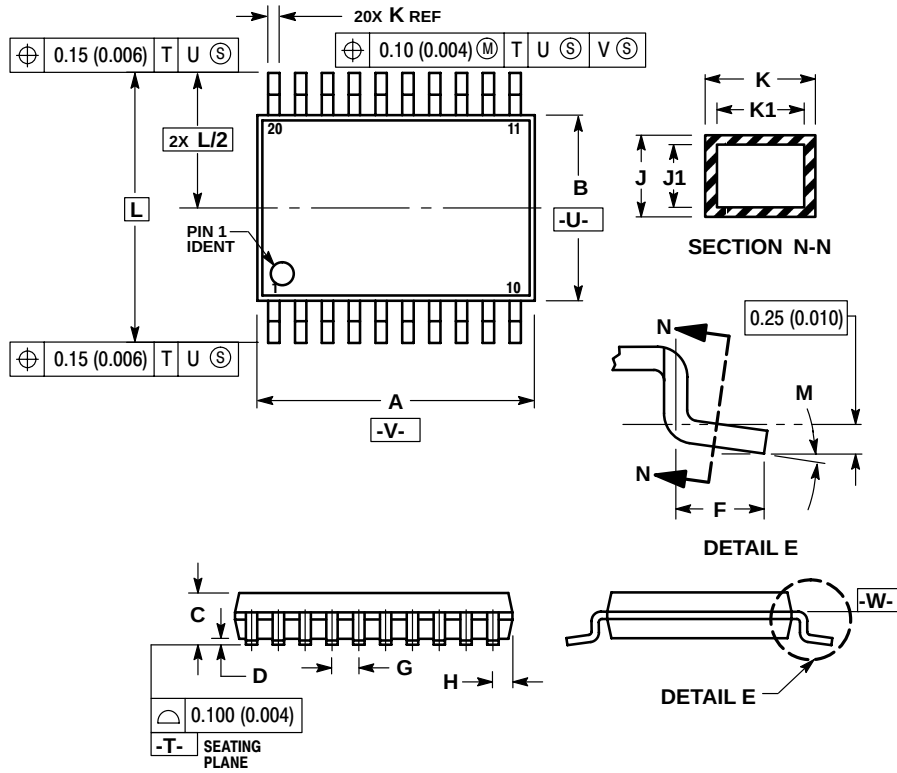
TSSOP-20

DT SUFFIX

PLASTIC TSSOP PACKAGE

CASE 948E-02

ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Notes

Notes

MC10EP139, MC100EP139

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