

# MC10ELT24, MC100ELT24

## 5V TTL to Differential ECL Translator

The MC10ELT/100ELT24 is a TTL to differential ECL translator. Because ECL levels are used a +5 V, -5.2 V (or -4.5 V) and ground are required. The small outline 8-lead package and the single gate of the ELT24 makes it ideal for those applications where space, performance and low power are at a premium.

The 100 Series contains temperature compensation.

- 0.8 ns  $t_{PHL}$ , 0.95 ns  $t_{PLH}$  Typical Propagation Delay
- PNP TTL Inputs for Minimal Loading
- Flow Through Pinouts
- Operating Range:  $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{EE} = -4.2\text{ V to }-5.5\text{ V}$  with  $GND = 0\text{ V}$

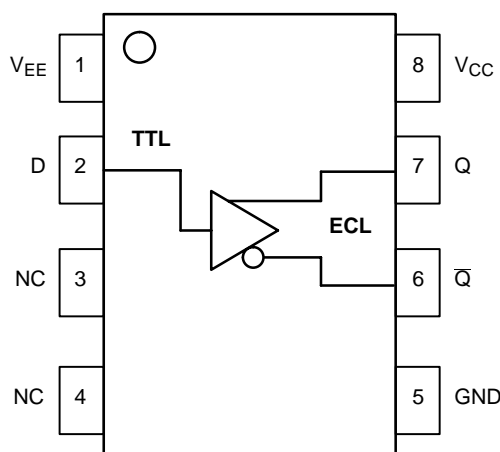


Figure 1. Logic Diagram and Pinout Assignment

### PIN DESCRIPTION

PIN	FUNCTION
Q, $\bar{Q}$	ECL Differential Outputs*
D	TTL Input
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply
GND	Ground
NC	No Connect

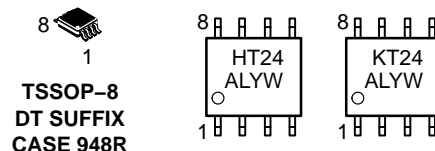
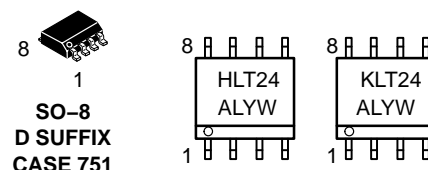
\* Output state undetermined when inputs are open.



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### MARKING DIAGRAMS\*



H = MC10                      L = Wafer Lot  
K = MC100                  Y = Year  
A = Assembly Location    W = Work Week

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

Device	Package	Shipping†
MC10ELT24D	SO-8	98 Units/Rail
MC10ELT24DR2	SO-8	2500 Tape & Reel
MC100ELT24D	SO-8	98 Units/Rail
MC100ELT24DR2	SO-8	2500 Tape & Reel
MC10ELT24DT	TSSOP-8	98 Units/Rail
MC10ELT24DTR2	TSSOP-8	2500 Tape & Reel
MC100ELT24DT	TSSOP-8	98 Units/Rail
MC100ELT24DTR2	TSSOP-8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection	Human Body Model Machine Model
	> 4 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34
	UL 94 V-0 @ 0.125 in
Transistor Count	51
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

## MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	Positive Power Supply	GND = 0 V	$V_{EE} = -5.0$ V	7	V
$V_{EE}$	Negative Power Supply	GND = 0 V	$V_{CC} = +5.0$ V	-8	V
$V_{IN}$	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	0 to $V_{CC}$	V
$I_{out}$	Output Current	Continuous Surge		50 100	mA mA
$T_A$	Operating Temperature Range			-40 to +85	°C
$T_{stg}$	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	SO-8 SO-8	190 130	°C/W °C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SO-8	41 to 44	°C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 $\pm 5\%$	°C/W
$T_{sol}$	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

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## 10ELT SERIES NECL OUTPUT DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$ ; $V_{EE} = -5.0\text{ V}$ ; $GND = 0\text{ V}$ (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{CC}$	$V_{CC}$ Power Supply Current			7.0		4.5	7.0			7.0	mA
$I_{EE}$	Power Supply Current			18		12.5	18			18	mA
$V_{OH}$	Output HIGH Voltage (Note 4)	-1080	-990	-890	-980	-895	-810	-910	-815	-720	mV
$V_{OL}$	Output LOW Voltage (Note 4)	-1950	-1800	-1650	-1950	-1790	-1630	-1950	-1773	-1595	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

- Output parameters vary 1:1 with GND.  $V_{CC}$  can vary 4.5 V / 5.5 V.  $V_{EE}$  can vary -4.2 V / -5.5 V.
- Outputs are terminated through a 50  $\Omega$  resistor to GND - 2 V.

## 100ELT SERIES NECL OUTPUT DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$ ; $V_{EE} = -5.0\text{ V}$ ; $GND = 0\text{ V}$ (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{CC}$	$V_{CC}$ Power Supply Current			7.0		4.5	7.0			7.0	mA
$I_{EE}$	Power Supply Current			18		12.5	18			18	mA
$V_{OH}$	Output HIGH Voltage (Note 6)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 6)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

- Output parameters vary 1:1 with GND.  $V_{CC}$  can vary 4.5 V / 5.5 V.  $V_{EE}$  can vary -4.2 V / -5.5 V.
- Outputs are terminated through a 50  $\Omega$  resistor to GND - 2 V.

## TTL INPUT DC CHARACTERISTICS $V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$ ; $V_{EE} = -4.2\text{ V}$ to $-5.5\text{ V}$ ; $GND = 0.0\text{ V}$ ; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

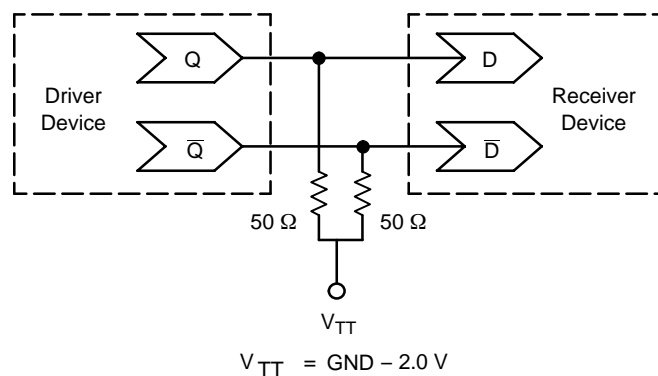
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IHH}$	Input HIGH Current	$V_{IN} = 7.0\text{ V}$			100	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{IN} = 0.5\text{ V}$			-0.6	mA
$V_{IK}$	Input Clamp Diode Voltage	$I_{IN} = -18\text{ mA}$			-1.2	V
$V_{IH}$	Input HIGH Voltage		2.0			V
$V_{IL}$	Input LOW Voltage				0.8	V

## AC CHARACTERISTICS $V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$ ; $V_{EE} = -4.2\text{ V}$ to $-5.5\text{ V}$ ; $GND = 0.0\text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency					400					MHz
$t_{PLH}$	Propagation Delay (Note 7) 1.5 V to 50%	0.7		1.3	0.65	0.95	1.25	0.65		1.25	ns
$t_{PHL}$	Propagation Delay (Note 7) 1.5 V to 50%	0.4		1.0	0.50	0.80	1.10	0.70		1.30	ns
$t_{JITTER}$	Random Clock Jitter (RMS)					2.5					ps
$t_r/t_f$	Output Rise/Fall Time (20-80%)	0.25		1.25	0.25		1.25	0.25		1.25	ns

- Specifications for standard TTL input signal.
- Devices are designed to meet the AC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

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**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

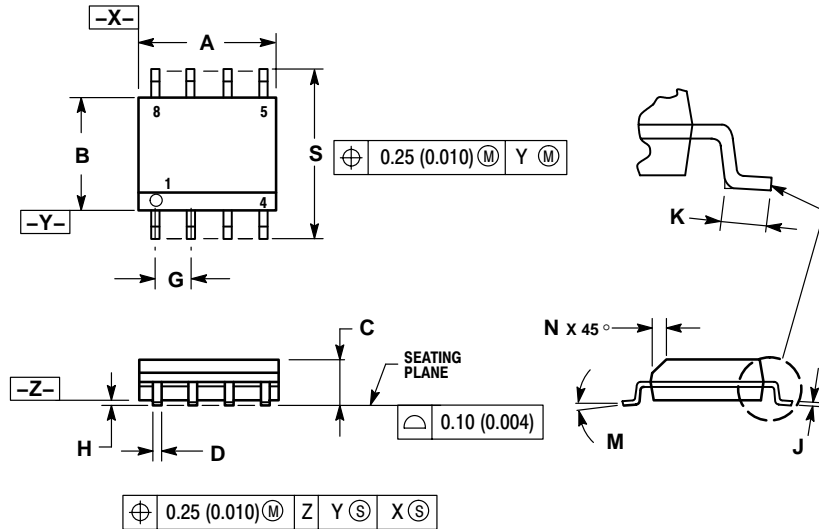
### Resource Reference of Application Notes

- |                |   |
|----------------|---|
| <b>AN1404</b>  | – ECLinPS Circuit Performance at Non-Standard $V_{IH}$ Levels |
| <b>AN1405</b>  | – ECL Clock Distribution Techniques                           |
| <b>AN1406</b>  | – Designing with PECL (ECL at +5.0 V)                         |
| <b>AN1503</b>  | – ECLinPS I/O SPICE Modeling Kit                              |
| <b>AN1504</b>  | – Metastability and the ECLinPS Family                        |
| <b>AN1560</b>  | – Low Voltage ECLinPS SPICE Modeling Kit                      |
| <b>AN1568</b>  | – Interfacing Between LVDS and ECL                            |
| <b>AN1596</b>  | – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit      |
| <b>AN1650</b>  | – Using Wire-OR Ties in ECLinPS Designs                       |
| <b>AN1672</b>  | – The ECL Translator Guide                                    |
| <b>AND8001</b> | – Odd Number Counters Design                                  |
| <b>AND8002</b> | – Marking and Date Codes                                      |
| <b>AND8020</b> | – Termination of ECL Logic Devices                            |
| <b>AND8090</b> | – AC Characteristics of ECL Devices                           |

# MC10ELT24, MC100ELT24

## PACKAGE DIMENSIONS

### SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE AA



#### NOTES:

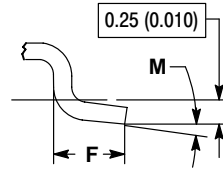
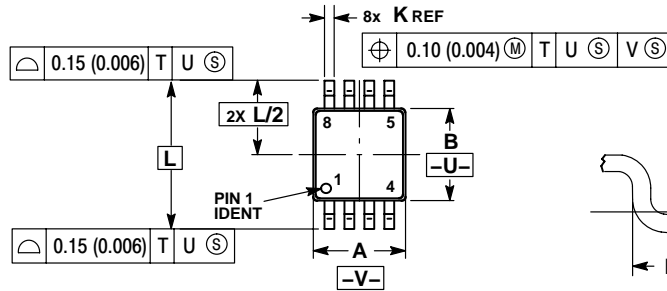
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
E	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

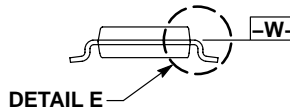
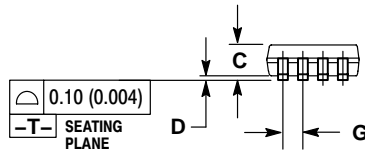
# MC10ELT24, MC100ELT24

## PACKAGE DIMENSIONS

**TSSOP-8**  
**DT SUFFIX**  
 PLASTIC TSSOP PACKAGE  
 CASE 948R-02  
 ISSUE A



**DETAIL E**




**DETAIL E**

### NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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