MC10E431, MC100E431

5V ECL 3-Bit Differential Flip-Flop

The MC10E/100E431 is a 3-bit flip-flop with differential clock, data input and data output.

The asynchronous Set and Reset controls are edge-triggered rather than level controlled. This allows the user to rapidly set or reset the flip-flop and then continue clocking at the next clock edge, without the necessity of de-asserting the set/reset signal (as would be the case with a level controlled set/reset).

The E431 is also designed with larger internal swings, an approach intended to minimize the time spent crossing the threshold region and thus reduce the metastability susceptibility window.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the $\overline{D}$ and the $\overline{CLK}$ sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5 V below V_{CC}.

The 100 Series contains temperature compensation.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 µF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- Edge-Triggered Asynchronous Set and Reset
- Differential D, CLK and Q; V_{BB} Reference Available
- 1100 MHz Min. Toggle Frequency
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V
  with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V
  with V_{EE} = −4.2 V to −5.7 V
- Internal Input 50 KΩ Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V−0 @ 0.125 in,
  Oxygen Index: 28 to 34
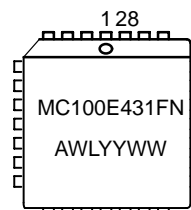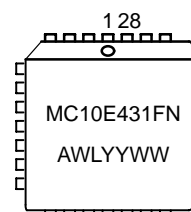- Transistor Count = 348 devices

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MARKING DIAGRAMS
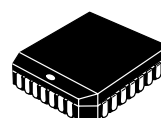
PLCC−28
FN SUFFIX
CASE 776

1 28

MC10E431FN
AWLYYWW

1 28

MC100E431FN
AWLYYWW

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MC10E431FN	PLCC−28	37 Units/Rail
MC10E431FNR2	PLCC−28	500 Units/Reel
MC100E431FN	PLCC−28	37 Units/Rail
MC100E431FNR2	PLCC−28	500 Units/Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
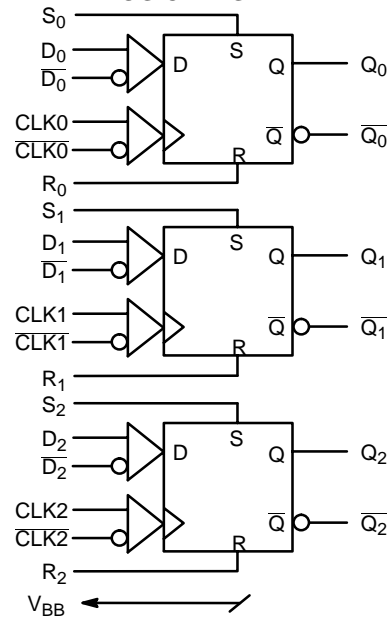
MC10E431, MC100E431

LOGIC DIAGRAM AND PINOUT ASSIGNMENT

Pinout: 28-Lead PLCC
(Top View)
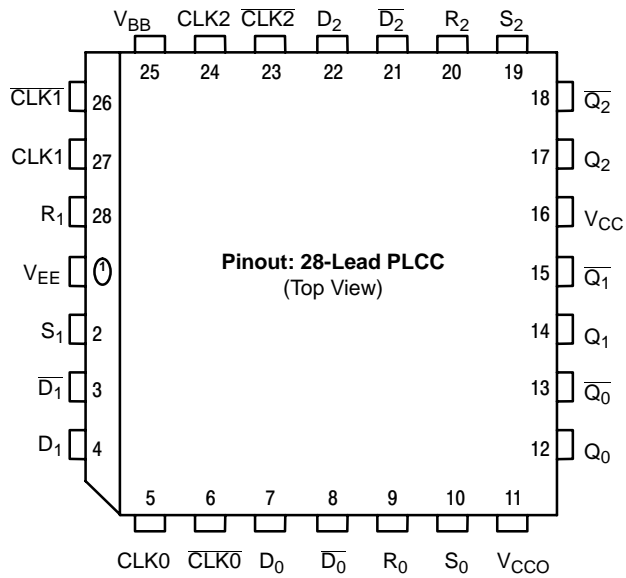
* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally
connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM

PIN DESCRIPTION

PIN	FUNCTION
D[0:2], $\overline{D}$[0:2]	ECL Differential Data Inputs
CLK[0:2], $\overline{CLK}$[0:2]	ECL Differential Clock
S[0:2]	ECL Edge Triggered Set Inputs
R[0:2]	ECL Edge Triggered Reset Input
Q[0:2], $\overline{Q}$[0:2]	ECL Differential Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE

Dn	CLKn	Rn	Sn	Qn
L	Z	L	L	L
H	Z	L	L	H
X	X	Z	L	L
X	X	L	Z	H

Z = Low to high transition
X = Don't Care

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MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_I	PECL Mode Input Voltage	V_{EE} = 0 V	$V_I \leq V_{CC}$	6	V
	NECL Mode Input Voltage	V_{CC} = 0 V	$V_I \geq V_{EE}$	−6	V
I_{out}	Output Current	Continuous		50	mA
		Surge		100	mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 LFPM	28 PLCC	63.5	°C/W
		500 LFPM	28 PLCC	43.5	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	28 PLCC	22 to 26	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 2)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		110	132		110	132		110	132	mA
V_{OH}	Output HIGH Voltage (Note 3)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 3)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single−Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	2.7		5.0	2.7		5.0	2.7		5.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.06 V.
3. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2 V.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= −5.0 V (Note 5)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		110	132		110	132		110	132	mA
V_{OH}	Output HIGH Voltage (Note 6)	−1020	−930	−840	−980	−895	−810	−910	−815	−720	mV
V_{OL}	Output LOW Voltage (Note 6)	−1950	−1790	−1630	−1950	−1790	−1630	−1950	−1773	−1595	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1170	−1005	−840	−1130	−970	−810	−1060	−890	−720	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1950	−1715	−1480	−1950	−1715	−1480	−1950	−1698	−1445	mV
V_{BB}	Output Voltage Reference	−1.38		−1.37	−1.35		−1.25	−1.31		−1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)	−2.3		0.0	−2.3		0.0	−2.3		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.06 V.
6. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2 V.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 8)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		110	132		110	132		127	152	mA
V_{OH}	Output HIGH Voltage (Note 9)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 9)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	3835	3975	4120	3835	3975	4120	3835	3975	4120	mV
V_{IL}	Input LOW Voltage (Single−Ended)	3190	3355	3525	3190	3355	3525	3190	3355	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	2.7		5.0	2.7		5.0	2.7		5.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

8. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.8 V.
9. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2 V.
10. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= −5.0 V (Note 11)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		110	132		110	132		127	152	mA
V_{OH}	Output HIGH Voltage (Note 12)	−1025	−950	−880	−1025	−950	−880	−1025	−950	−880	mV
V_{OL}	Output LOW Voltage (Note 12)	−1810	−1705	−1620	−1810	−1745	−1620	−1810	−1740	−1620	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1165	−1025	−880	−1165	−1025	−880	−1165	−1025	−880	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1810	−1645	−1475	−1810	−1645	−1475	−1810	−1645	−1475	mV
V_{BB}	Output Voltage Reference	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	−2.3		0.0	−2.3		0.0	−2.3		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

11. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.8 V.
12. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2 V.
13. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

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AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V   or V_{CCx}= 0.0 V; V_{EE}= −5.0 V (Note 14)

Symbol	Characteristic		−40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency						1.1					GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	CLK (Diff) CLK (SE) R S	410 460 500 500	600 600 725 725	790 840 975 975	450 400 550 550	600 600 725 725	750 800 925 925	450 400 550 550	600 600 725 725	750 800 925 925	ps
t_S	Setup Time	D R (Note 15) S (Note 15)	250 1100 1100	0 700 700		200 1000 1000	0 700 700		200 1000 1000	0 700 700		ps
t_H	Hold Time	D	250	0		200	0		200	0		ps
t_{PW}	Minimum Pulse Width	CLK	400			400			400			ps
t_{skew}	Within-Device Skew (Note 16)			50						50		ps
t_{JITTER}	Random Clock Jitter (RMS)			< 1			< 1			< 1		ps
V_{PP}	Input Voltage Swing (Differential Configuration)		150		1000	150		1000	150		1000	mV
t_r/t_f	Rise/Fall Times (20–80%)		250	450	700				275	450	650	ps

14. 10 Series: V_{EE} can vary −0.46 V / +0.06 V.
    100 Series: V_{EE} can vary −0.46 V / +0.8 V.
15. These setup times define the minimum time the CLK or SET/RESET input must wait after the assertion of the RESET/SET input to assure the proper operation of the flip-flop.
16. Within-device skew is defined as identical transitions on similar paths through a device.

$$V_{TT} = V_{CC} - 2.0\ V$$
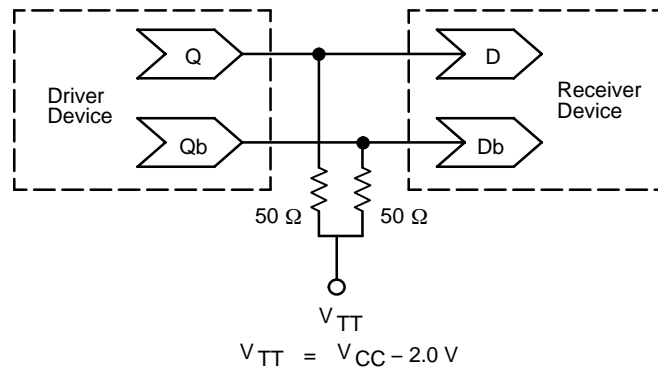
**Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)**

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

PACKAGE DIMENSIONS

PLCC–28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE E

VIEW D-D

VIEW S
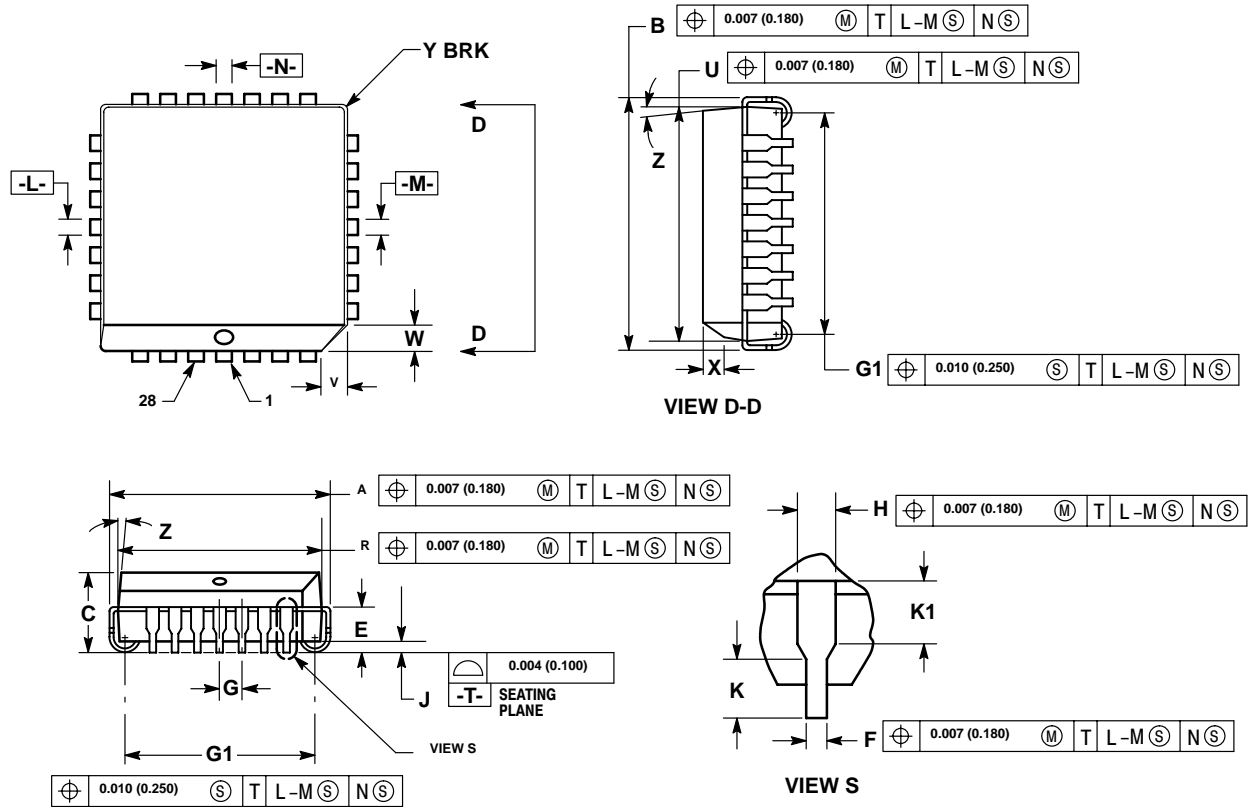
NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

MC10E431, MC100E431

PUBLICATION ORDERING INFORMATION