MC100LVEP210

2.5V / 3.3V 1:5 Dual Differential ECL/PECL/HSTL Clock Driver

The MC100LVEP210 is a low skew 1-to-5 dual differential driver, designed with clock distribution in mind. The ECL/PECL input signals can be either differential or single-ended if the V_{BB} output is used. The signal is fanned out to 5 identical differential outputs. HSTL inputs can be used when the EP210 is operating in PECL mode.

The LVEP210 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure the tight skew specification is realized, both sides of the differential output need to be terminated identically into 50 Ω even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The MC100LVEP210, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVEP210 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single-ended CLK input operation is limited to a $V_{CC} \geq 3.0$ V in PECL mode, or $V_{EE} \leq -3.0$ V in ECL mode.

Designers can take advantage of the LVEP210's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Application Note AN1406/D.

- 85 ps Typical Device-to- Device Skew
- 20 ps Typical Output-to-Output Skew
- V_{BB} Output
- Jitter Less than 1 ps RMS
- 350 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode Operating Range: V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -2.375 V to -3.8 V
- Open Input Default State
- LVDS Input Compatible
- Fully Compatible with Motorola MC100EP210

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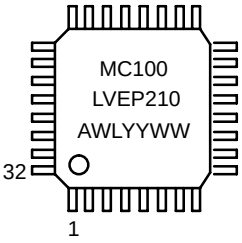
MARKING DIAGRAM*

32-LEAD LQFP
FA SUFFIX
CASE 873A

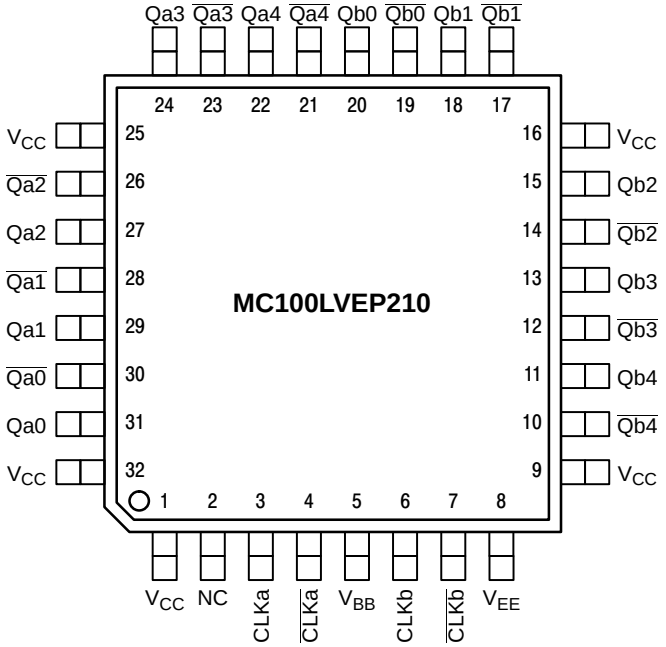


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEP210FA	LQFP	250 Units/Tray
MC100LVEP210FAR2	LQFP	2000 Tape & Reel



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32-Lead LQFP Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
CLKn*, $\overline{CLKn}$**	ECL/PECL/HSTL CLK Inputs
Qn0:4, $\overline{Qn0:4}$	ECL/PECL Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default LOW when left open.
** Pins will default to $V_{CC}/2$ when left open.

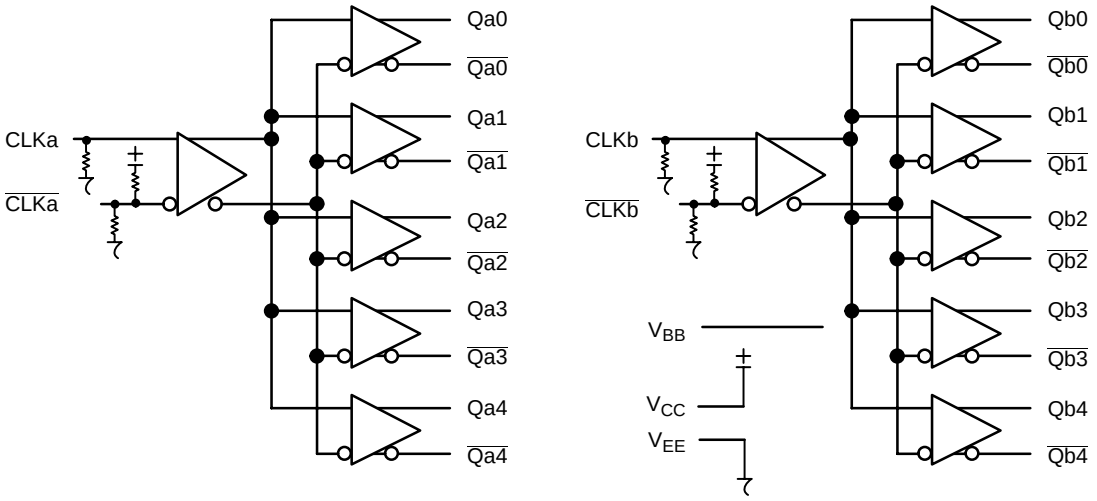


Figure 2. Logic Diagram

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pull-up Resistor		37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV
Moisture Sensitivity (Note 1)		Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		461 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		-6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 -6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
q_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	32 LQFP	12 to 17	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

PECL DC CHARACTERISTICS V_{CC} = 3.3 V; V_{EE} = 0 V (Note 3)

		-40 °C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	60	70	90	60	70	90	60	70	90	mA
V_{OH}	Output HIGH Voltage (Note 4)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 4)	1355	1480	1700	1355	1480	1700	1355	1480	1700	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1675	1490		1675	1490		1675	mV
V_{BB}	Output Reference Voltage (Note 5)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 100LVEP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary + 0.925 V to -0.5 V.
4. All loading with 50 Ω to V_{CC}-2.0 volts.
5. Single ended input operation is limited $V_{CC} \ge 3.0$ V in PECL mode.
6. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

PECL DC CHARACTERISTICS V_{CC} = 2.5 V; V_{EE} = 0 V (Note 7)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	60	70	90	60	70	90	60	70	90	mA
V_{OH}	Output HIGH Voltage (Note 8)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 8)	555	680	900	555	680	900	555	680	900	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 9)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 100LVEP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

7. Input and output parameters vary 1:1 with V_{CC}.. V_{EE} can vary + 0.125 V to -1.3 V.
8. All loading with 50 Ω to V_{EE}.
9. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NECL DC CHARACTERISTICS V_{CC} = 0 V, V_{EE} = -2.375 V to -3.8 V (Note 10)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	60	70	90	60	70	90	60	70	90	mA
V_{OH}	Output HIGH Voltage (Note 11)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 11)	-1945	-1820	-1600	-1945	-1820	-1600	-1945	-1820	-1600	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1810		-1625	-1810		-1625	-1810		-1625	mV
V_{BB}	Output Reference Voltage (Note 12)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 13)	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 -150			0.5 -150			0.5 -150		150	μA

NOTE: 100LVEP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

10. Input and output parameters vary 1:1 with V_{CC}.
11. All loading with 50 Ω to V_{CC}-2.0 volts.
12. Single ended input operation is limited $V_{EE} \leq$ -3.0V in NECL mode.
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

HSTL DC CHARACTERISTICS V_{CC} = 2.375 to 3.8 V, V_{EE} = 0 V

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	1200			1200			1200			mV
V_{IL}	Input LOW Voltage			400			400			400	mV
V_{CM}	Input Crossover Voltage	680		900	680		900	680		900	mV
I_{CC}	Power Supply Current	60	70	90	60	70	90	60	70	90	mA

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = -2.375 to -3.8 V or V_{CC} = 2.375 to 3.8 V; V_{EE} = 0 V (Note 14)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
$f_{maxPECL/HSTL}$	Maximum Frequency (See Figure 3. F_{max}/JITTER)		> 3			> 3			> 3		GHz
t_{PLH} t_{PHL}	Propagation Delay Propagation Delay @ 2.5 V	220	300	380	270	350	430	300 330	500 410	750 490	ps
t_{skew}	Within-Device Skew (Note 15) Device-to-Device Skew (Note 16)		20 85	25 160		20 85	25 160		20 85	35 160	ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 3. F_{max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	Output Rise/Fall Time (20%-80%)	100	170	250	120	190	270	150	280	350	ps

14. Measured with 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2 V.
15. Skew is measured between outputs under identical transitions of similar paths through a device.
16. Device-to-Device skew for identical transitions at identical V_{CC} levels.

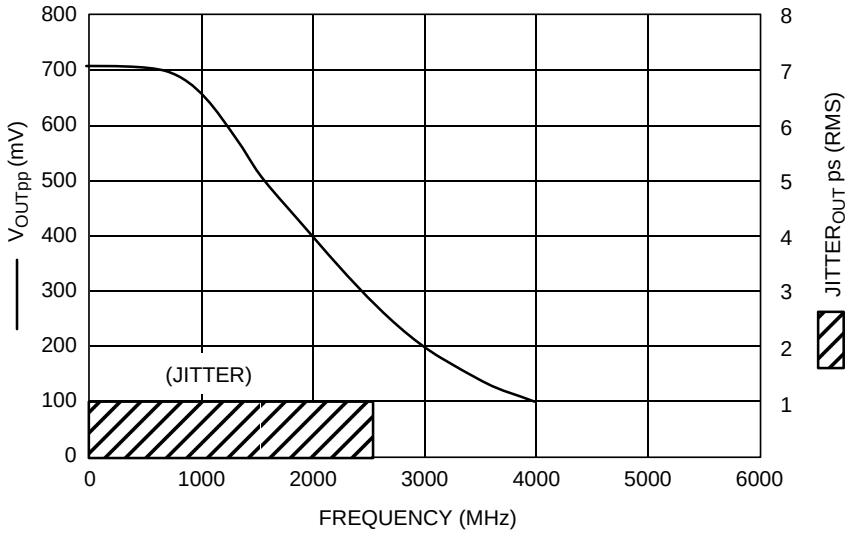


Figure 3. F_{max}/Jitter

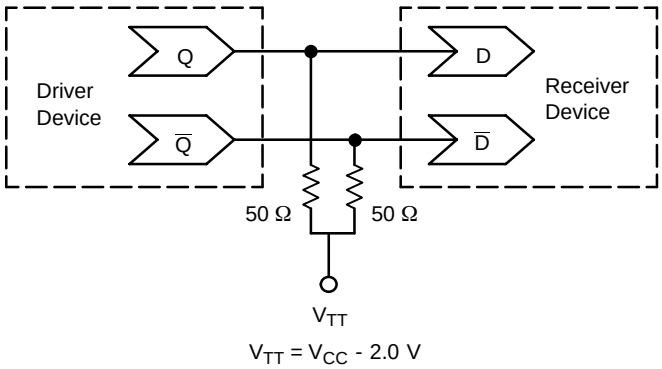


Figure 4. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 - Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels

AN1405 - ECL Clock Distribution Techniques

AN1406 - Designing with PECL (ECL at +5.0 V)

AN1504 - Metastability and the ECLinPS Family

AN1568 - Interfacing Between LVDS and ECL

AN1650 - Using Wire-OR Ties in ECLinPS Designs

AN1672 - The ECL Translator Guide

AND8001 - Odd Number Counters Design

AND8002 - Marking and Date Codes

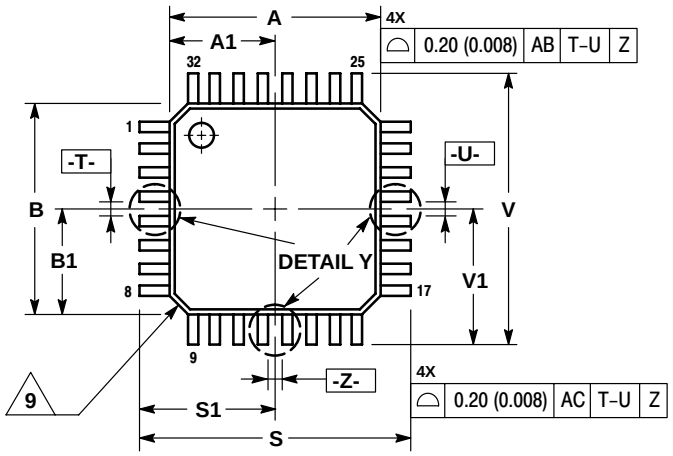
AND8009 - ECLinPS Plus Spice I/O Model Kit

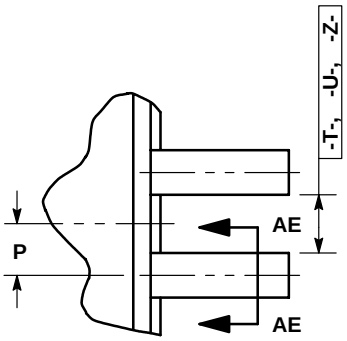
AND8020 - Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

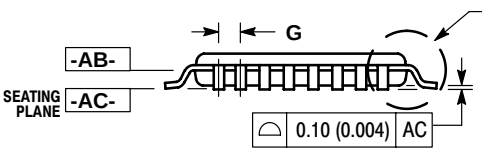
PACKAGE DIMENSIONS

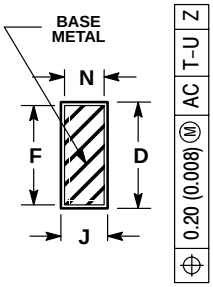
LQFP
FA SUFFIX
32-LEAD PLASTIC PACKAGE
CASE 873A-02
ISSUE A





DETAIL Y





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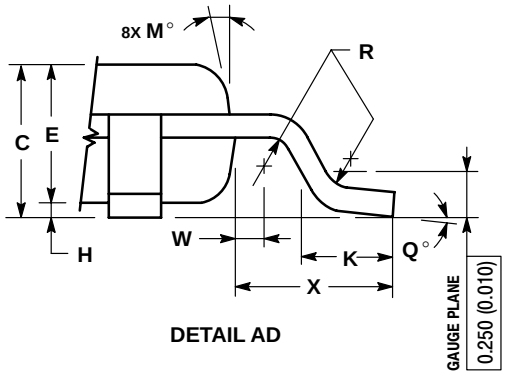

DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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