

MC100LVEP14

2.5V / 3.3V 1:5 Differential ECL/PECL/HSTL Clock Driver

The MC100LVEP14 is a low skew 1-to-5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended (if the V_{BB} output is used). HSTL inputs can be used when the LVEP14 is operating under PECL conditions.

The LVEP14 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into 50 Ω even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The common enable ($\overline{EN}$) is synchronous, outputs are enabled/disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

The MC100LVEP14, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVEP14 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single ended CLK input pin operation is limited to a $V_{CC} \geq 3.0$ V in PECL mode, or $V_{EE} \leq -3.0$ V in NECL mode. Designers can take advantage of the LVEP14's performance to distribute low skew clocks across the backplane or the board.

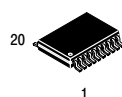
- 100 ps Device-to-Device Skew
- 25 ps Within Device Skew
- 400 ps Typical Propagation Delay
- Maximum Frequency > 2 GHz Typical
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode: $V_{CC} = 2.375$ V to 3.8 V with $V_{EE} = 0$ V
- NECL Mode: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.8 V
- LVDS Input Compatible
- Open Input Default State



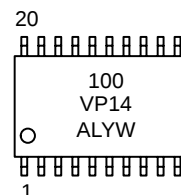
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MARKING DIAGRAM*



TSSOP-20
DT SUFFIX
CASE 948E



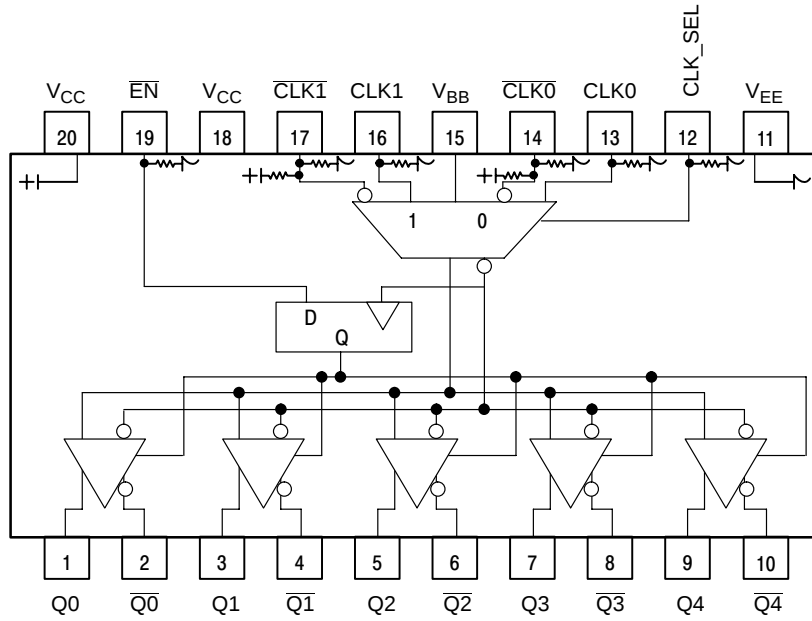
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEP14DT	TSSOP	75 Units/Rail
MC100LVEP14DTR2	TSSOP	2500 Tape & Reel

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Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View) and Logic Diagram

PIN DESCRIPTION

PINS	FUNCTION
CLK0*, $\overline{CLK0}$ **	ECL/PECL/HSTL CLK Input
CLK1*, $\overline{CLK1}$ **	ECL/PECL/HSTL CLK Input
Q0:4, $\overline{Q0}$:4	ECL/PECL Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
$\overline{EN}$ *	ECL Sync Enable
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default LOW when left open.

** Pins will default to $V_{CC}/2$ when left open.

FUNCTION TABLE

CLK0	CLK1	CLK_SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK0 or CLK1

ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 k Ω
Internal Input Pullup Resistor	37.5 k Ω
ESD Protection	Human Body Model Machine Model Charged Device Model
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating Oxygen Index	UL-94 code V-0 A 1/8" 28 to 34
Transistor Count	357 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

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MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		6	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		−6	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 −6	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			−40 to +85	°C
T _{stg}	Storage Temperature Range			−65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 TSSOP 20 TSSOP	140 100	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	std bd	20 TSSOP	23 to 41	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

100LVEP DC CHARACTERISTICS, PECL V_{CC} = 2.5 V, V_{EE} = 0 V (Note 3)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V _{OH}	Output HIGH Voltage (Note 4)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V _{OL}	Output LOW Voltage (Note 4)	555	680	805	555	680	805	555	680	805	mV
V _{IH}	Input HIGH Voltage (Single-Ended) (Note 5)	1335		1620	1335		1620	1275		1620	mV
V _{IL}	Input LOW Voltage (Single-Ended) (Note 5)	555		875	555		875	555		875	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	1.2		2.5	1.2		2.5	1.2		2.5	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current CLK CLK	0.5 −150			0.5 −150			0.5 −150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to −1.3 V.

4. All loading with 50 ohms to V_{CC}−2.0 volts.

5. Do not use V_{BB} at V_{CC} < 3.0 V.

6. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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100LVEP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 7)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 8)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 8)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Reference Voltage (Note 9)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 10)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

7. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925 V to -0.5 V.

8. All loading with 50 ohms to V_{CC} -2.0 volts.

9. Single ended input operation is limited to $V_{CC} \geq 3.0\text{ V}$ in PECL mode.

10. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100LVEP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.8\text{ V}$ to -2.375 V (Note 11)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	45	60	75	45	60	75	45	60	95	mA
V_{OH}	Output HIGH Voltage (Note 12)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 12)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{BB}	Output Reference Voltage (Note 13)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 14)	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

11. Input and output parameters vary 1:1 with V_{CC} .

12. All loading with 50 ohms to V_{CC} -2.0 volts.

13. Single ended input operation is limited to $V_{EE} \leq 3.0\text{ V}$ in NECL mode.

14. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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DC CHARACTERISTICS, HSTL $V_{CC} = 2.375 \text{ V to } 3.8 \text{ V}$, $V_{EE} = 0 \text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	1200			1200			1200			mV
V_{IL}	Input LOW Voltage			400			400			400	mV

AC CHARACTERISTICS $V_{CC} = 0 \text{ V}$, $V_{EE} = -2.375 \text{ V to } -3.8 \text{ V}$ or $V_{CC} = 2.375 \text{ V to } 3.8 \text{ V}$; $V_{EE} = 0 \text{ V}$ (Note 15)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max\text{LVPECL/HSTL}}$	Maximum Frequency (See Figure 2. $F_{\max}/\text{JITTER}$)		> 2			> 2			> 2		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output Differential	300	375	425	300	400	475	300	430	525	ps
t_{skew}	Within-Device Skew Device-to-Device Skew (Note 16)		10 100	25 125		15 150	25 175		15 200	25 225	ps
t_s t_h	Setup Time Hold Time	100 200	50 140		100 200	50 140		100 200	50 140		ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 2. $F_{\max}/\text{JITTER}$)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	125	165	225	125	180	250	125	200	275	ps

15. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to $V_{CC} - 2.0 \text{ V}$.

16. Skew is measured between outputs under identical transitions.

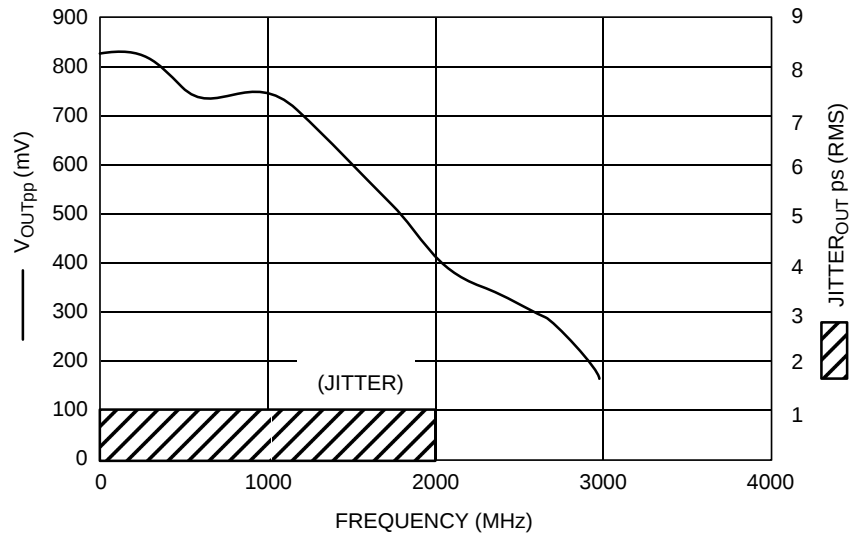


Figure 2. $F_{\max}/\text{Jitter}$

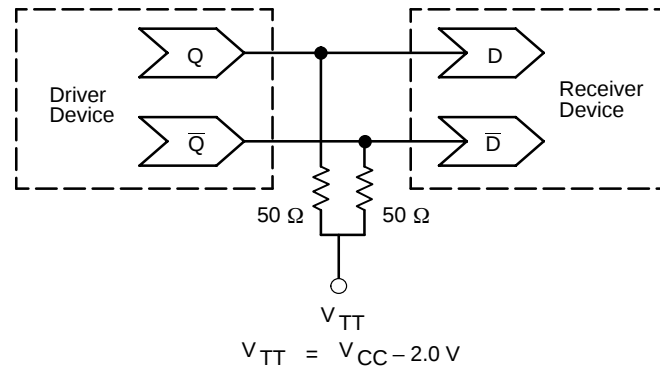


Figure 3. Typical Termination for Output Driver and Device Evaluation
 (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

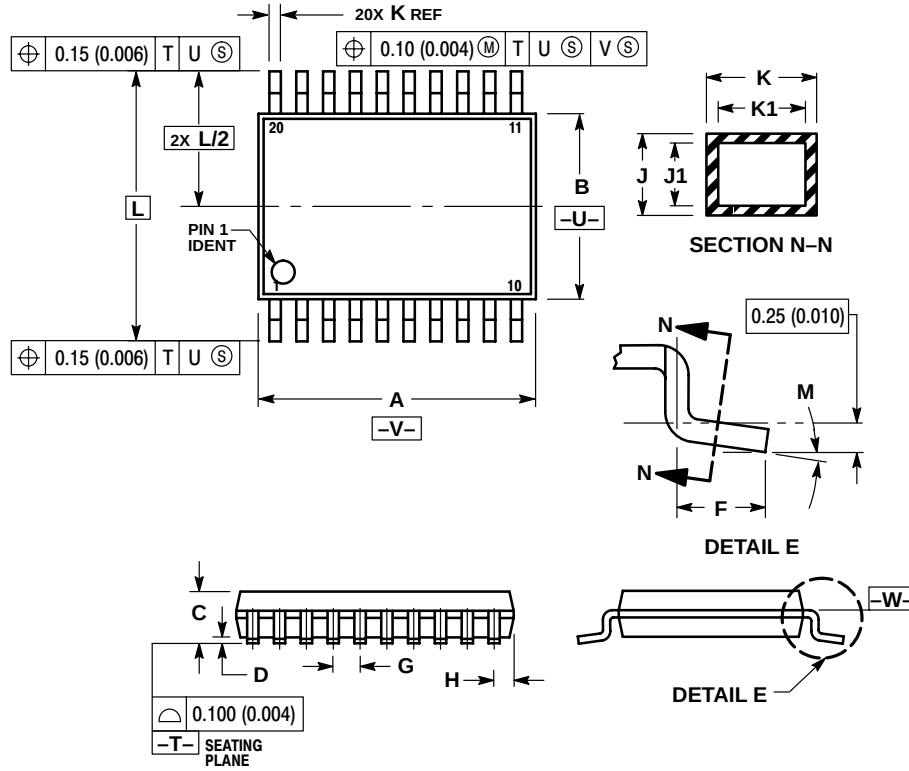
- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

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PACKAGE DIMENSIONS

TSSOP-20
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E-02
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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