

MC100LVEL91

3.3V / 5V Triple LVPECL / PECL Input to -3.3V ECL Output Translator

The MC100LVEL91 is a triple LVPECL / PECL input to ECL output translator. The device receives standard or low voltage differential PECL signals, determined by the V_{CC} supply level, and translates them to differential -3.3 V ECL output signals. (For translation to -5 V ECL output, see MC100EL91.)

To accomplish the level translation the LVEL91 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01 μ F capacitors.

Under open input conditions, the $\overline{D}$ input will be biased at $V_{CC}/2$ and the D input will be pulled to GND. This condition will force the Q output to a low, ensuring stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

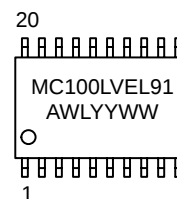
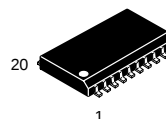
- 620 ps Typical Propagation Delay
- The 100 Series Contains Temperature Compensation
- Operating Range: V_{CC} = 3.0 V to 5.25 V;
 V_{EE} = -3.0 V to -3.8 V; GND= 0 V
- Q Output will Default LOW with Inputs Open or at GND



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MARKING DIAGRAM*



SO-20 DW SUFFIX CASE 751D

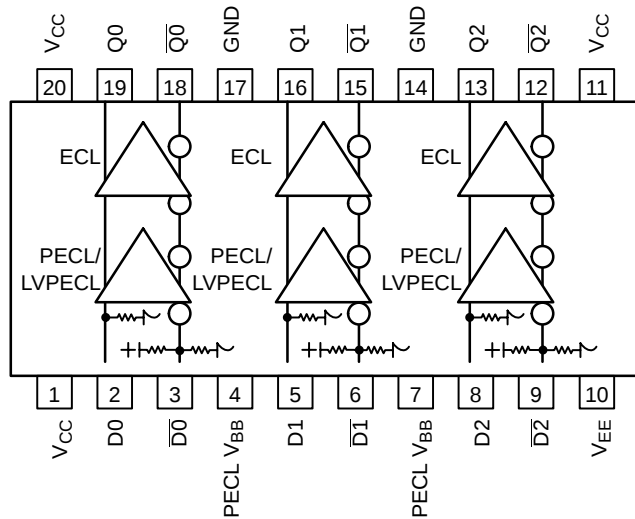
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note
AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL91DW	SO-20	38 Units/Rail
MC100LVEL91DWR2	SO-20	1000 Units/Reel

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PIN DESCRIPTION

PIN	FUNCTION
Dn, $\overline{Dn}$	PECL/LVPECL Inputs
Qn, $\overline{Qn}$	ECL Outputs
PECL V_{BB}	PECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

Figure 1. 20-Lead Pinout (Top View) and Logic Diagram

* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} , V_{EE} , and GND pins must be externally connected to Power Supply to guarantee proper operation.

ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 k Ω
Internal Input Pullup Resistor	75 k Ω
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 2 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in
Transistor Count	282 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Power Supply	GND = 0 V		8 to 0	V
V_{EE}	NECL Power Supply	GND = 0 V		-8 to 0	V
V_I	PECL Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	PECL V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	$^{\circ}\text{C/W}$ $^{\circ}\text{C/W}$
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	$^{\circ}\text{C/W}$
T_{sol}	Wave Solder	<2 to 3 sec @ 248 $^{\circ}\text{C}$		265	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which device damage may occur.

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LVPECL INPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $V_{EE} = -3.3\text{ V}$; GND = 0 V (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	V_{CC} Power Supply Current			11		6	11			11	mA
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
LVPECL V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4) $V_{pp} < 500\text{ mV}$ $V_{pp} \geq 500\text{ mV}$										
		1.0		2.9	0.9		2.9	0.9		2.9	V
		1.2		2.9	1.1		2.9	1.1		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	D	0.5		0.5			0.5			μA
		$\bar{D}$	-600		-600			-600			

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

3. Input parameters vary 1:1 with V_{CC} . V_{CC} can vary +0.5 / -0.3 V.

4. V_{IHCMR} min varies 1:1 with GND. V_{IHCMR} max varies 1:1 with V_{CC} .

PECL INPUT DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$; $V_{EE} = -3.3\text{ V}$; GND = 0 V (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	V_{CC} Power Supply Current			11		6	11			11	mA
V_{IH}	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
PECL V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6) $V_{pp} < 500\text{ mV}$ $V_{pp} \geq 500\text{ mV}$										V
		1.0		4.6	0.9		4.6	0.9		4.6	
		1.2		4.6	1.1		4.6	1.1		4.6	
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	D	0.5		0.5			0.5			μA
		$\bar{D}$	-600		-600			-600			

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

5. Input parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.25\text{ V}$.

6. V_{IHCMR} min varies 1:1 with GND. V_{IHCMR} max varies 1:1 with V_{CC} .

NECL OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V to }5.0\text{ V}$; $V_{EE} = -3.3\text{ V}$; GND = 0 V (Note 7)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	V_{EE} Power Supply Current			27		21	27			29	mA
V_{OH}	Output HIGH Voltage (Note 8)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 8)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

7. Output parameters vary 1:1 with GND. V_{EE} can vary +0.3 V / -0.5 V.

8. All loading with 50 ohm resistor to GND-2 volts.

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AC CHARACTERISTICS $V_{CC} = 3.0\text{ V to } 5.5\text{ V}$; $V_{EE} = -3.0\text{ V to } -3.8\text{ V}$; $GND = 0\text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
F _{max}	Maximum Toggle Frequency		600			600			600		MHz
t _{PLH} t _{PHL}	Propagation Delay D to Q Differential Select-Ended	490 440	590 590	690 740	520 470	620 620	720 770	560 510	660 660	760 810	ps
t _{SKEW}	Skew Output-to-Output (Note 9) Part-to-Part (Differential) (Note 9) Duty Cycle (Differential) (Note 10)		40 25	100 200		40 25	100 200		40 25	100 200	ps
V _{PP}	Input Swing (Note 11)	200		1000	200		1000	200		1000	mV
t _r t _f	Output Rise/Fall Times Q (20% – 80%)	320	400	580	320	400	580	320	400	580	ps

9. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.

10. Duty cycle skew is the difference between a T_{PLH} and T_{PHL} propagation delay through a device.

11. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40.

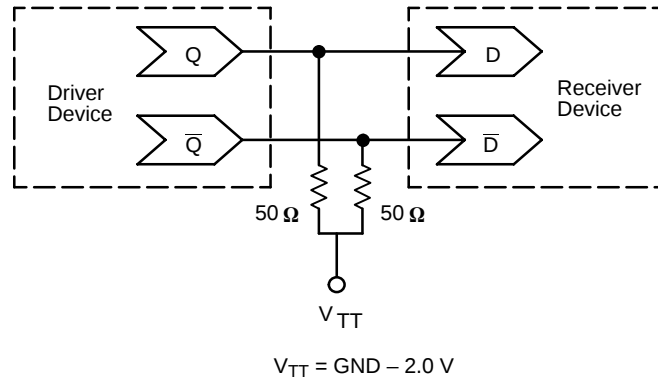


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

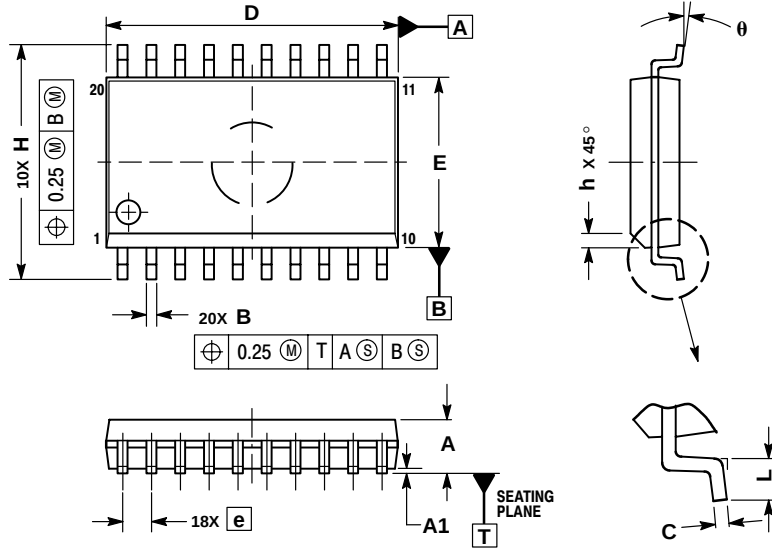
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

MC100LVEL91

PACKAGE DIMENSIONS

SO-20
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-05
ISSUE F



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

Notes

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