

MC100LVEL37

3.3V ECL 1:4 ÷1/÷2 Clock Fanout Buffer

The MC100LVEL37 is a fully differential 1:4 fanout buffer. The device offers two outputs at ± 1 of the input frequency, and two outputs at ± 2 of the input frequency. The Low Output–Output Skew of the device makes it ideal for distributing 1x and 1/2x frequency synchronous signals.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the CLK_n input will pull down to V_{EE} , The $\overline{\text{CLK}}_n$ input will bias around $V_{CC}/2$ and the Q_n output will go LOW.

- 700 ps Typical Propagation Delays
- 50 ps Maximum Output–Output Skews
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC} = 3.0 \text{ V}$ to 3.8 V with $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0 \text{ V}$ with $V_{EE} = -3.0 \text{ V}$ to -3.8 V
- Internal Input Pulldown Resistors
- Q_n Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 256 devices



ON Semiconductor™

<http://onsemi.com>

MARKING DIAGRAM*



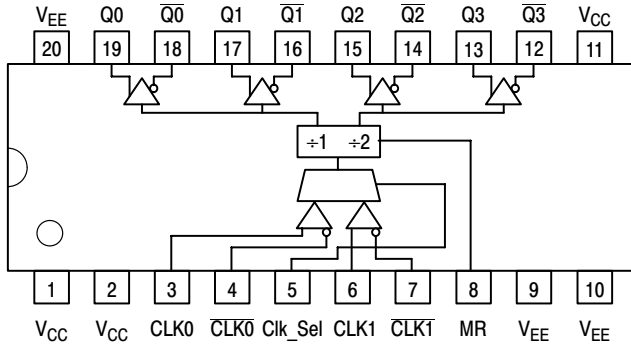
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL37DW	SO–20	38 Units/Rail
MC100LVEL37DWR2	SO–20	1000 Units/Reel

MC100LVEL37



20-Lead Pinout (Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

TRUTH TABLE

Clk_Sel	MR	Q0, 1	Q2, 3
L	L	CLK0/+1	CLK0/+2
H	L	CLK1/+1	CLK1/+2
X	H	L	L

X = Don't Care

PIN DESCRIPTION

PIN	FUNCTION
Q0, $\overline{Q0}$; Q1, $\overline{Q1}$	ECL Differential Clock +1 Outputs
Q2, $\overline{Q2}$; Q3, $\overline{Q3}$	ECL Differential Clock +2 Outputs
CLKn, $\overline{CLKn}$	ECL Differential Clock Inputs
Clk_Sel	ECL Input Clock Selection
MR	ECL Asynchronous Master Reset
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8 to 0	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 -6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	140 100	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

MC100LVEL37

LVPECL DC CHARACTERISTICS $V_{CC}=3.3\text{ V}$; $V_{EE}=0.0\text{ V}$ (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		38	50		38	55		38	55	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)										
		$V_{pp} < 500\text{ mV}$		2.9	1.2		2.9	1.2		2.9	V
		$V_{pp} \geq 500\text{ mV}$		2.9	1.4		2.9	1.4		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	$\overline{\text{CLKn}}$ $\overline{\text{CLKn}}$	0.5 -300		0.5 -300			0.5 -300			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}-2\text{ volts}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1 V.

LVNECL DC CHARACTERISTICS $V_{CC}=0.0\text{ V}$; $V_{EE}=-3.3\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		38	50		38	55		38	55	mA
V_{OH}	Output HIGH Voltage (Note 2.)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 2.)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)										
		$V_{pp} < 500\text{ mV}$	-2.0	-0.4	-2.1		-0.4	-2.1		-0.4	V
		$V_{pp} \geq 500\text{ mV}$	-1.8	-0.4	-1.9		-0.4	-1.9		-0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	$\overline{\text{CLKn}}$ $\overline{\text{CLKn}}$	0.5 -300		0.5 -300			0.5 -300			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}-2\text{ volts}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1 V.

MC100LVEL37

AC CHARACTERISTICS $V_{CC}= 3.3\text{ V}$; $V_{EE}= 0.0\text{ V}$ or $V_{CC}= 0.0\text{ V}$; $V_{EE}= -3.3\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to $Q/\bar{Q}$ (Diff) CLK to $Q/\bar{Q}$ MR to Q	640 620 640		940 920 920	680 680 680	700 700 700	920 940 920	720 720 720		980 970 980	ps
t_{SKEW}	Within-Device Skew (Note 2.) Duty Cycle Skew (Diff) (Note 3.)			50 50			50 50			50 50	ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 4.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

1. V_{EE} can vary $\pm 0.3\text{ V}$.
2. Within-device skew defined as identical transitions on similar paths through a device.
3. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
4. $V_{\text{PP}}(\text{min})$ is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈ 40 .

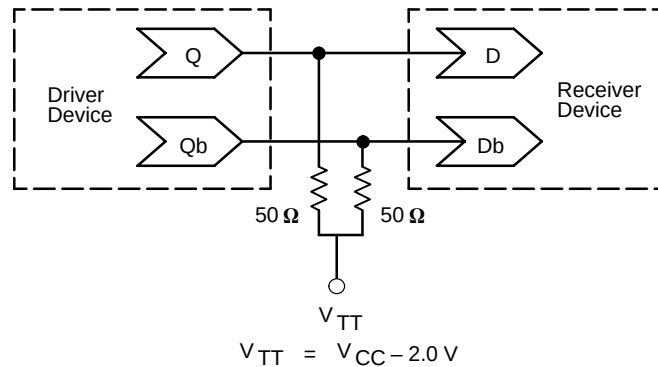


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

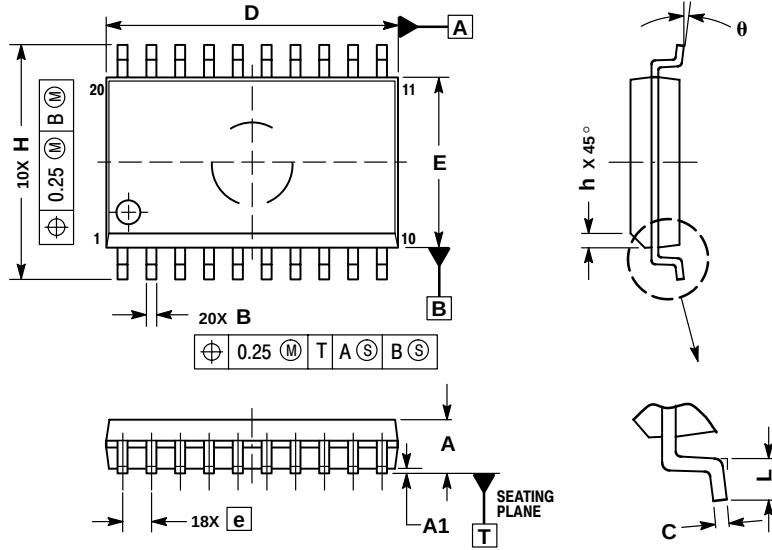
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

MC100LVEL37

PACKAGE DIMENSIONS

SO-20
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-05
ISSUE F



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

Notes

Notes

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)
Email: ONlit-german@hibbertco.com

French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)
Email: ONlit-french@hibbertco.com

English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)

Email: ONlit-spanish@hibbertco.com

Toll-Free from Mexico: Dial 01-800-288-2872 for Access –
then Dial 866-297-9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)

Toll Free from Hong Kong & Singapore:

001-800-4422-3781

Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031

Phone: 81-3-5740-2700

Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local
Sales Representative.