3.3V ECL Differential Receiver

The MC100LVEL16 is a differential receiver. The device is functionally equivalent to the EL16 device, operating from a 3.3 V supply. The LVEL16 exhibits a wider V_{IHCMR} range than its EL16 counterpart. With output transition times and propagation delays comparable to the EL16 the LVEL16 is ideally suited for interfacing with high frequency sources at 3.3 V supplies.

Under open input conditions, the Q input will be pulled down to V_{EE} and the \overline{Q} input will be biased to $V_{CC}/2$. This condition will force the Q output low.

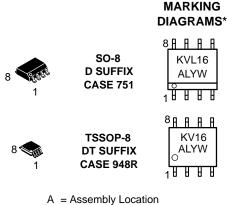
The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 300 ps Propagation Delay
- High Bandwidth Output Transitions
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC} = 3.0$ V to 3.8 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -3.0 V to -3.8 V
- Internal Input Pulldown Resistors on D, Pullup and Pulldown Resistors on D
- Q Output will Default LOW with Inputs Open or at VEE



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A = Assembly Location L = Wafer Lot Y = Year W = Work Week

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping [†]						
MC100LVEL16D	SO-8	98 Units / Rail						
MC100LVEL16DR2	SO-8	2500 Tape & Reel						
MC100LVEL16DT	TSSOP-8	98 Units / Rail						
MC100LVEL16DTR2	TSSOP-8	2500 Tape & Reel						

NC 1 $\overline{)}$ 8 V_{CC} D 2 $\overline{)}$ 7 Q \overline{D} 3 $\overline{)}$ 6 \overline{Q} V_{BB} 4 5 V_{EE}

Figure 1. Logic Diagram and Pinout Assignment

†For additional tape and reel information, refer to Brochure BRD8011/D.

PIN DESCRIPTION

PIN	FUNCTION
D, D	ECL Data Inputs
Q, <u>Q</u>	ECL Data Outputs
V _{BB}	Reference Voltage Output
V _{CC}	Positive Supply
V _{EE}	Negative Supply
NC	No Connect

ATTRIBUTES

Characterist	Value	
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 4 KV > 400 V > 2 kV
Moisture Sensitivity (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		79
Meets or Exceeds JEDEC Spec EIA/J	IESD78 IC Latchup Test	

1. Refer to Application Note AND8003/D for additional information.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0 V$		-8 to 0	V
VI	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	$\begin{array}{c} V_{I} \leq V_{CC} \\ V_{I} \geq V_{EE} \end{array}$	6 to 0 -6 to 0	V V
l _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	SO-8 SO-8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SO-8	41 to 44 \pm 5%	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 \pm 5%	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

Unit

mΑ

mV

mV

mV

mV V

V

V

μΑ

μΑ

μA

150

LVPECL	LVPECL DC CHARACTERISTICS V _{CC} = 3.3 V; V _{EE} = 0.0 V (Note 3)										
		-40 °C 25°C			85°C						
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
I _{EE}	Power Supply Current		17	23		17	23		18	24	
V _{OH}	Output HIGH Voltage (Note 4)	2215	2295	2420	2275	2345	2420	2275	2345	2420	
V _{OL}	Output LOW Voltage (Note 4)	1470	1605	1745	1490	1595	1680	1490	1595	1680	
V _{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	
V _{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	
VIHCMR	Input HIGH Voltage Common Mode Range (Differential) (Note 5)										
	Vpp < 500 mV	1.2		2.9	1.1		2.9	1.1		2.9	
	Vpp ≧ 500 mV	1.5		2.9	1.4		2.9	1.4		2.9	
	I designed and the second s										

L

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

150

0.5

-600

150

0.5

-600

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ± 0.3 V. 4. Outputs are terminated through a 50 Ω resistor to V_{CC} - 2 V.

D

D

0.5

-600

Input HIGH Current

Input LOW Current

Iн

Ι_{ΙL}

VIHCMR min varies 1:1 with VEE, max varies 1:1 with VCC. The VIHCMR range is referenced to the most positive side of the differential input signal. 5. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between VPPmin and 1 V.

		-40 °C			25°C						
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		17	23		17	23		18	24	mA
V _{OH}	Output HIGH Voltage (Note 7)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V _{OL}	Output LOW Voltage (Note 7)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
VIH	Input HIGH Voltage (Single-Ended)	-1 165		-880	-1 165		-880	-1 165		-880	mV
V _{IL}	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 8) Vpp < 500 mV Vpp ≧ 500 mV	-2.1 -1.8		-0.4 -0.4	-2.2 -1.9		-0.4 -0.4	-2.2 -1.9		-0.4 -0.4	v v
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current D D	0.5 -600			0.5 -600			0.5 -600			μΑ μΑ

LVNECL DC CHARACTERISTICS V_{CC} = 0.0 V; V_{EE} = -3.3 V (Note 6)

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The 6. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.

7. Outputs are terminated through a 50 Ω resistor to V_{CC} - 2 V. 8. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between VPPmin and 1 V.

			-40 °C		25°C						
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{max}	Maximum Toggle Frequency		1.75			1.75			1.75		GHz
t _{PLH} t _{PHL}	Propagation Delay to Output Differential Single-Ended	150 100	275 275	400 450	225 175	300 300	375 425	240 190	315 315	390 440	ps
t _{SKEW}	Duty Cycle Skew (Differential) (Note 10)		5	30		5	20		5	20	ps
t _{JITTER}	Random Clock Jitter (RMS)		0.7			0.7			0.7		ps
V _{PP}	Input Swing (Note 11)	150		1000	150		1000	150		1000	mV
t _r t _f	Output Rise/Fall Times Q (20% - 80%)	120	220	320	120	220	320	120	220	320	ps

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= -3.3 V (Note 9)

9. V_{EE} can vary ±0.3 V.
 10. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
 11. V_{PP(}min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

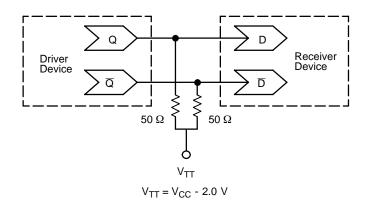


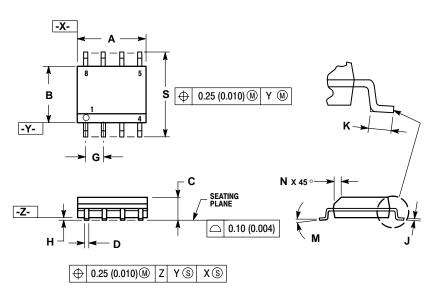
Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 - Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	-	ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
AN1405	-	ECL Clock Distribution Techniques
AN1406	-	Designing with PECL (ECL at +5.0 V)
AN1503	-	ECLinPS I/O SPICE Modeling Kit
AN1504	-	Metastability and the ECLinPS Family
AN1560	-	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	-	Interfacing Between LVDS and ECL
AN1596	-	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	-	Using Wire-OR Ties in ECLinPS Designs
AN1672	-	The ECL Translator Guide
AND8001	-	Odd Number Counters Design
AND8002	-	Marking and Date Codes
AND8020	-	Termination of ECL Logic Devices
AND8090	-	AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 **ISSUE AA**



NOTES:

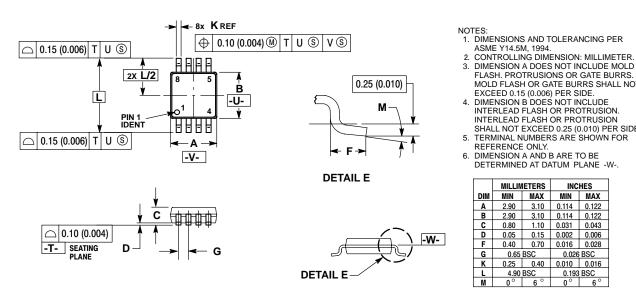
- VOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE

- A. MAXIMUM MOLD PROTRUSION 0.15 (0.000) FEM SIDE.
 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D UMENSION AT MAXIMUM MATERIAL CONDITION.
 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.197	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.053	0.069	
D	0.33	0.51	0.013	0.020	
G	1.27	7 BSC	0.050 BSC		
н	0.10	0.25	0.004	0.010	
J	0.19	0.25	0.007	0.010	
K	0.40	1.27	0.016	0.050	
М	0 °	8 °	0 °	8 °	
Ν	0.25	0.50	0.010	0.020	
S	5.80	6.20	0.228	0.244	

PACKAGE DIMENSIONS

TSSOP-8 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948R-02 ISSUE A



REFERENCE ONLY. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-. INCHES MILLIMETERS DIM MIN MAX MIN MAX 2.90 3.10 0.114 0.122 А в 2.90 3.10 0.114 0.122 1.10 0.031 0.043 С 0.80 D 0.15 0.002 0.006 0.05 F 0.40 0.70 0.016 0.028 0.65 BSC G 0.026 BSC 0.25 0.40 0.010 0.016 4.90 BSC 0.193 BSC

6

0

0

6

DIMENSIONS AND TOLERANCING PER

CONTROLLING DIMENSION: MILLIMETER.

MOLD FLASH OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.

SHALL NOT EXCEED 0.25 (0.010) PER SIDE. TERMINAL NUMBERS ARE SHOWN FOR

INTERLEAD FLASH OR PROTRUSION

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