

# MC100LVEL13

## 3.3V ECL Dual 1:3 Fanout Buffer

The MC100LVEL13 is a dual, fully differential 1:3 fanout buffer. The Low Output–Output Skew of the device makes it ideal for distributing two different frequency synchronous signals.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to  $V_{EE}$ , The  $\bar{D}$  input will bias around  $V_{CC}/2$  and the Q output will go LOW.

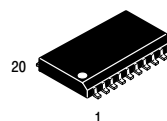
- 500 ps Typical Propagation Delays
- 50 ps Output–Output Skews
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC}$ = 3.0 V to 3.8 V with  $V_{EE}$  = 0 V
- NECL Mode Operating Range:  $V_{CC}$ = 0 V with  $V_{EE}$  = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at  $V_{EE}$
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",  
Oxygen Index 28 to 34
- Transistor Count = 143 devices



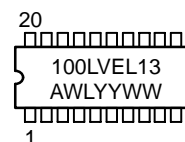
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### MARKING DIAGRAM



SO–20  
DW SUFFIX  
CASE 751D



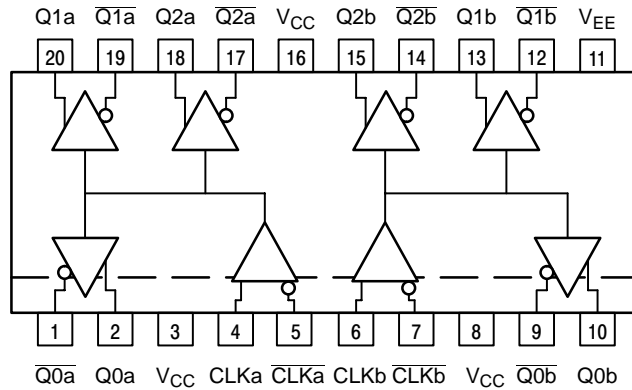
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL13DW	SOIC–20	38 Units/Rail
MC100LVEL13DWR2	SOIC–20	1000 Units/Reel

# MC100LVEL13

## Logic Diagram and Pinout: 20-Lead SOIC (Top View)



Warning: All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

### PIN DESCRIPTION

PIN	FUNCTION
Qna, Qna	ECL Differential Clock Outputs
Qnb, Qnb	ECL Differential Clock Outputs
CLKn, CLKn	ECL Differential Clock Inputs
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply

### MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8 to 0	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		–8 to 0	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 to 0 –6 to 0	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			–65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

# MC100LEVEL13

## LVPECL DC CHARACTERISTICS $V_{CC}=3.3\text{ V}$ ; $V_{EE}=0.0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		30	38		30	38		32	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) $V_{pp} < 500\text{ mV}$ $V_{pp} \geq 500\text{ mV}$										
		1.3		2.9	1.2		2.9	1.2		2.9	V
		1.5		2.9	1.4		2.9	1.4		2.9	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current $\overline{\text{CLKn}}$ $\overline{\text{CLKn}}$	0.5			0.5			0.5			$\mu\text{A}$
		-300			-300			-300			$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}-2\text{ volts}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

## LVNECL DC CHARACTERISTICS $V_{CC}=0.0\text{ V}$ ; $V_{EE}=-3.3\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		30	38		30	38		32	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) $V_{pp} < 500\text{ mV}$ $V_{pp} \geq 500\text{ mV}$										
		-2.0		-0.4	-2.1		-0.4	-2.1		-0.4	V
		-1.8		-0.4	-1.9		-0.4	-1.9		-0.4	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current $\overline{\text{CLKn}}$ $\overline{\text{CLKn}}$	0.5			0.5			0.5			$\mu\text{A}$
		-300			-300			-300			$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

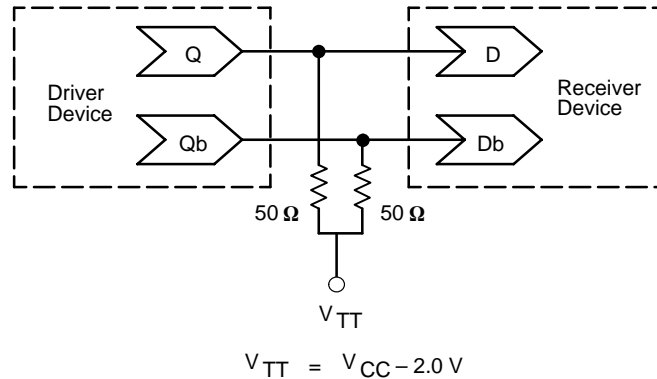
1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}-2\text{ volts}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

# MC100LVEL13

**AC CHARACTERISTICS**  $V_{CC}= 3.3\text{ V}$ ;  $V_{EE}= 0.0\text{ V}$  or  $V_{CC}= 0.0\text{ V}$ ;  $V_{EE}= -3.3\text{ V}$  (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay CLK to Q/ $\bar{Q}$	410		600	430	500	620	450		640	ps
$t_{sk(O)}$	Output–Output Skew Any Qa to Qa, Any Qb to Qb Any Qa to Any Qb			50 75			50 75			50 75	ps
$t_{skew}$	Duty Cycle Skew $ t_{PLH}-t_{PHL} $			50			50			50	ps
$t_{JITTER}$	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
$V_{PP}$	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
$t_r$ $t_f$	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	ps

- $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
- $V_{PP}(\min)$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .



**Figure 1. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

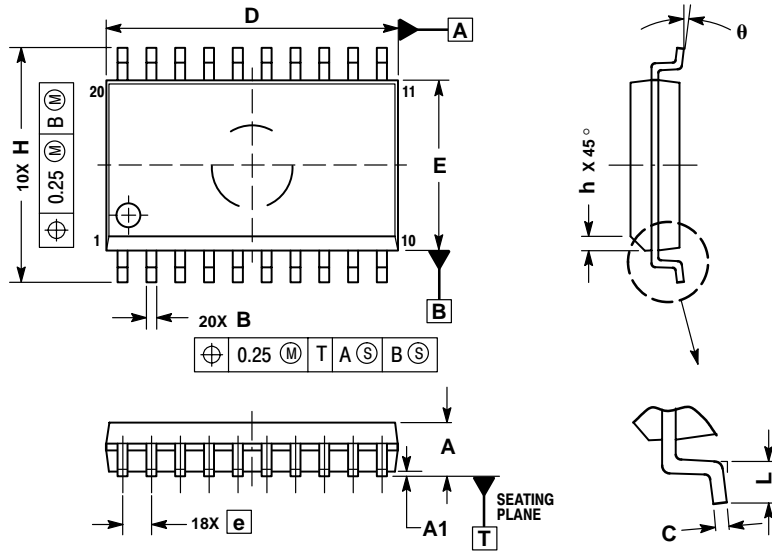
## Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non–Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire–OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

# MC100LVEL13

## PACKAGE DIMENSIONS

### SO-20 DW SUFFIX PLASTIC SOIC PACKAGE CASE 751D-05 ISSUE F



#### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

## **Notes**

## **Notes**

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