

MC100EPT24

3.3V LVTTL/LVCMOS to Differential LVECL Translator

The MC100EPT24 is a LVTTL/LVCMOS to differential LVECL translator. Because LVECL levels and LVTTL/LVCMOS levels are used, a -3.3 V , $+3.3\text{ V}$ and ground are required. The small outline 8-lead package and the single gate of the EPT24 makes it ideal for those applications where space, performance, and low power are at a premium.

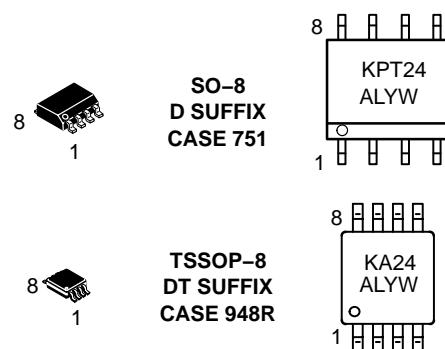
- 350 ps Typical Propagation Delay
- Maximum Input Clock Frequency > 1.0 GHz Typical
- The 100 Series Contains Temperature Compensation
- Operating Range: $V_{CC} = 3.0\text{ V}$ to 3.6 V ;
 $V_{EE} = -3.6\text{ V}$ to -3.0 V ; $GND = 0\text{ V}$
- PNP LVTTL Input for Minimal Loading
- Q Output will Default HIGH with Input Open



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note
AND8002/D

ORDERING INFORMATION

Device	Package	Shipping†
MC100EPT24D	SO-8	98 Units / Rail
MC100EPT24DR2	SO-8	2500 Tape & Reel
MC100EPT24DT	TSSOP-8	100 Units / Rail
MC100EPT24DTR2	TSSOP-8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC100EPT24

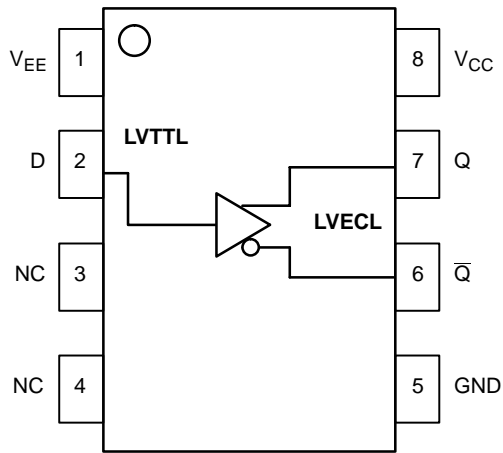


Table 1. PIN DESCRIPTION

PIN	FUNCTION
Q, \bar{Q}	Differential LVECL Outputs
D	LVTTL Input
V _{CC}	Positive Supply
GND	Ground
V _{EE}	Negative Supply
NC	No Connect

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection	Human Body Model Machine Model Charged Device Model
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) Flammability Rating Oxygen Index	Level 1 UL-94 code V-0 @ 1.25 in 28 to 34
Transistor Count	181 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	Positive Power Supply	GND = 0 V	V _{EE} = -3.3 V	3.8	V
V _{EE}	Negative Power Supply	GND = 0 V	V _{CC} = +3.3 V	-3.8	V
V _{IN}	Input Voltage	GND = 0 V	V _I ≤ V _{CC}	0 to V _{CC}	V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	8 SOIC	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	8 TSSOP	41 to 44	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

MC100EPT24

Table 4. LVTTTL INPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$, $V_{EE} = -3.6\text{ V}$ to -3.0 V , $GND = 0.0\text{ V}$; $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	$V_{IN} = 2.7\text{ V}$			20	μA
I_{IHH}	Input HIGH Current HIGH Voltage	$V_{CC} = V_{IN} = 3.8\text{ V}$			100	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.5\text{ V}$			-0.6	mA
V_{IK}	Input Clamp Diode Voltage	$I_{IN} = -18\text{ mA}$			-1.2	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

Table 5. NECL OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$, $V_{EE} = -3.3\text{ V}$, $GND = 0.0\text{ V}$ (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (Note 4)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1030	-895	mV
V_{OL}	Output LOW Voltage (Note 4)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
I_{CC}	Positive Power Supply Current		2.0	4.0		2.0	4.0		2.0	4.0	mA
I_{EE}	Negative Power Supply Current	20	30	38	20	30	38	20	30	38	mA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

3. Output levels will vary 1:1 with GND. V_{EE} can vary $\pm 0.3\text{ V}$.

4. Outputs are terminated through a $50\ \Omega$ resistor to GND-2 volts.

Table 6. AC CHARACTERISTICS $V_{CC} = 3.0\text{ V}$ to 3.6 V , $V_{EE} = -3.6\text{ V}$ to -3.0 V , $GND = 0.0\text{ V}$ (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Input Clock Frequency (See Figure 2)		> 1			> 1			> 1		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential (Note 6)	300	500	800	300	530	800	300	560	800	ps
t_{JITTER}	RMS Random Clock Jitter (See Figure 2)		0.2	< 1		0.2	< 1		0.2	< 1	ps
t_r , t_f	Output Rise/Fall Times Q, \bar{Q} (20% – 80%) @ 50 MHz	70	125	170	80	130	180	100	150	200	ps

NOTE: Devices are designed to meet the AC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

5. Measured using a LVTTTL source, 50% duty cycle clock source. All loading with $50\ \Omega$ to GND-2.0 V.

6. Specifications for standard TTL input signal.

MC100EPT24

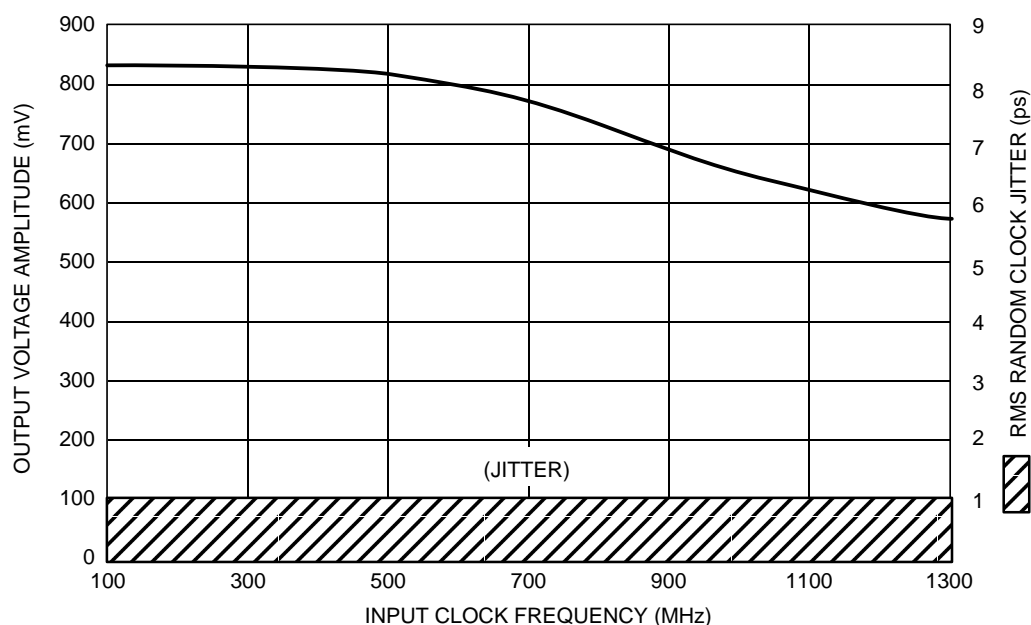


Figure 2. Output Voltage Amplitude (V_{OUTpp})/RMS Jitter vs. Input Clock Frequency at Ambient Temperature

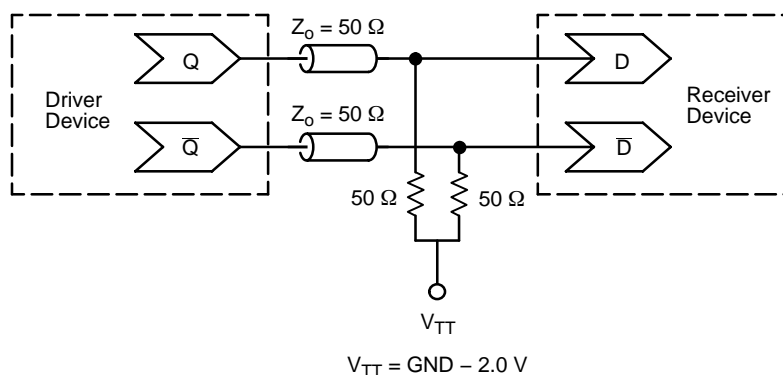


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

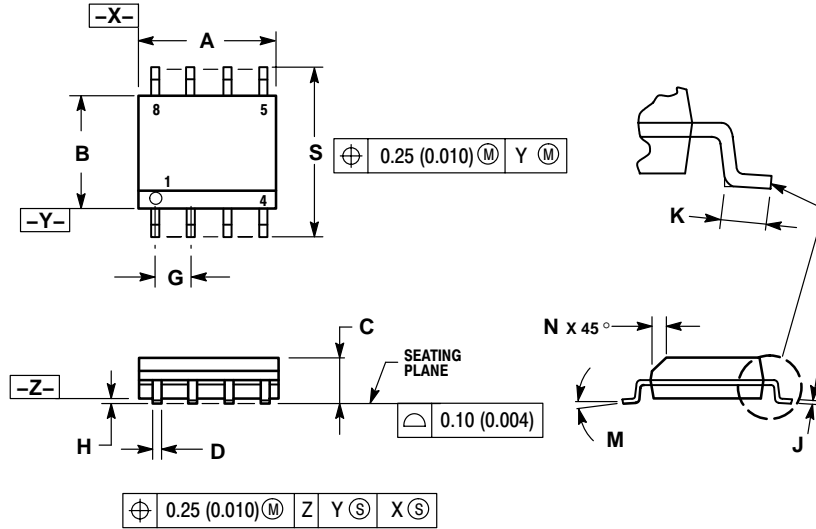
- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

MC100EPT24

PACKAGE DIMENSIONS

SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE AA

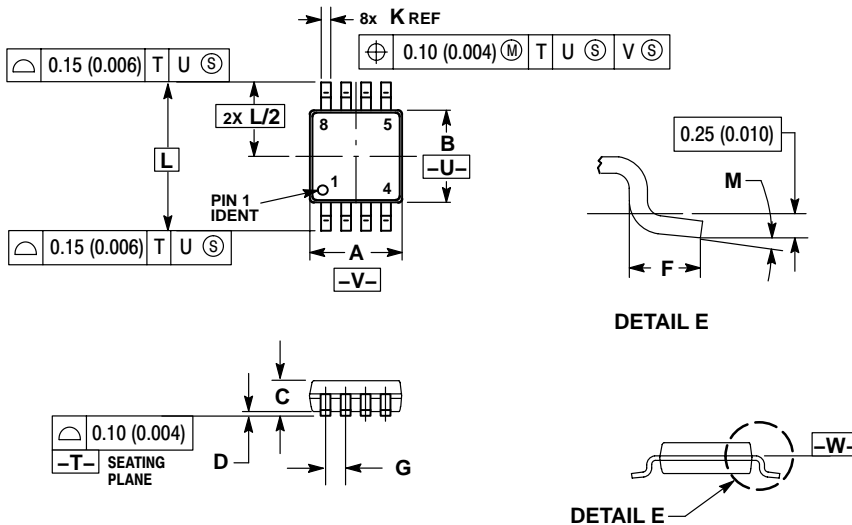


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

TSSOP-8 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948R-02 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.