

MC100EPT21

3.3V Differential LVPECL to LVTTTL Translator

The MC100EPT21 is a Differential LVPECL to LVTTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The small outline 8-lead SOIC package makes the EPT21 ideal for applications which require the translation of a clock or data signal.

The V_{BB} output allows this EPT21 to be cap coupled in either single-ended or differential input mode. When single-ended cap coupled, V_{BB} output is tied to the \overline{D} input and D is driven for a non-inverting buffer, or V_{BB} output is tied to the D input and \overline{D} is driven for an inverting buffer. When cap coupled differentially, V_{BB} output is connected through a resistor to each input pin. If used, the V_{BB} pin should be bypassed to V_{CC} via a 0.01 μ F capacitor. For additional information see AND8020. For a single-ended direct connection use an external voltage reference source such as a resistor divider. Do not use V_{BB} for a single-ended direct connection or port to another device.

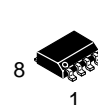
- 1.4 ns Typical Propagation Delay
- Maximum Frequency > 275 MHz Typical
- 24 mA TTL outputs
- Operating Range: $V_{CC} = 3.0$ V to 3.6 V with GND = 0 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at GND
- The 100 Series Contains Temperature Compensation
- V_{BB} Output
- New Differential Input Common Mode Range



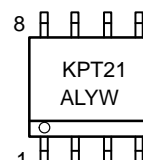
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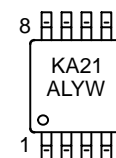
MARKING DIAGRAMS*



SO-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

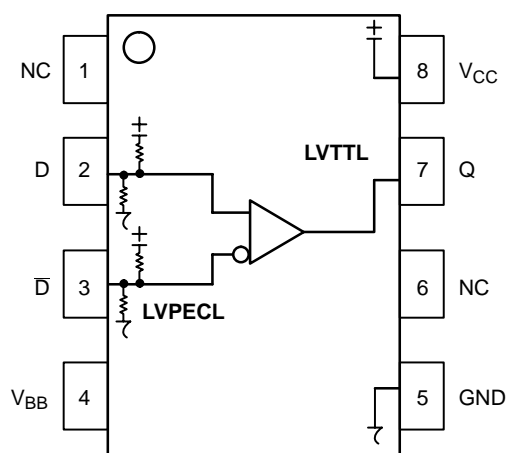
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping†
MC100EPT21D	SO-8	98 Units/Rail
MC100EPT21DR2	SO-8	2500 Tape & Reel
MC100EPT21DT	TSSOP-8	100 Units/Rail
MC100EPT21DTR2	TSSOP-8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC100EPT21



PIN DESCRIPTION

PIN	FUNCTION
Q	LVTTTL Output
D**, \bar{D} **	Differential LVPECL Input Pair
V _{CC}	Positive Supply
V _{BB}	Output Reference Voltage
GND	Ground
NC	No Connect

** Pins will default to V_{CC}/2 when left open.

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	50 k Ω
Internal Input Pullup Resistor	50 k Ω
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 1.5 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34
	UL 94 V-0 @ 0.125 in
Transistor Count	81 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Power Supply	GND = 0 V		3.8	V
V _{IN}	PECL Input Voltage	GND = 0 V	V _I ≤ V _{CC}	0 to 3.8	V
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			−40 to +85	°C
T _{stg}	Storage Temperature Range			−65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 SOIC	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 TSSOP	41 to 44	°C/W
T _{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

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PECL INPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$, $GND = 0.0\text{ V}$ (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current $\begin{smallmatrix} D \\ \overline{D} \end{smallmatrix}$	-150		0.5	-150		0.5	-150		0.5	μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

3. Input parameters vary 1:1 with V_{CC} .

4. V_{IHCMR} min varies 1:1 with GND , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

TTL OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$, $GND = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.0\text{ mA}$	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 24\text{ mA}$			0.5	V
I_{CCH}	Power Supply Current	Outputs set to HIGH	5	12	20	mA
I_{CCL}	Power Supply Current	Outputs set to LOW	8	18	26	mA
I_{OS}	Output Short Circuit Current		-130		-80	mA

AC CHARACTERISTICS $V_{CC} = 3.0\text{ V}$ to 3.6 V , $GND = 0.0\text{ V}$ (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 2. $F_{max}/JITTER$)	275	350		275	350		275	350		MHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential	1200 1200	1450 1400	1800 1800	1200 1200	1450 1400	1800 1800	1300 1200	1450 1400	1900 1900	ps
t_{SKPP}	Part-to-Part Skew (Note 6)			500			500			500	ps
t_{JITTER}	Random Clock Jitter (RMS) (See Figure 2 $F_{max}/JITTER$)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
t_r , t_f	Output Rise/Fall Times (0.8V – 2.0V) Q, \overline{Q}	330	500	900	330	500	900	330	500	900	ps

5. Measured with a 750 mV 50% duty-cycle clock source. $R_L = 500\ \Omega$ to GND and $C_L = 20\text{ pF}$ to GND . Refer to Figure 3.

6. Skews are measured between outputs under identical transitions.

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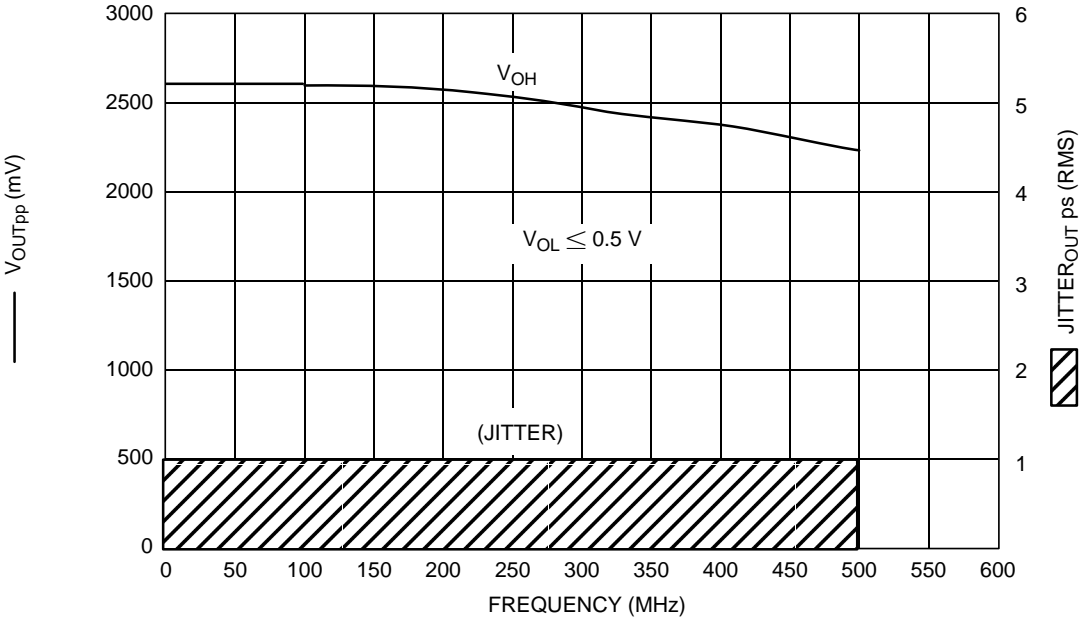


Figure 2. F_{max} /Jitter

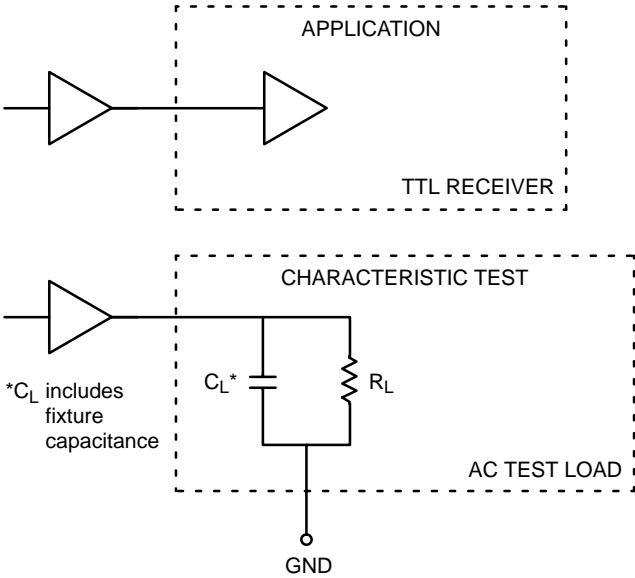


Figure 3. TTL Output Loading Used For Device Evaluation

Resource Reference of Application Notes

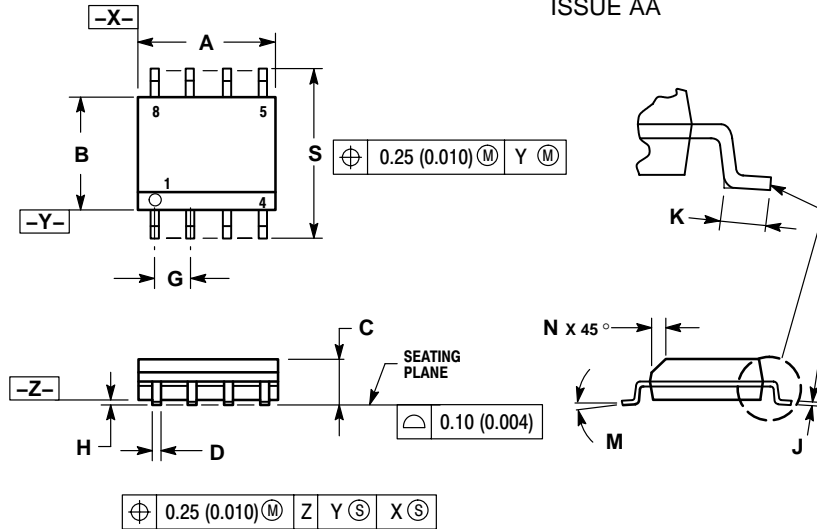
- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

MC100EPT21

PACKAGE DIMENSIONS

SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

NOTES:

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