

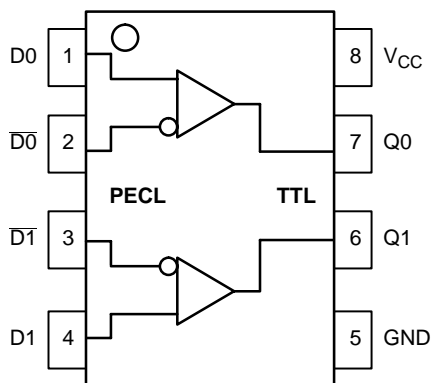
# MC100ELT23

## 5 V Dual Differential PECL to TTL Translator

The MC100ELT23 is a dual differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the dual gate design of the ELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The PECL inputs are differential; therefore, the MC100ELT23 can accept any standard differential PECL input referenced from a  $V_{CC}$  of 5.0 V.

- 3.5 ns Typical Propagation Delay
- 24 mA TTL Outputs
- Flow Through Pinouts
- The 100 Series Contains Temperature Compensation
- Operating Range  $V_{CC} = 4.75$  V to 5.25 V with GND = 0 V
- Internal Input 50 K $\Omega$  Pulldown Resistors
- Q Output Will Default LOW with Inputs Left Open or < 1.3 V



**Figure 1. 8-Lead Pinout and Logic Diagram**  
(Top View)



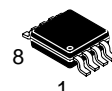
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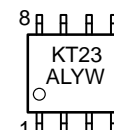
### MARKING DIAGRAMS\*



**SOIC-8  
D SUFFIX  
CASE 751**



**TSSOP-8  
DT SUFFIX  
CASE 948R**



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*For additional marking information, refer to Application Note AND8002/D.

### PIN DESCRIPTION

PIN	FUNCTION
Qn Dn, $\overline{Dn}$ $V_{CC}$ GND	TTL Outputs PECL Differential Inputs Positive Supply Ground

### ORDERING INFORMATION

Device	Package	Shipping†
MC100ELT23D	SOIC-8	98 Units / Rail
MC100ELT23DR2	SOIC-8	2500 Tape & Reel
MC100ELT23DT	TSSOP-8	98 Units / Rail
MC100ELT23DTR2	TSSOP-8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MC100ELT23

## ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	50 k $\Omega$
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model	> 2 kV > 400 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	91
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

## MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Power Supply	GND = 0 V		7	V
V <sub>I</sub>	Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	0 to 6	V
T <sub>A</sub>	Operating Temperature Range			−40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			−65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm	SOIC-8	190	°C/W
		500 lfpm	SOIC-8	130	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	°C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm	TSSOP-8	185	°C/W
		500 lfpm	TSSOP-8	140	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ± 5%	°C/W
T <sub>sol</sub>	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected. Functional operation should be restricted to the Recommended Operating Conditions.

## PECL INPUT DC CHARACTERISTICS V<sub>CC</sub> = 5.0 V; GND = 0.0 V (Note 2)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended) (Note 4)	3835		4120	3835		4120	3835		4120	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.2		5.0	2.2		5.0	2.2		5.0	V
I <sub>IH</sub>	Input HIGH Current			255			175			175	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input parameters vary 1:1 with V<sub>CC</sub>. V<sub>CC</sub> can vary ± 0.25 V.
- V<sub>IHCMR</sub> min varies 1:1 with GND, V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>.
- TTL output R<sub>L</sub> = 500  $\Omega$  to GND.

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## TTL OUTPUT DC CHARACTERISTICS $V_{CC} = 4.75V$ to $5.25V$ ; $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.0$ mA	2.4		(Note 5)	V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA			0.5	V
$I_{CCH}$	Power Supply Current			23	33	mA
$I_{CCL}$	Power Supply Current			26	36	mA
$I_{OS}$	Output Short Circuit Current		-150		-60	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Max level is  $V_{CC} - 0.7$  V by design.

## AC CHARACTERISTICS $V_{CC} = 5.0$ V; GND= 0.0 V (Note 6 and Note 7)

Symbol	Characteristic	$-40^{\circ}C$			$25^{\circ}C$			$85^{\circ}C$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency					100					MHz
$t_{JITTER}$	Random Clock Jitter (RMS)					35					ps
$t_{PLH}$	Propagation Delay @ 1.5 V	2.0		5.5	2.0		5.5	2.0		5.5	ns
$t_{PHL}$	Propagation Delay @ 1.5 V	2.0		5.5	2.0		5.5	2.0		5.5	ns
$V_{PP}$	Input Swing (Note 8)	200		1000	200		1000	200		1000	mV
$t_r/t_f$	Output Rise Time (10–90%) Output Fall Time (10–90%)					1.6 1.1					ns ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6.  $V_{CC}$  can vary  $\pm 0.25$  V.

7. TTL output  $R_L = 500 \Omega$  to GND, and  $C_L = 20$  pF to GND. Refer to Figure 2.

8.  $V_{PP(min)}$  is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of  $\approx 40$ .

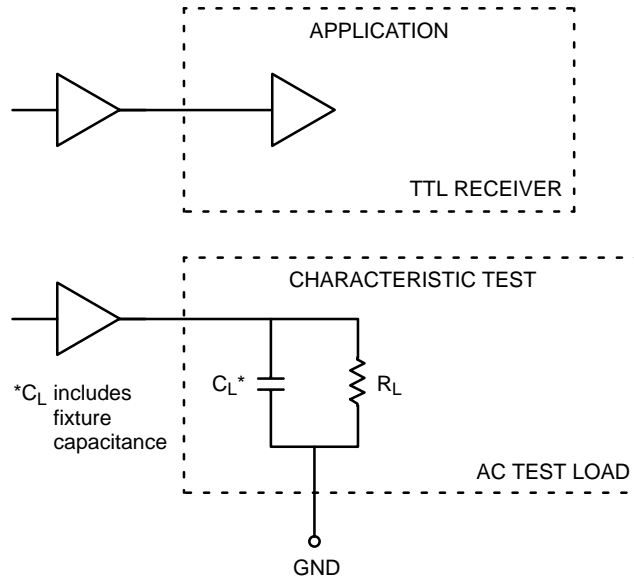


Figure 2. TTL Output Loading Used for Device Evaluation

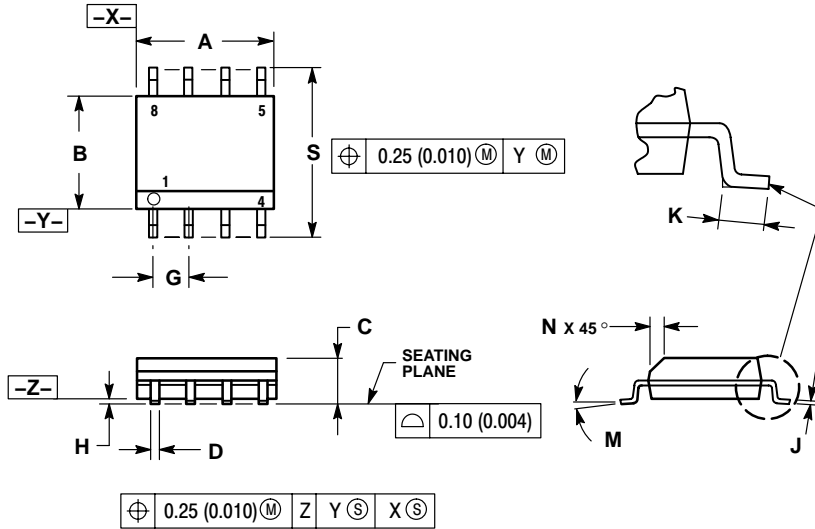
## Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices
- AND8090** – AC Characteristics of ECL Devices

# MC100ELT23

## PACKAGE DIMENSIONS

### SOIC-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE AB

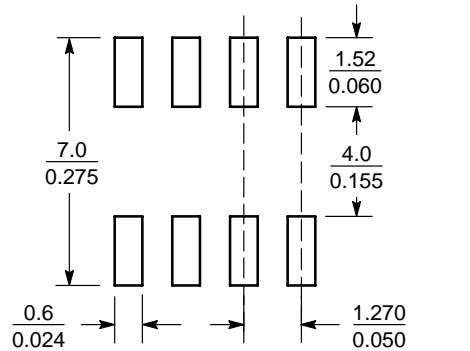


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT



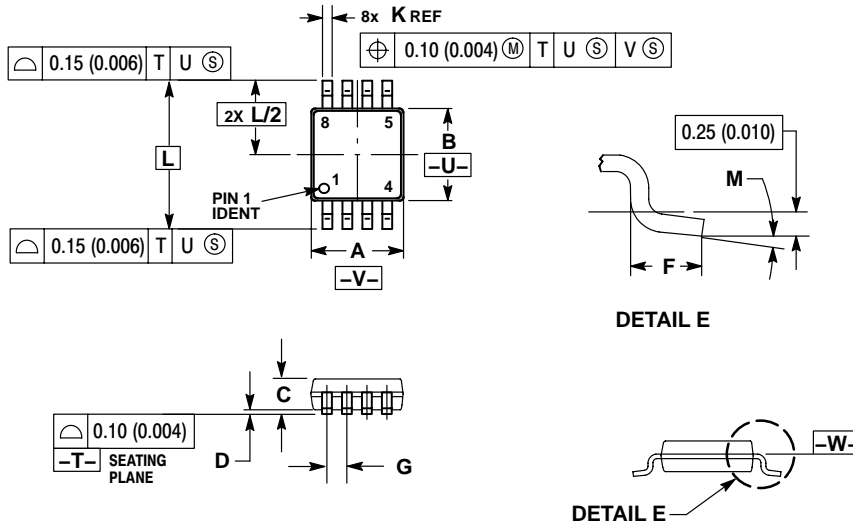
### SOIC-8

SCALE 6:1 (mm/inches)

# MC100ELT23


## PACKAGE DIMENSIONS

### TSSOP-8 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948R-02 ISSUE A



- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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