

High-Power PNP Silicon Transistors

... designed for use in industrial-military power amplifier and switching circuit applications.

• High Collector–Emitter Sustaining Voltage —

• High DC Current Gain —

$$h_{FE} = 20-80 @ I_C = 10 Adc$$

= 12 (Min) @ $I_C = 25 Adc$

• Low Collector-Emitter Saturation Voltage —

$$V_{CE(sat)} = 1.0 \text{ Vdc (Max)} @ I_C = 10 \text{ Adc}$$

• Fast Switching Times @ $I_C = 10$ Adc

 $t_r = 0.3 \mu s (Max)$

 $t_s = 1.0 \, \mu s \, (Max)$

 $t_f = 0.25 \, \mu s \, (Max)$

• Complement to NPN 2N6339 thru 2N6341

2N6437 2N6438*

*ON Semiconductor Preferred Device

25 AMPERE POWER TRANSISTORS PNP SILICON 100, 120 VOLTS 200 WATTS



CASE 1-07 TO-204AA (TO-3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N6437	2N6438	Unit
Collector-Base Voltage	V _{CB}	120	140	Vdc
Collector–Emitter Voltage	V_{CEO}	100	120	Vdc
Emitter–Base Voltage	V _{EB}	6.0 25 50 10		Vdc
Collector Current — Continuous Peak	I _C			Adc
Base Current	I _B			Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	200 1.14		Watts W/°C
Operating and Storage Junction Temperature Range	T _J ,T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta,IC}$	0.875	°C/W

⁽¹⁾ Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

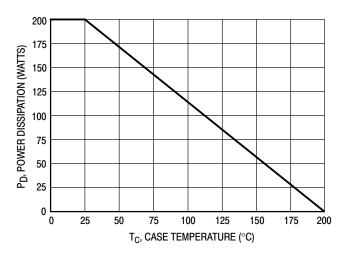


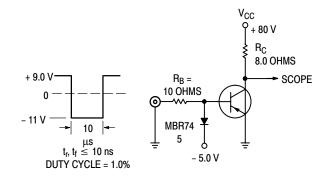
Figure 1. Power Derating

*ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) $(I_C = 50 \text{ mAdc}, I_B = 0)$	2N6437 2N6438	V _{CEO(sus)}	100 120	_	Vdc
Collector Cutoff Current $(V_{CE} = 50 \text{ Vdc}, I_B = 0)$ $(V_{CE} = 60 \text{ Vdc}, I_B = 0)$	2N6437 2N6438	I _{CEO}	_ _ _	50 50	μAdc
Collector Cutoff Current $ \begin{array}{l} (V_{CE}=110~\text{Vdc},~V_{BE(off)}=-1.5~\text{Vdc}) \\ (V_{CE}=130~\text{Vdc},~V_{BE(off)}=-1.5~\text{Vdc}) \\ (V_{CE}=100~\text{Vdc},~V_{BE(off)}=-1.5~\text{Vdc},~T_{C}=150~\text{C}) \\ (V_{CE}=120~\text{Vdc},~V_{BE(off)}=-1.5~\text{Vdc},~T_{C}=150~\text{C}) \end{array} $	2N6437 2N6438 2N6437 2N6438	I _{CEX}	_ _ _ _	10 10 1.0 1.0	μAdc mAdc
Collector Cutoff Current $(V_{CB} = 120 \text{ Vdc}, I_E = 0)$ $(V_{CB} = 140 \text{ Vdc}, I_E = 0)$	2N6437 2N6438	I _{CBO}	_ _	10 10	μAdc
Emitter Cutoff Current (V _{EB} = 6.0 Vdc, I _C = 0)		I _{EBO}		100	μAdc
ON CHARACTERISTICS					
DC Current Gain (1) ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 10 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 25 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$)		h _{FE}	30 20 12	 120 	_
Collector–Emitter Saturation Voltage (1) ($I_C = 10$ Adc, $I_B = 1.0$ Adc) ($I_C = 25$ Adc, $I_B = 2.5$ Adc)		V _{CE(sat)}	_	1.0 1.8	Vdc
Base–Emitter Saturation Voltage (1) $(I_C = 10 \text{ Adc}, I_B = 1.0 \text{ Adc})$ $(I_C = 25 \text{ Adc}, I_B = 2.5 \text{ Adc})$		V _{BE(sat)}		1.8 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I _C = 1.0 Adc, V _{CE} = 10 Vdc, f	test = 10 MHz)	f _T	40	_	MHz
Output Capacitance (V _{CE} = 10 Vdc, I _E = 0, f = 100 kHz)		C _{ob}	_	700	pF
SWITCHING CHARACTERISTICS					
Rise Time ($V_{CC} = 80 \text{ Vdc}$, $I_{C} = 10 \text{ A}$, $V_{BE(off)} = 6.0 \text{ Vdc}$, $I_{B1} = 1.0 \text{ Adc}$)		t _r	_	0.3	μs
Storage ($V_{CC} = 80 \text{ Vdc}$, $I_{C} = 10 \text{ A}$, $V_{BE(off)} = 6.0 \text{ Vdc}$, $I_{B1} = I_{B2} = 1.0 \text{ A}$	0 Adc)	t _s	_	1.0	μs
Fall Time ($V_{CC} = 80 \text{ Vdc}$, $I_{C} = 10 \text{ A}$, $V_{BE(off)} = 6.0 \text{ Vdc}$, $I_{B1} = I_{B2} = 1$.	.0 Adc)	t _f	_	0.25	μs
Indicates JEDEC Registered Data.					•

^{*}Indicates JEDEC Registered Data.

⁽¹⁾ Pulse Test: Pulse Width \leq 300 μ s; Duty Cycle \leq 2.0%.



NOTE: For information on Figures 3 and 6, R_{B} and R_{C} were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

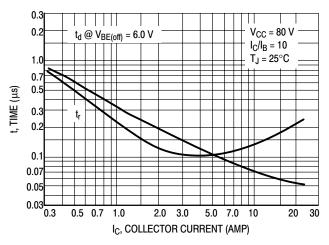


Figure 3. Turn-On Time

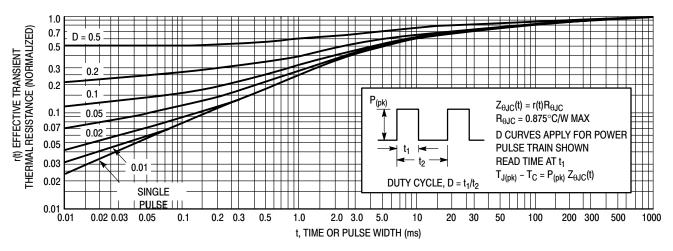


Figure 4. Thermal Response

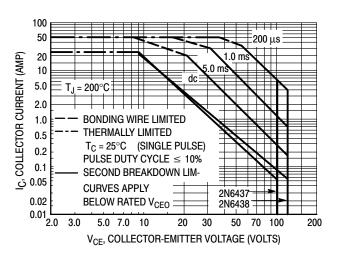


Figure 5. Active Region Safe Operating Area

operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will

reduce the power that can be handled to values less than the

limitations imposed by second breakdown.

There are two limitations on the power handling ability of

a transistor: average junction temperature and second

breakdown. Safe operating area curves indicate I_C - V_{CE}

limits of the transistor that must be observed for reliable

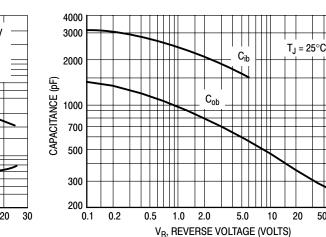


Figure 7. Capacitance

100

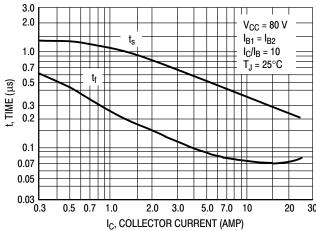


Figure 6. Turn-Off Time

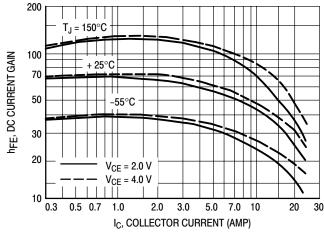


Figure 8. DC Current Gain

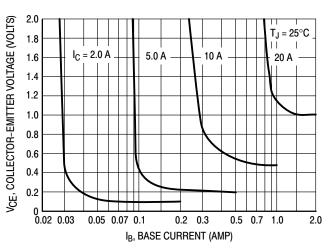


Figure 9. Collector Saturation Region

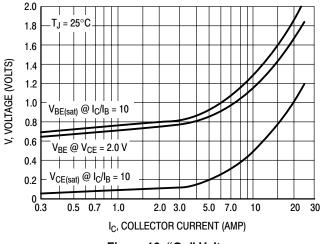


Figure 10. "On" Voltages

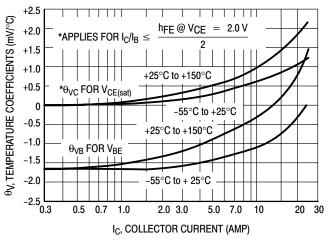


Figure 11. Temperature Coefficients

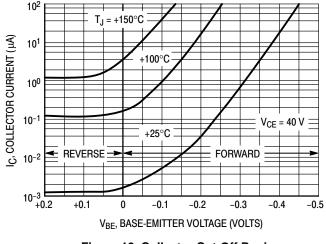


Figure 12. Collector Cut-Off Region

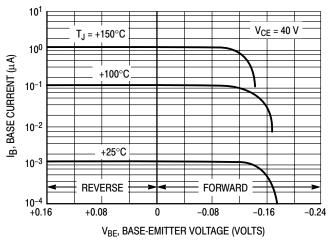
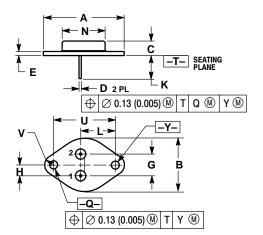


Figure 13. Base Cutoff Region

PACKAGE DIMENSIONS

CASE 1-07 TO-204AA (TO-3) ISSUE Z



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	1.550 REF		39.37 REF		
В		1.050		26.67	
С	0.250	0.335	6.35	8.51	
D	0.038	0.043	0.97	1.09	
Е	0.055	0.070	1.40	1.77	
G	0.430	BSC	10.92 BSC		
Н	0.215	BSC	5.46 BSC		
K	0.440	0.480	11.18 12.19		
L	0.665 BSC		16.89 BSC		
N		0.830		21.08	
Q	0.151	0.165	3.84	4.19	
U	1.187	BSC	30.15 BSC		
V	0.131	0.188	3 33	4 77	

STYLE 1: PIN 1. BASE 2. EMITTER CASE: COLLECTOR

Notes

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