



VNB14NV04/VND14NV04 VND14NV04-1/VNP14NV04/VNS14NV04

“OMNIFET II”: FULLY AUTOPROTECTED POWER MOSFET

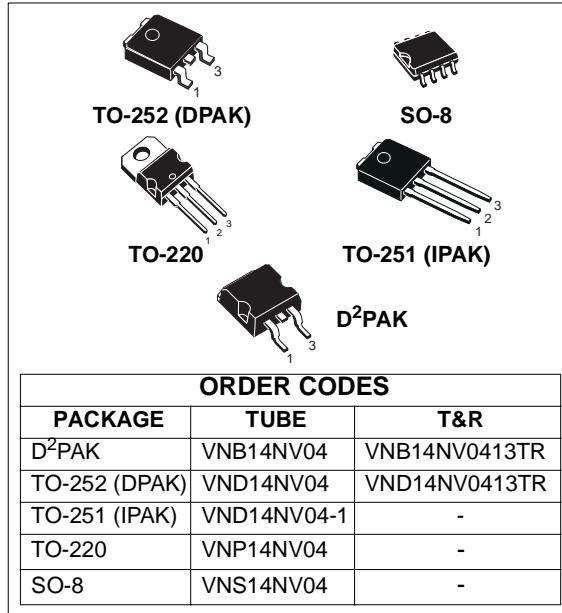
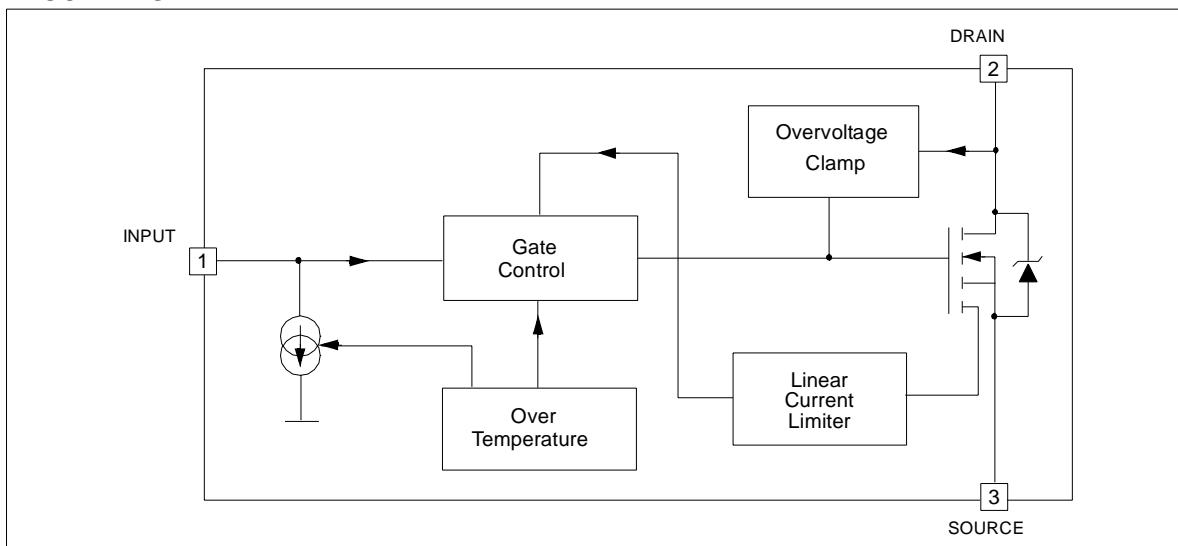
TYPE	R _{DS(on)}	I _{lim}	V _{clamp}
VNB14NV04			
VND14NV04	35 mΩ		
VND14NV04-1		12 A	
VNP14NV04			
VNS14NV04			

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

DESCRIPTION

The VNB14NV04, VND14NV04, VND14NV04-1, VNP14NV04, VNS14NV04, are monolithic devices designed in STMicroelectronics VIPower M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50KHz

BLOCK DIAGRAM



applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

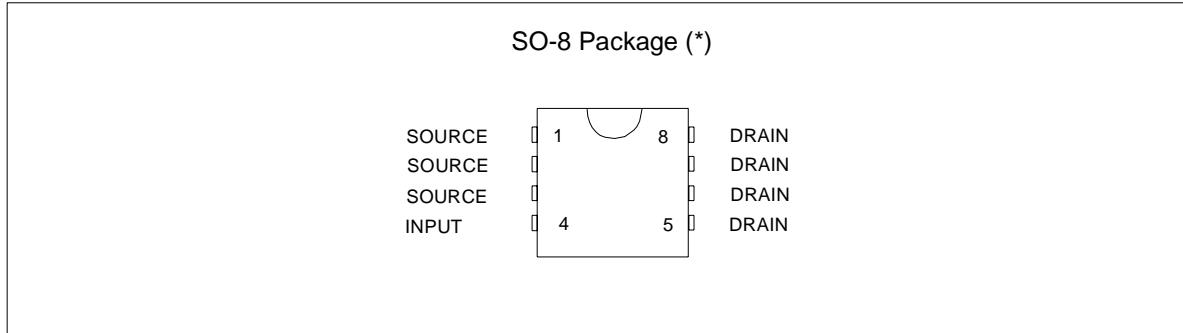
Fault feedback can be detected by monitoring the voltage at the input pin.

VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

ABSOLUTE MAXIMUM RATING

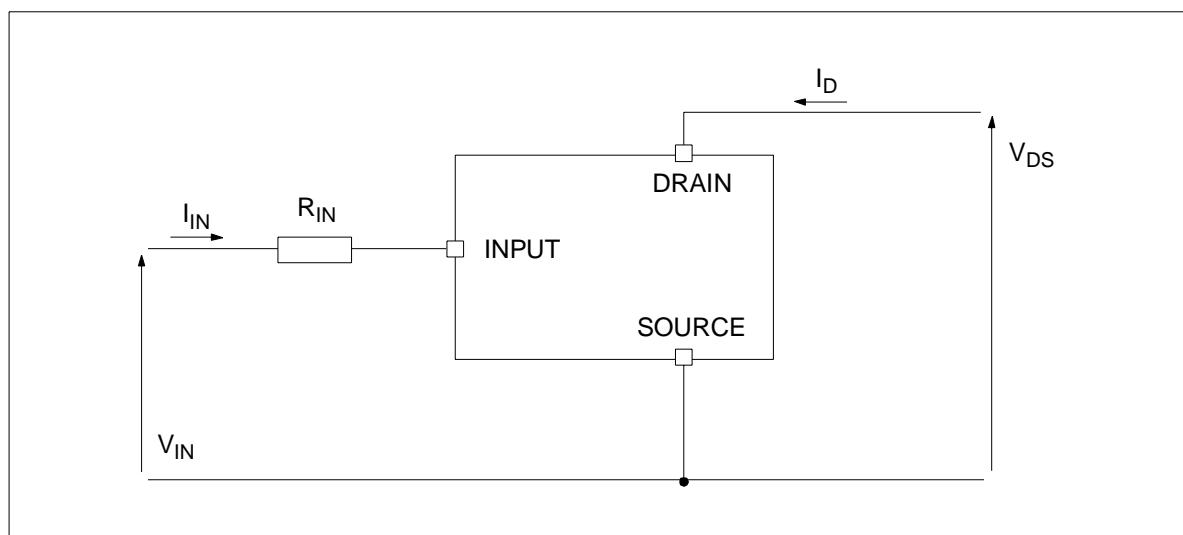
Symbol	Parameter	Value					Unit
		SO-8	DPAK	TO-220	IPAK	D ² PAK	
V_{DS}	Drain-source Voltage ($V_{IN}=0V$)			Internally Clamped			V
V_{IN}	Input Voltage			Internally Clamped			V
I_{IN}	Input Current			+/-20			mA
$R_{IN\ MIN}$	Minimum Input Series Impedance			10			Ω
I_D	Drain Current			Internally Limited			A
I_R	Reverse DC Output Current			-15			A
V_{ESD1}	Electrostatic Discharge ($R=1.5K\Omega$, $C=100pF$)			4000			V
V_{ESD2}	Electrostatic Discharge on output pin only ($R=330\Omega$, $C=150pF$)			16500			V
P_{tot}	Total Dissipation at $T_c=25^\circ C$	4.6	74	74	74	74	W
E_{MAX}	Maximum Switching Energy ($L=0.4mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_L=18A$)		93			93	mJ
T_j	Operating Junction Temperature			Internally limited			$^\circ C$
T_c	Case Operating Temperature			Internally limited			$^\circ C$
T_{stg}	Storage Temperature			-55 to 150			$^\circ C$

CONNECTION DIAGRAM (TOP VIEW)



(*) For the pins configuration related to DPAK, D²PAK, IPAK, TO-220 see outlines at page 1.

CURRENT AND VOLTAGE CONVENTIONS



VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

THERMAL DATA

Symbol	Parameter	Value					Unit
		SO-8	DPAK	TO-220	IPAK	D ² PAK	
R _{thj-case}	Thermal Resistance Junction-case MAX		1.7	1.7	1.7	1.7	°C/W
R _{thj-lead}	Thermal Resistance Junction-lead MAX	27					°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient MAX	90 (*)	65 (*)	62	102	52 (*)	°C/W

(*) When mounted on a standard single-sided FR4 board with 0.5cm² of Cu (at least 35 µm thick) connected to all DRAIN pins.
Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS (-40°C < T_j < 150°C, unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CLAMP}	Drain-source Clamp Voltage	V _{IN} =0V; I _D =7A	40	45	55	V
V _{CLTH}	Drain-source Clamp Threshold Voltage	V _{IN} =0V; I _D =2mA	36			V
V _{INTH}	Input Threshold Voltage	V _{DS} =V _{IN} ; I _D =1mA	0.5		2.5	V
I _{ISS}	Supply Current from Input Pin	V _{DS} =0V; V _{IN} =5V		100	150	µA
V _{INCL}	Input-Source Clamp Voltage	I _{IN} =1mA I _{IN} =-1mA	6 -1.0	6.8	8 -0.3	V
I _{DSS}	Zero Input Voltage Drain Current (V _{IN} =0V)	V _{DS} =13V; V _{IN} =0V; T _j =25°C V _{DS} =25V; V _{IN} =0V			30 75	µA

ON

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
R _{DS(on)}	Static Drain-source On Resistance	V _{IN} =5V; I _D =7A; T _j =25°C V _{IN} =5V; I _D =7A			35 70	mΩ

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ELECTRICAL CHARACTERISTICS (continued) ($T_j=25^\circ\text{C}$, unless otherwise specified)

DYNAMIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs} (*)	Forward Transconductance	$V_{DD}=13\text{V}$; $I_D=7\text{A}$		18		s
C_{OSS}	Output Capacitance	$V_{DS}=13\text{V}$; $f=1\text{MHz}$; $V_{IN}=0\text{V}$		400		pF

SWITCHING

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}$; $I_D=7\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=R_{IN\ MIN}=10\Omega$ (see figure 1)		80	250	ns
t_r	Rise Time			350	1000	ns
$t_{d(off)}$	Turn-off Delay Time			450	1350	ns
t_f	Fall Time			150	500	ns
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}$; $I_D=7\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=2.2\text{K}\Omega$ (see figure 1)		1.5	4.5	μs
t_r	Rise Time			9.7	30.0	μs
$t_{d(off)}$	Turn-off Delay Time			9	25.0	μs
t_f	Fall Time			10.2	30.0	μs
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD}=15\text{V}$; $I_D=7\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=R_{IN\ MIN}=10\Omega$		16		$\text{A}/\mu\text{s}$
Q_i	Total Input Charge	$V_{DD}=12\text{V}$; $I_D=7\text{A}$; $V_{IN}=5\text{V}$; $I_{gen}=2.13\text{mA}$ (see figure 5)		36.8		nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SD} (*)	Forward On Voltage	$I_{SD}=7\text{A}$; $V_{IN}=0\text{V}$		0.8		V
t_{rr}	Reverse Recovery Time	$I_{SD}=7\text{A}$; $di/dt=40\text{A}/\mu\text{s}$		300		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD}=30\text{V}$; $L=200\mu\text{H}$		0.8		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, figure 2)		5		A

PROTECTIONS (-40°C < T_j < 150°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	Drain Current Limit	$V_{IN}=5\text{V}$; $V_{DS}=13\text{V}$	12	18	24	A
t_{dlim}	Step Response Current Limit	$V_{IN}=5\text{V}$; $V_{DS}=13\text{V}$		45		μs
T_{jsh}	Overtemperature Shutdown		150	175	200	$^\circ\text{C}$
T_{jrs}	Overtemperature Reset		135			$^\circ\text{C}$
I_{gf}	Fault Sink Current	$V_{IN}=5\text{V}$; $V_{DS}=13\text{V}$; $T_j=T_{jsh}$	10	15	20	mA
E_{as}	Single Pulse Avalanche Energy	starting $T_j=25^\circ\text{C}$; $V_{DD}=24\text{V}$ $V_{IN}=5\text{V}$; $R_{gen}=R_{IN\ MIN}=10\Omega$; $L=24\text{mH}$ (see figures 3 & 4)	400			mJ

(*) Pulsed: Pulse duration = 300μs, duty cycle 1.5%

PROTECTION FEATURES

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 50KHz. The only difference from the user's standpoint is that a small DC current I_{ISS} (typ. 100 μ A) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

- OVERVOLTAGE CLAMP PROTECTION:

internally set at 45V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

- LINEAR CURRENT LIMITER CIRCUIT:

limits the drain current I_D to I_{lim} whatever the INPUT pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

- OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:

these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15°C below shut-down temperature.

- STATUS FEEDBACK:

in the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current I_{gf} , the INPUT pin will fall to 0V. **This will not however affect the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current I_{SS} .**

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

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Figure 1: Switching Time Test Circuit for Resistive Load

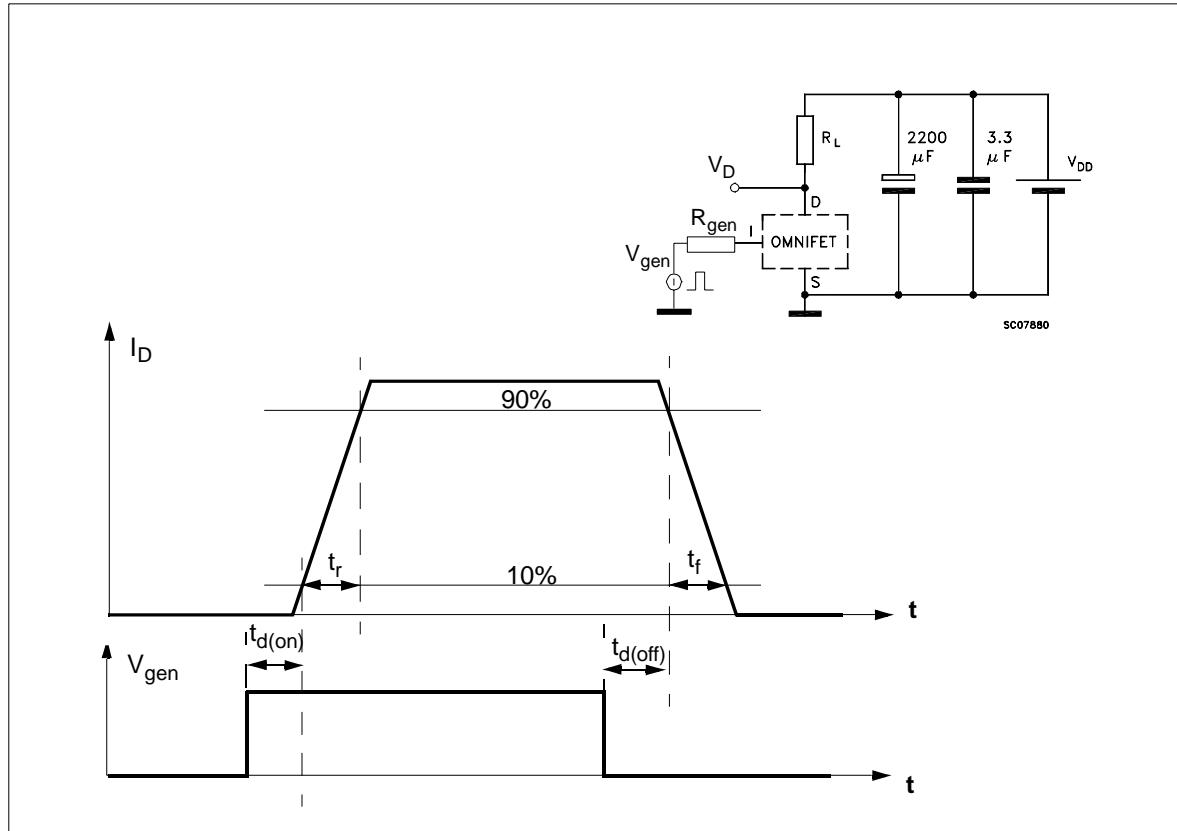
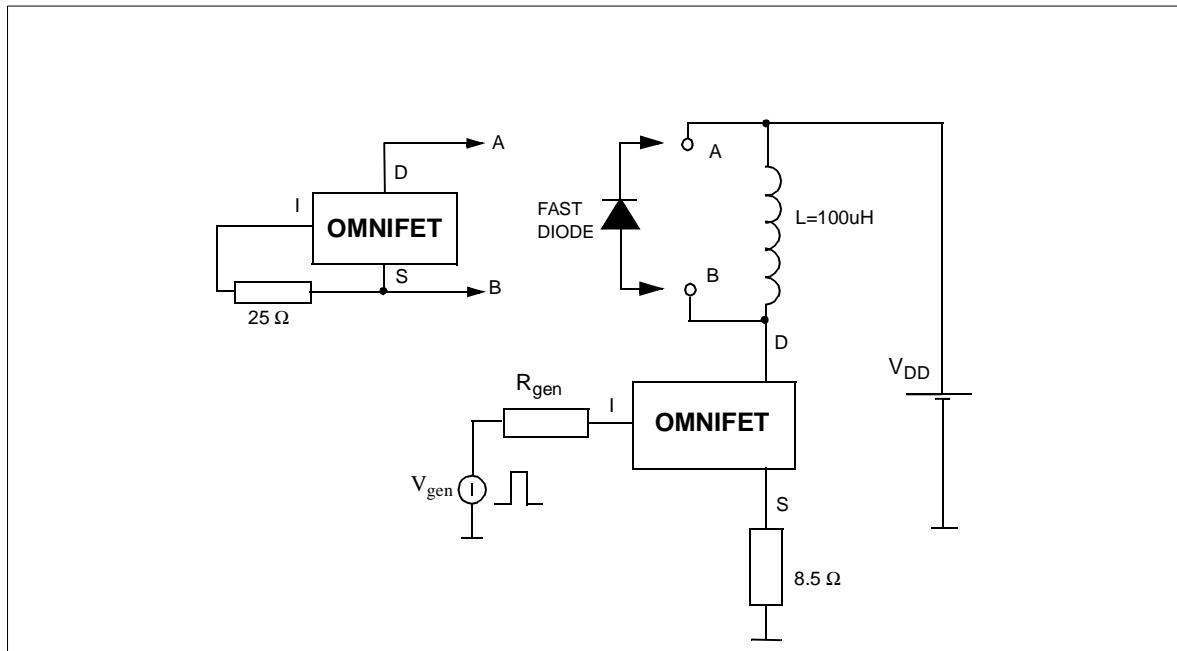


Figure 2: Test Circuit for Diode Recovery Times



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Figure 3: Unclamped Inductive Load Test Circuits

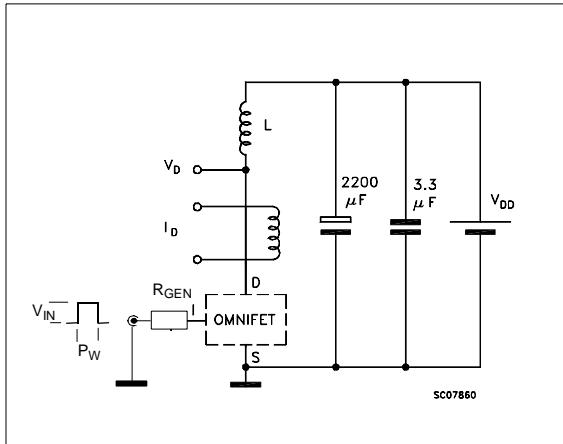


Figure 4: Unclamped Inductive Waveforms

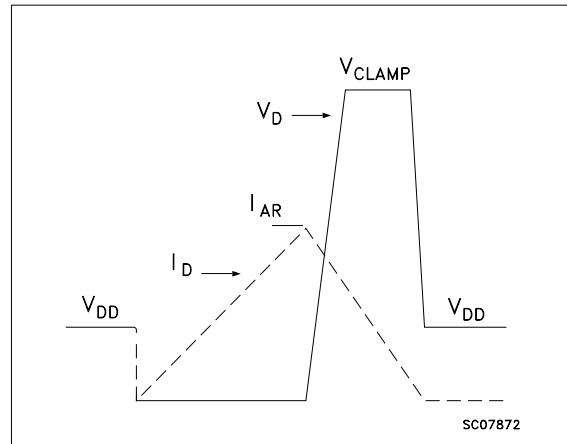
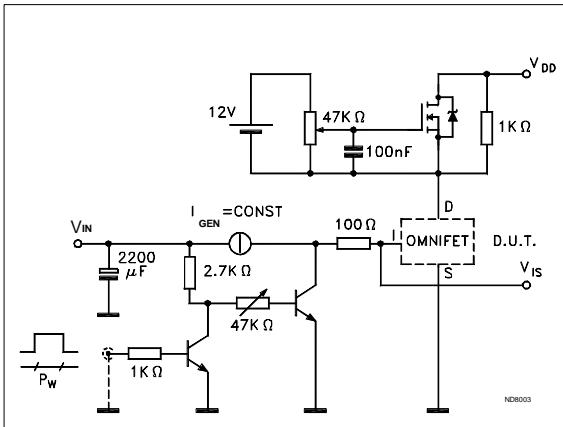
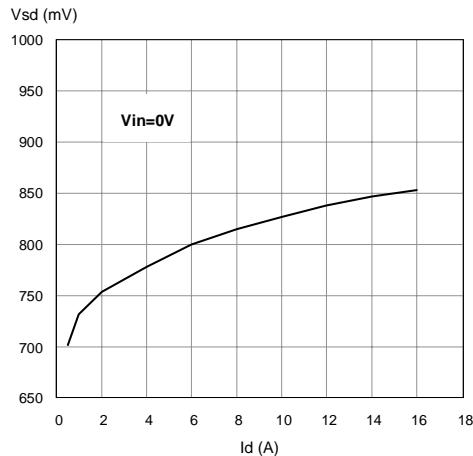


Figure 5: Input Charge Test Circuit

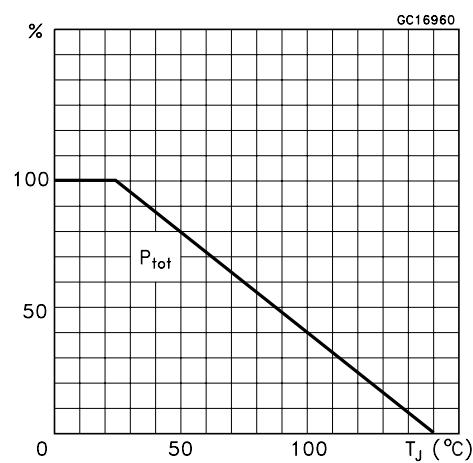


VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

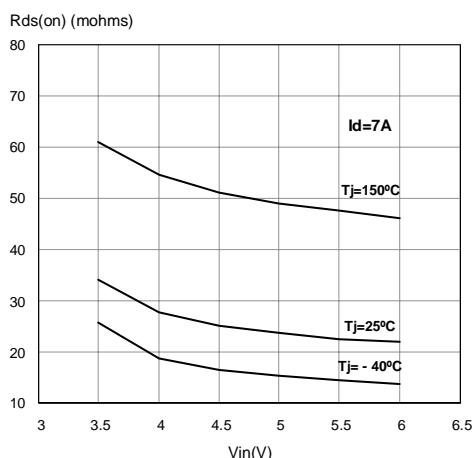
Source-Drain Diode Forward Characteristics



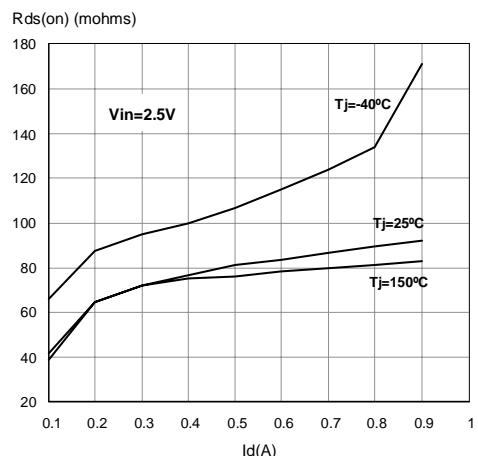
Derating Curve



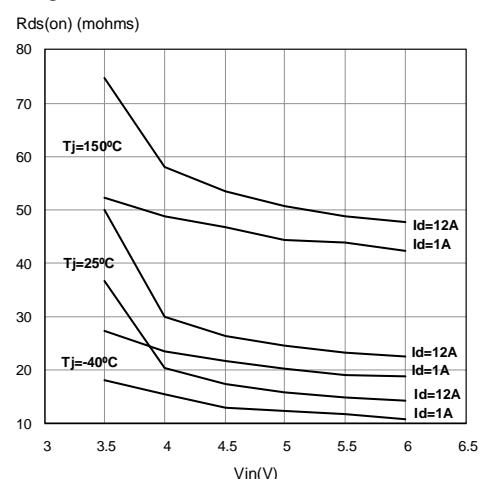
Static Drain-Source On resistance Vs. Input Voltage



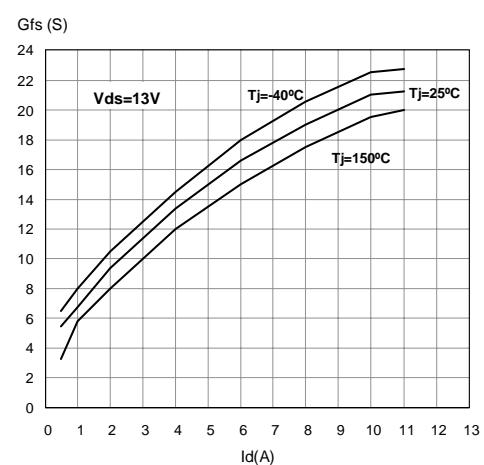
Static Drain Source On Resistance



Static Drain-Source On resistance Vs. Input Voltage

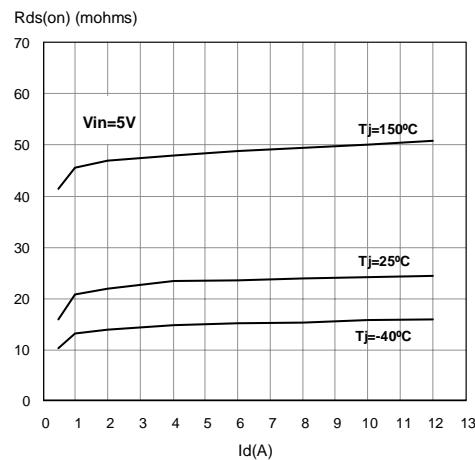


Transconductance

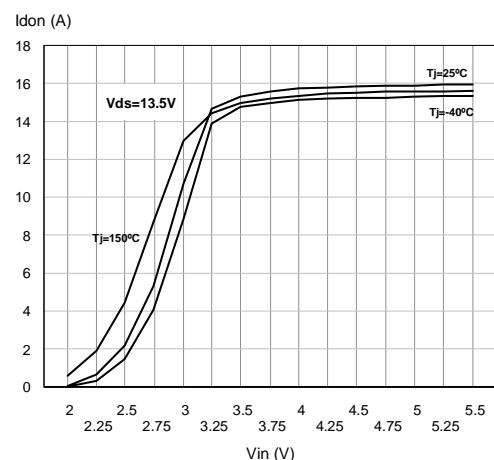


VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

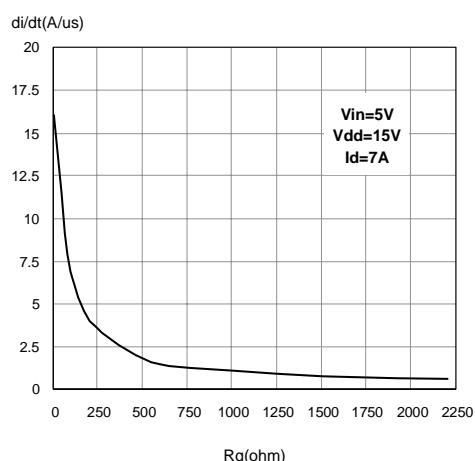
Static Drain-Source On Resistance Vs. Id



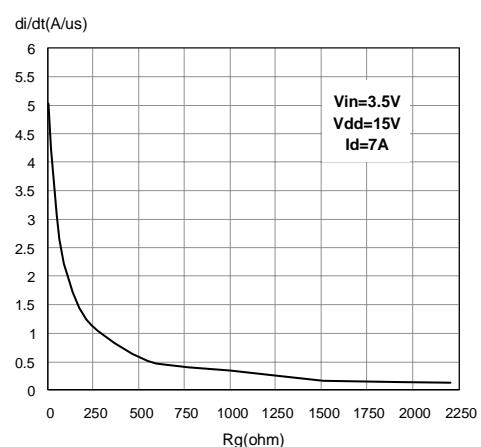
Transfer Characteristics



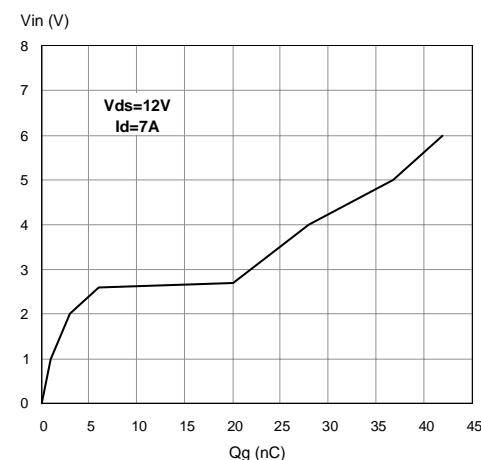
Turn On Current Slope



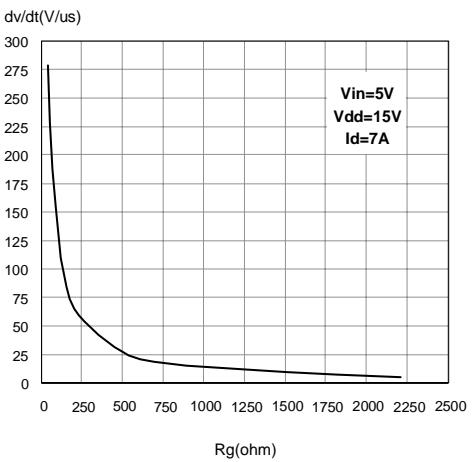
Turn On Current Slope



Input Voltage Vs. Input Charge

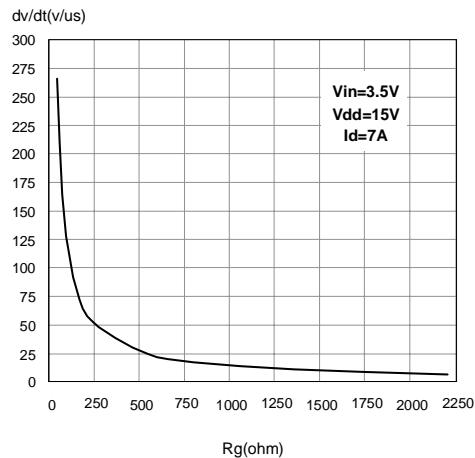


Turn off drain source voltage slope

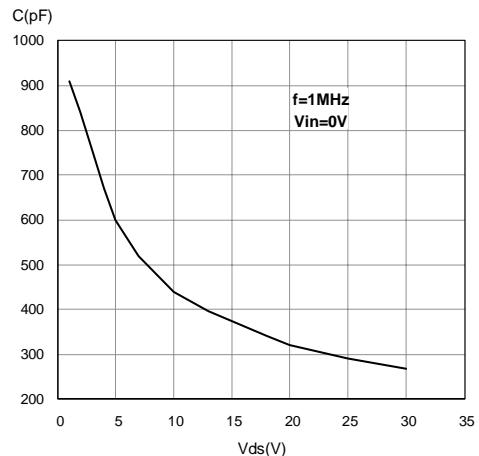


VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

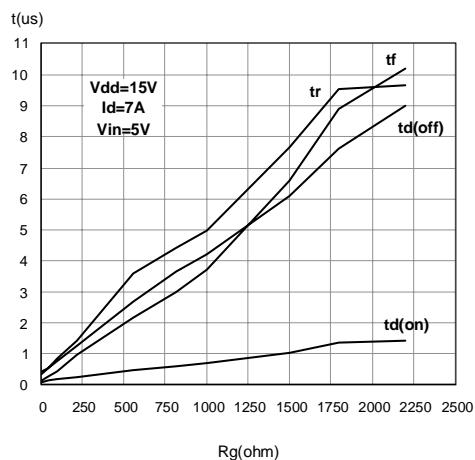
Turn Off Drain-Source Voltage Slope



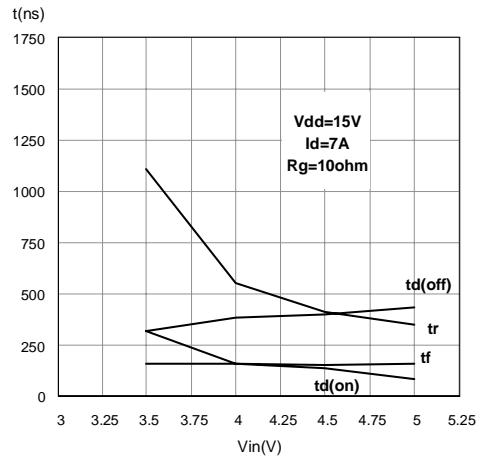
Capacitance Variations



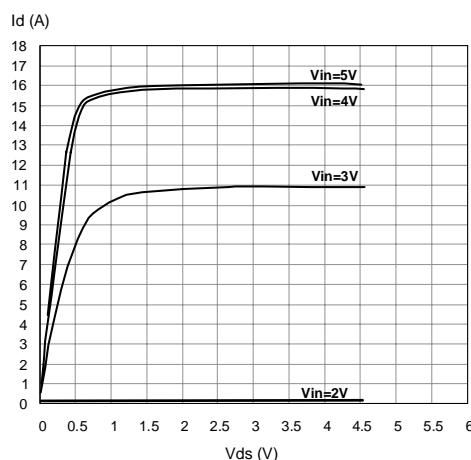
Switching Time Resistive Load



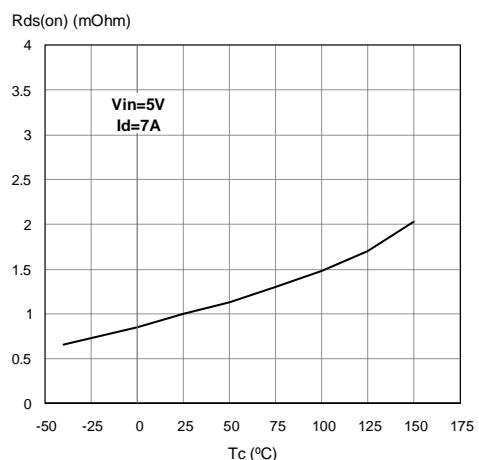
Switching Time Resistive Load



Output Characteristics

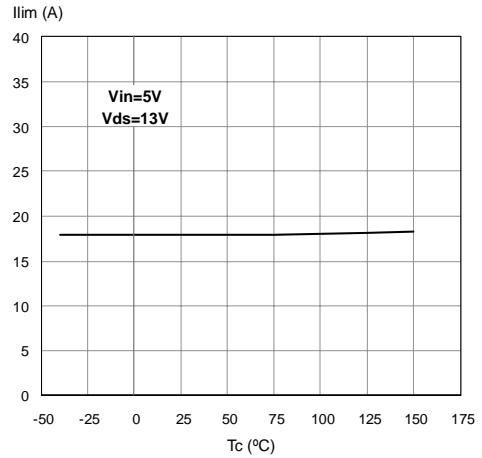
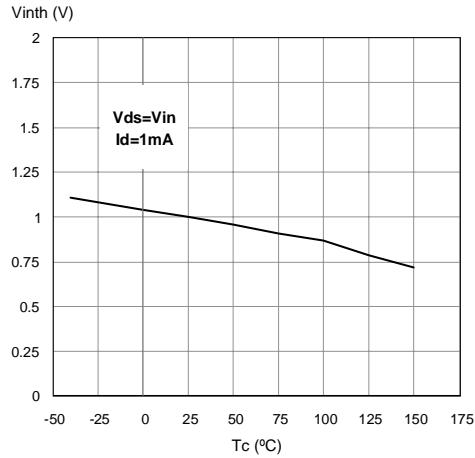


Normalized On Resistance Vs. Temperature

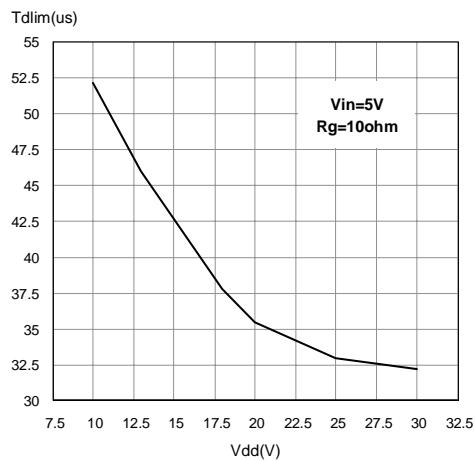


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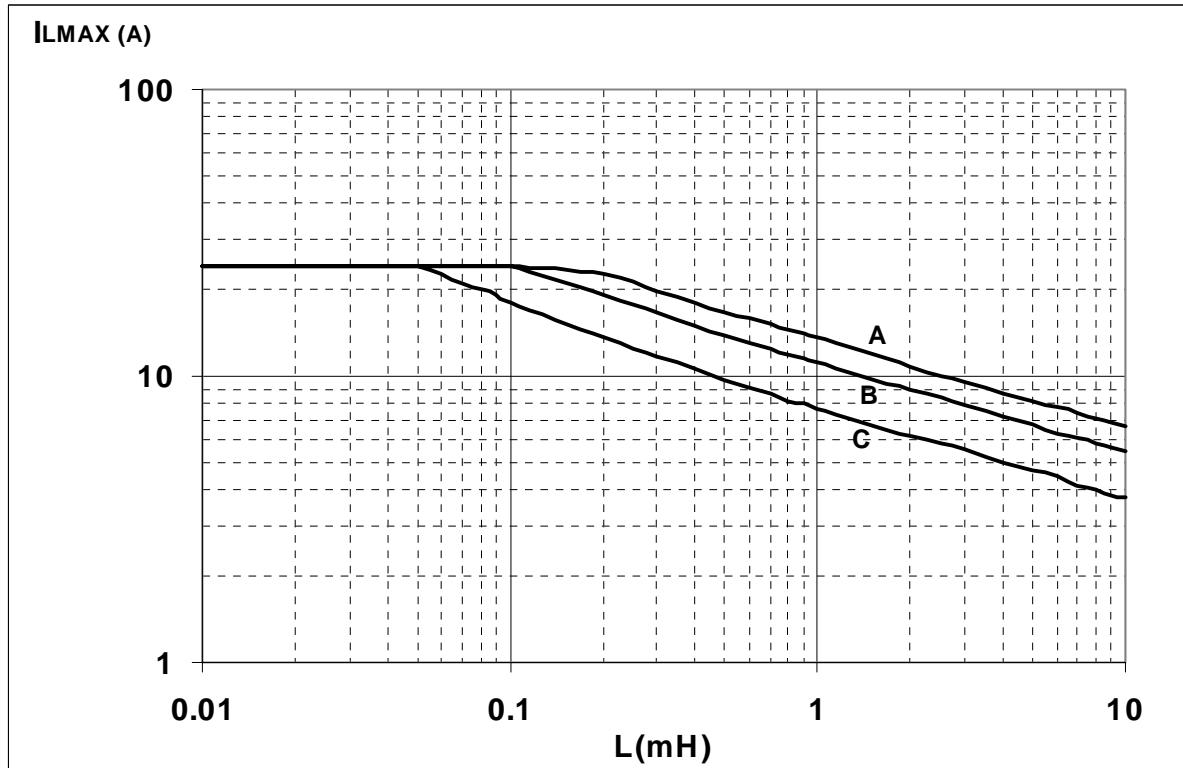
Normalized Input Threshold Voltage Vs. Current Limit Vs. Junction Temperature



Step Response Current Limit



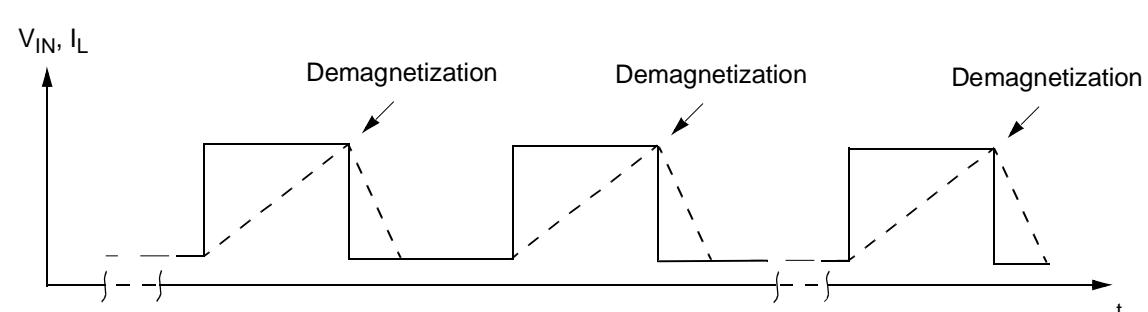
DPAK Maximum turn off current versus load inductance



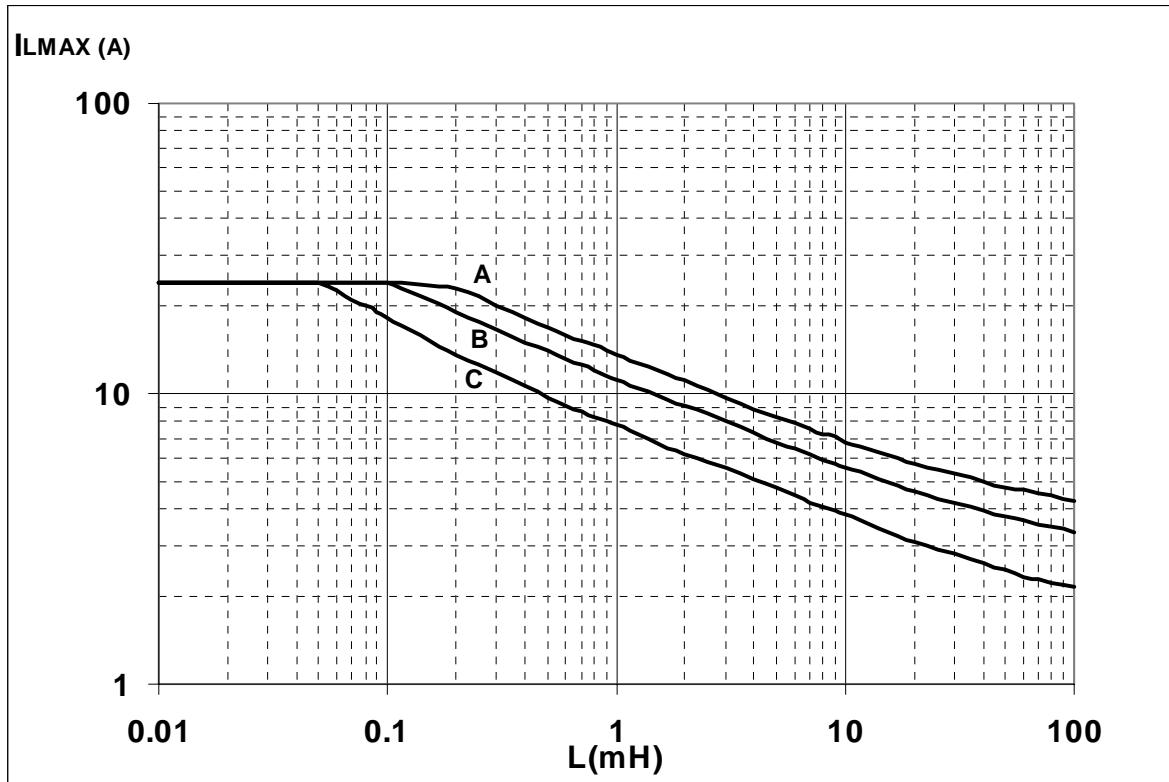
Conditions:

$V_{CC}=13.5\text{V}$

Values are generated with $R_L=0\Omega$
In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



D²PAK Maximum turn off current versus load inductance



A = Single Pulse at $T_{j\text{start}}=150^\circ\text{C}$

B= Repetitive pulse at $T_{j\text{start}}=100^\circ\text{C}$

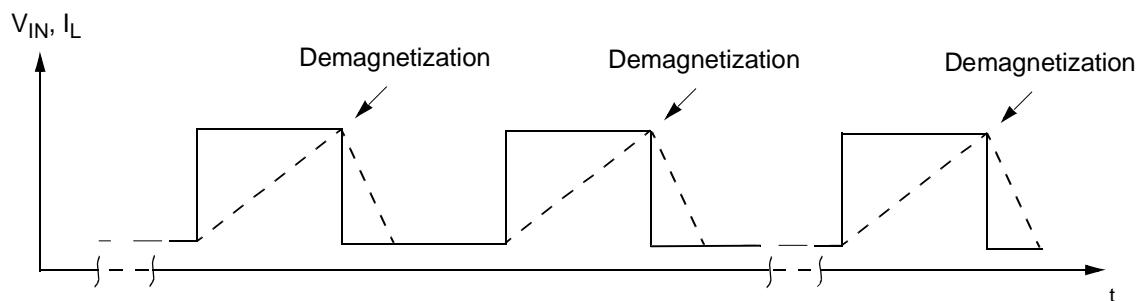
C= Repetitive Pulse at $T_{j\text{start}}=125^\circ\text{C}$

Conditions:

$V_{CC}=13.5\text{V}$

Values are generated with $R_L=0\Omega$

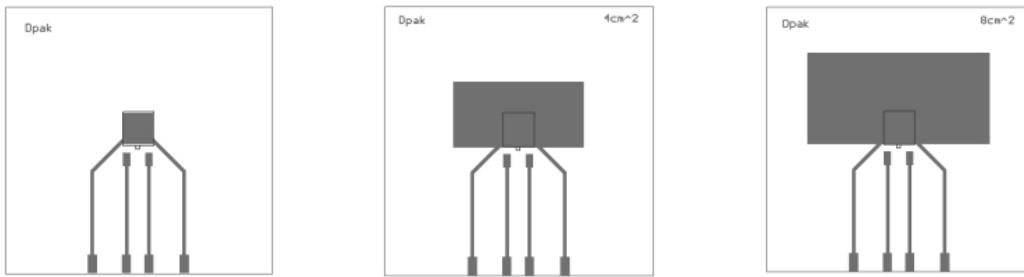
In case of repetitive pulses, $T_{j\text{start}}$ (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



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DPAK THERMAL DATA

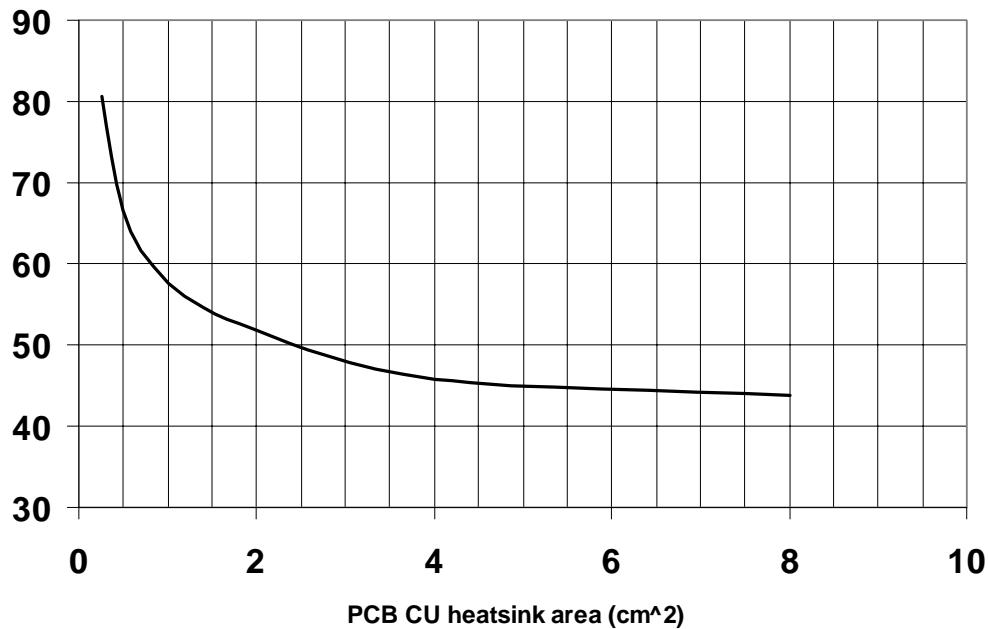
DPAK PC Board



Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 60mm x 60mm, PCB thickness=2mm, Cu thickness=35 μ m, Copper areas: from minimum pad lay-out to 8cm 2).

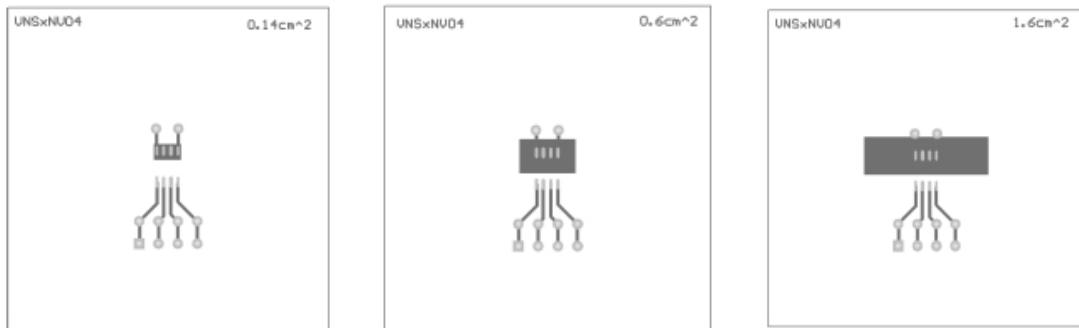
$R_{thj\text{-amb}}$ Vs PCB copper area in open box free air condition

$R_{thj\text{-amb}}$ ($^{\circ}\text{C/W}$)



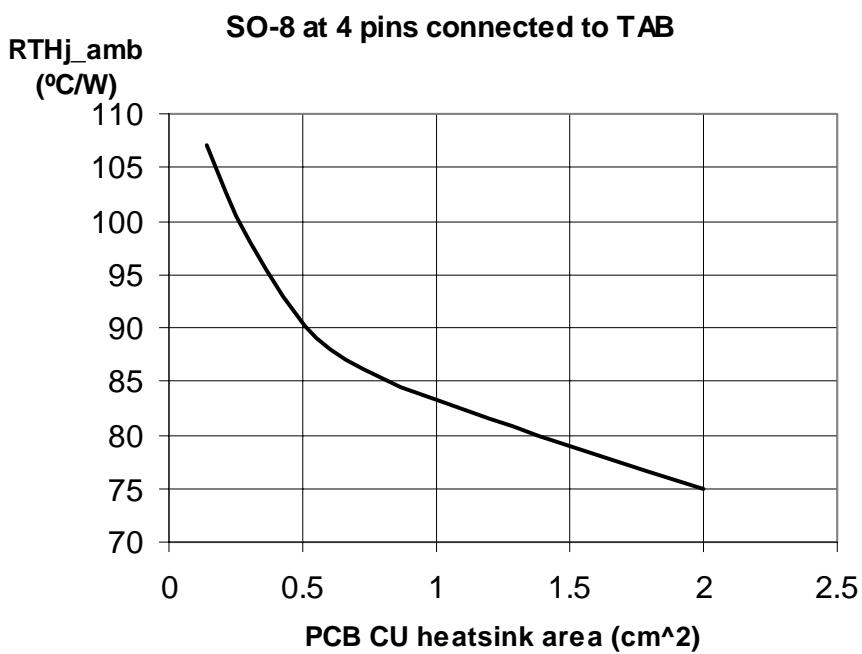
SO-8 THERMAL DATA

SO-8 PC Board



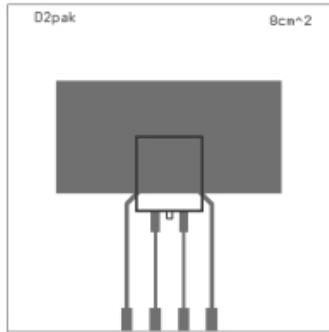
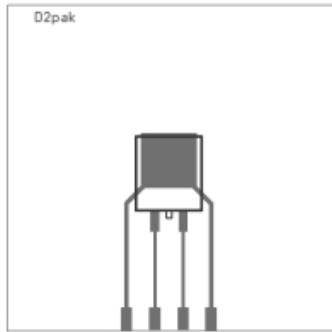
Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35 μ m, Copper areas: 0.14cm 2 , 0.6cm 2 , 1.6cm 2).

R_{thj_amb} Vs PCB copper area in open box free air condition



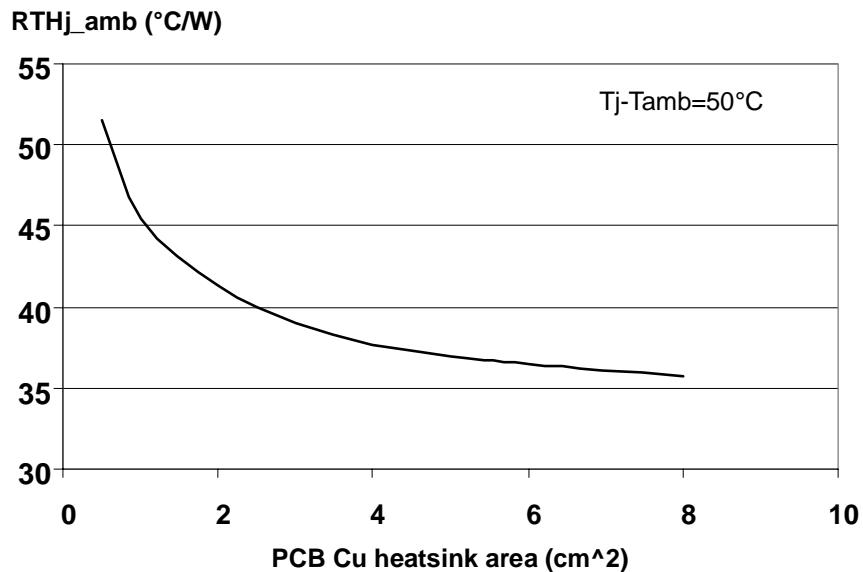
D²PAK THERMAL DATA

D²PAK PC Board

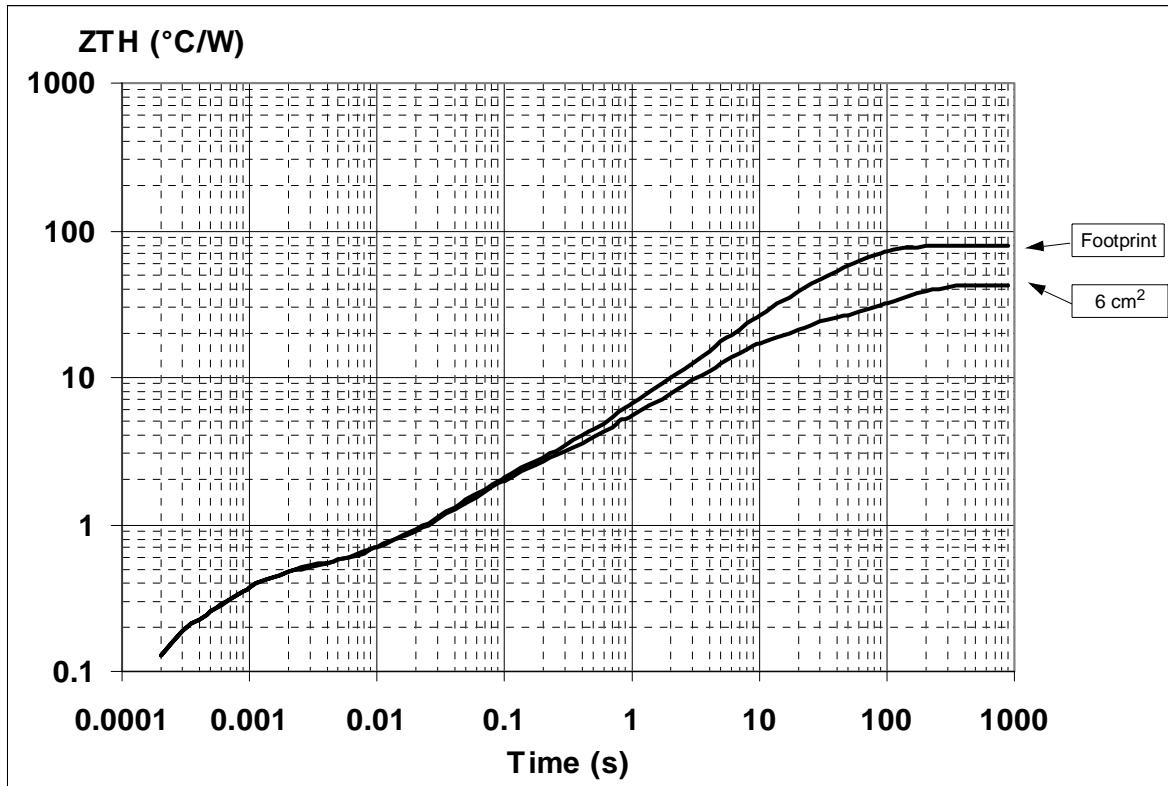


Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 60mm x 60mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: from minimum pad lay-out to 8cm²).

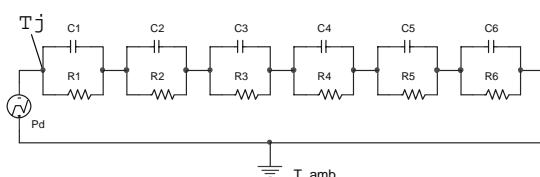
$R_{thj-amb}$ Vs PCB copper area in open box free air condition



DPAK Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of an OMNIFET II in DPAK



Pulse calculation formula

$$Z_{\text{TH}\delta} = R_{\text{TH}} \cdot \delta + Z_{\text{THtp}}(1 - \delta)$$

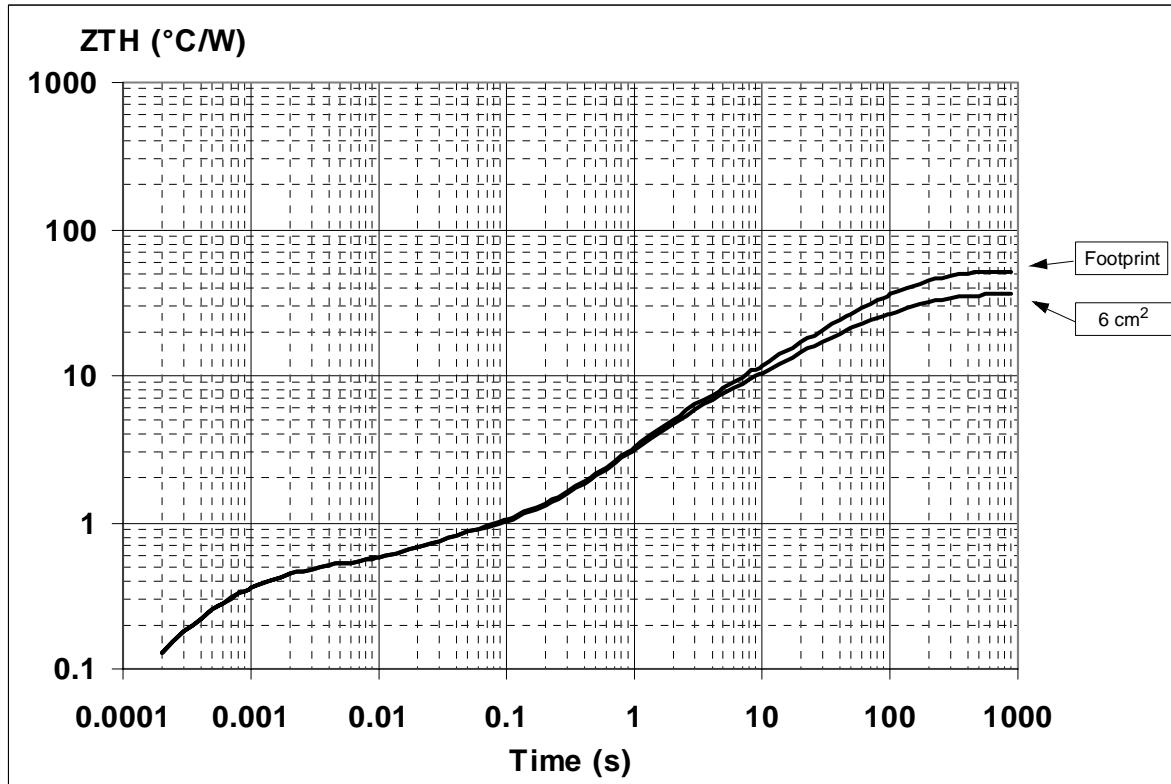
where $\delta = t_p/T$

Thermal Parameter

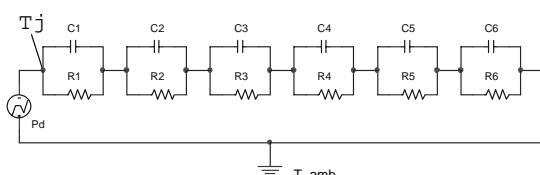
Area/island (cm^2)	Footprint	6
R1 ($^{\circ}\text{C}/\text{W}$)	0.1	
R2 ($^{\circ}\text{C}/\text{W}$)	0.35	
R3 ($^{\circ}\text{C}/\text{W}$)	1.20	
R4 ($^{\circ}\text{C}/\text{W}$)	2	
R5 ($^{\circ}\text{C}/\text{W}$)	15	
R6 ($^{\circ}\text{C}/\text{W}$)	61	24
C1 ($\text{W.s}/^{\circ}\text{C}$)	0.0006	
C2 ($\text{W.s}/^{\circ}\text{C}$)	0.0021	
C3 ($\text{W.s}/^{\circ}\text{C}$)	0.05	
C4 ($\text{W.s}/^{\circ}\text{C}$)	0.3	
C5 ($\text{W.s}/^{\circ}\text{C}$)	0.45	
C6 ($\text{W.s}/^{\circ}\text{C}$)	0.8	5

VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

D²PAK Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of an OMNIFET II in D²PAK



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

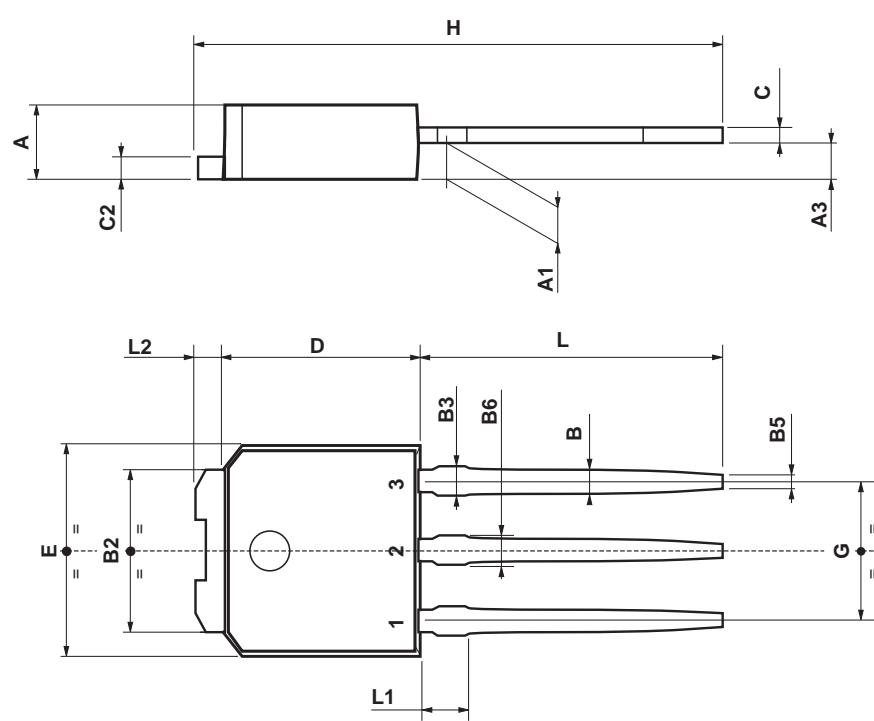
where $\delta = t_p/T$

Thermal Parameter

Area/island (cm ²)	Footprint	6
R1 (°C/W)	0.1	
R2 (°C/W)	0.35	
R3 (°C/W)	0.3	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	2.10E-03	
C3 (W.s/°C)	8.00E-02	
C4 (W.s/°C)	0.45	
C5 (W.s/°C)	2	
C6 (W.s/°C)	3	5

TO-251 (IPAK) MECHANICAL DATA

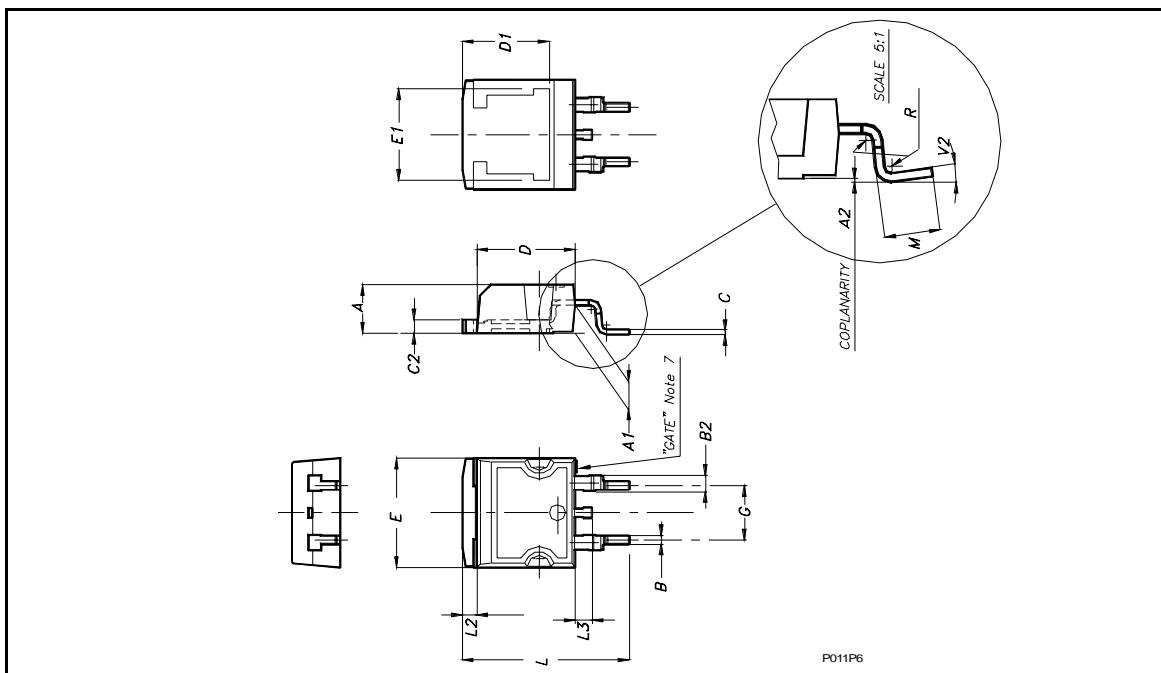
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

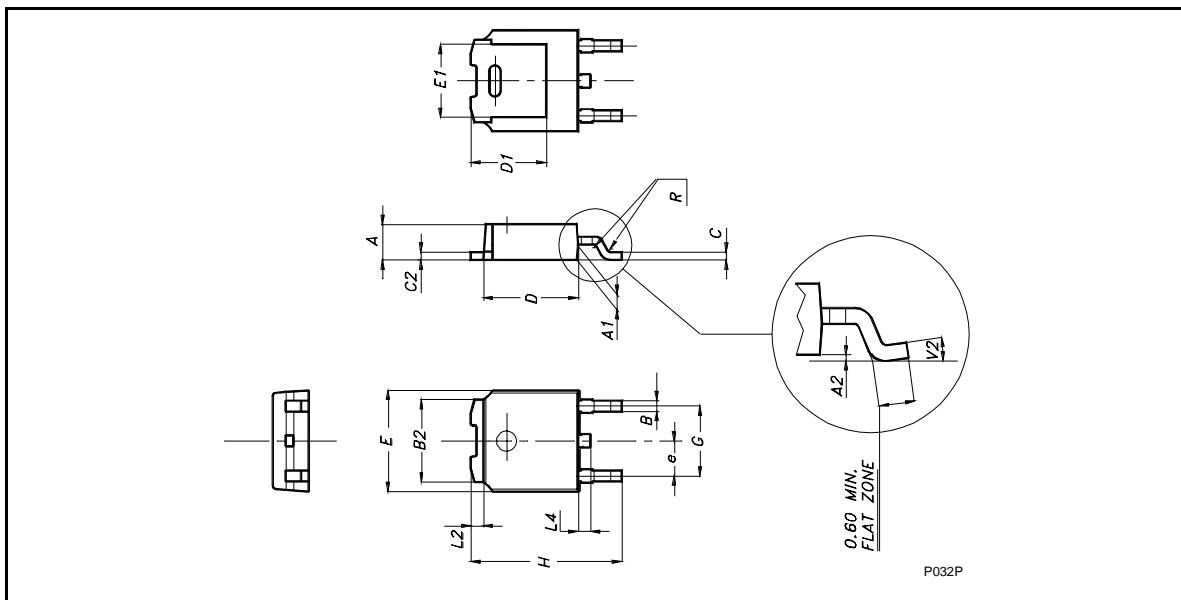
D²PAK MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A	4.4		4.6
A1	2.49		2.69
A2	0.03		0.23
B	0.7		0.93
B2	1.14		1.7
C	0.45		0.6
C2	1.23		1.36
D	8.95		9.35
D1		8	
E	10		10.4
E1		8.5	
G	4.88		5.28
L	15		15.85
L2	1.27		1.4
L3	1.4		1.75
M	2.4		3.2
R		0.4	
V2	0°		8°



TO-252 (DPAK) MECHANICAL DATA

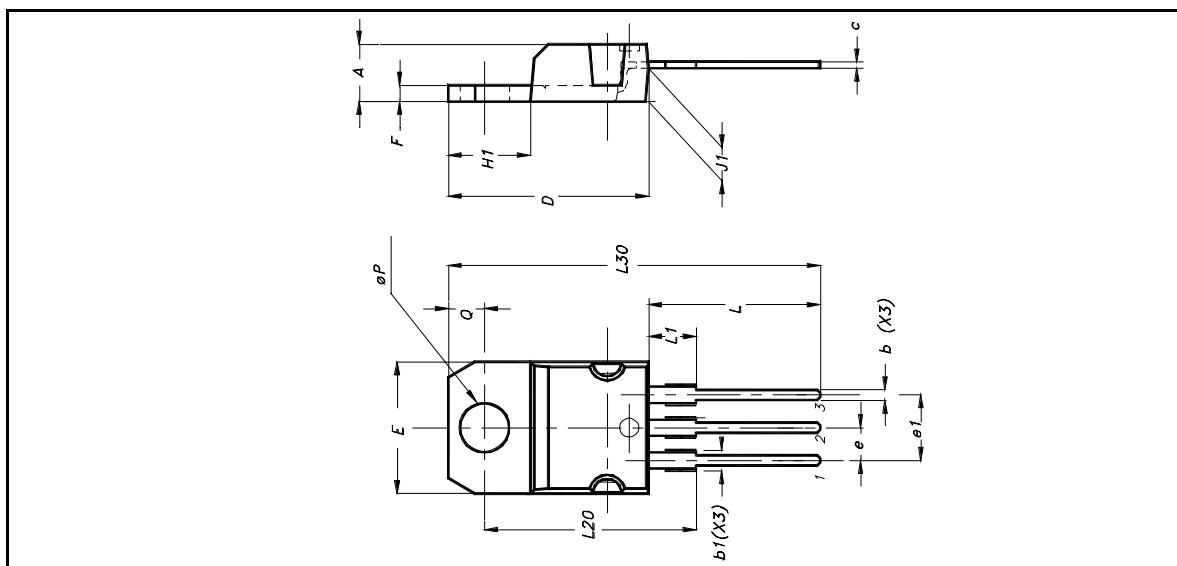
DIM.	mm.		
	MIN.	TYP	MAX.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		2.28	
G	4.40		4.60
H	9.35		10.10
L2		0.8	
L4	0.60		1.00
R		0.2	
V2	0°	8°	
Package Weight	Gr. 0.29		



VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

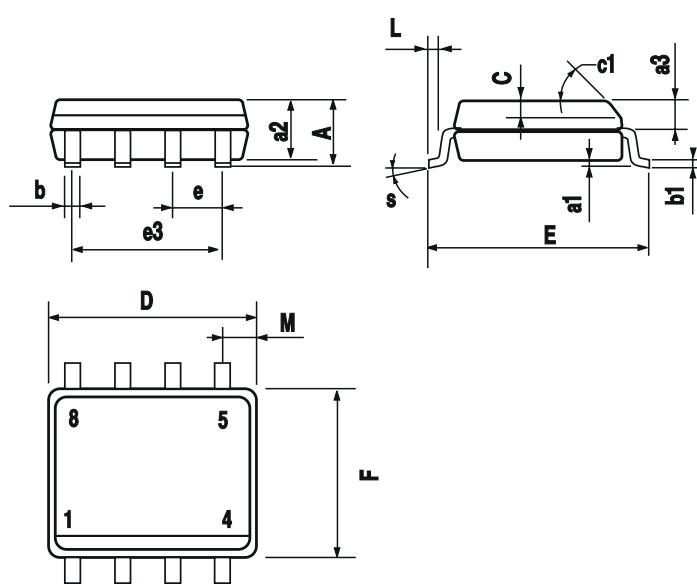
TO-220 MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A	4.40		4.60
b	0.61		0.88
b1	1.15		1.70
c	0.49		0.70
D	15.25		15.75
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95
Package Weight	1.9Gr. (Typ.)		



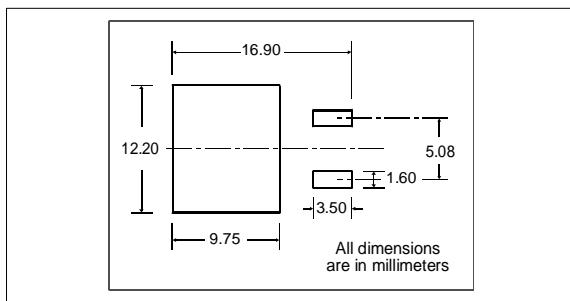
SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
F	8 (max.)					

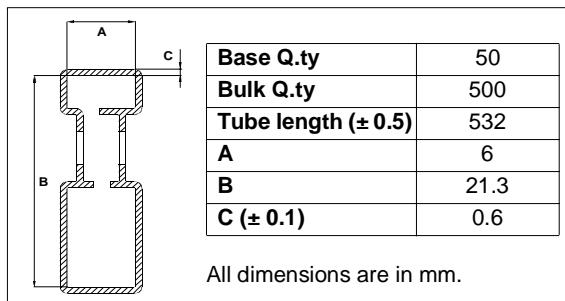


VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

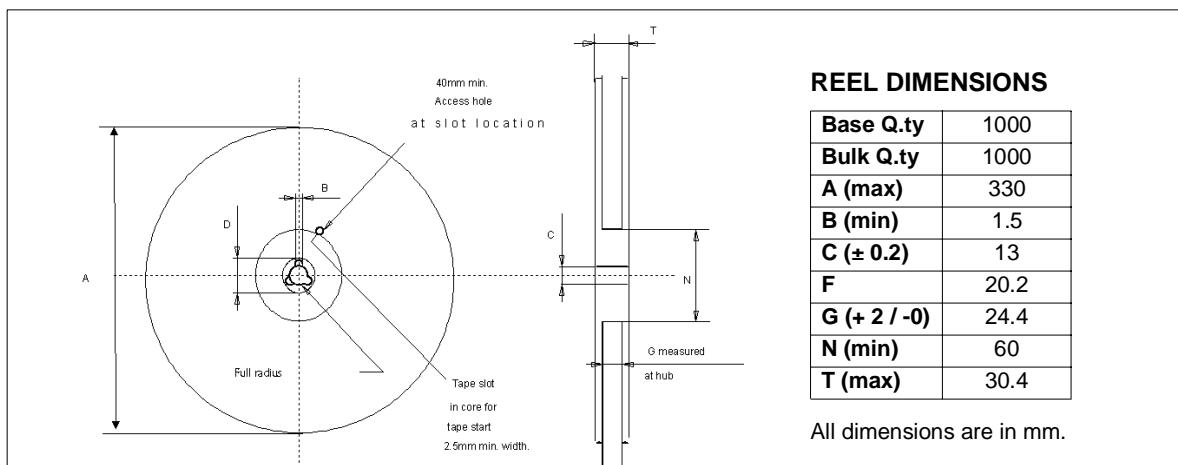
D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)



TAPE AND REEL SHIPMENT (suffix "13TR")

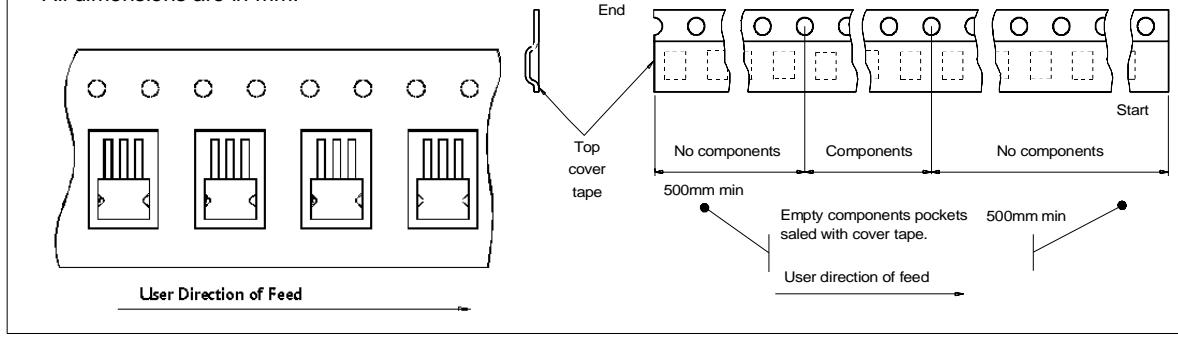
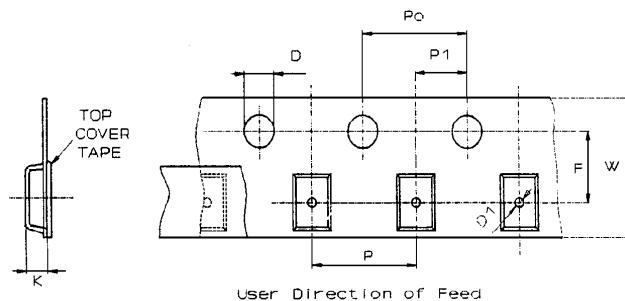


TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

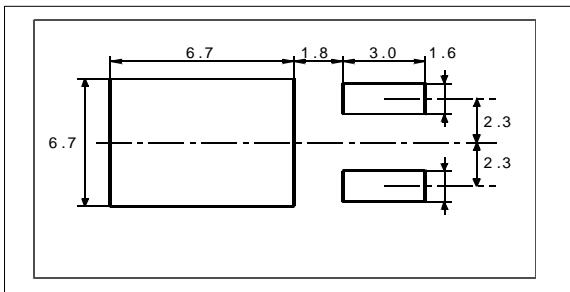
Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	16
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

DPAK FOOTPRINT

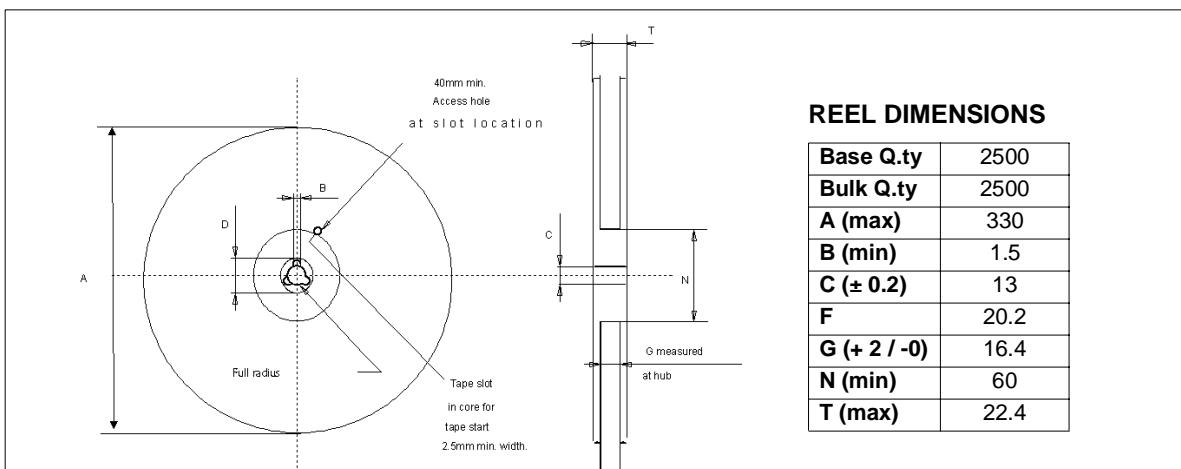


TUBE SHIPMENT (no suffix)

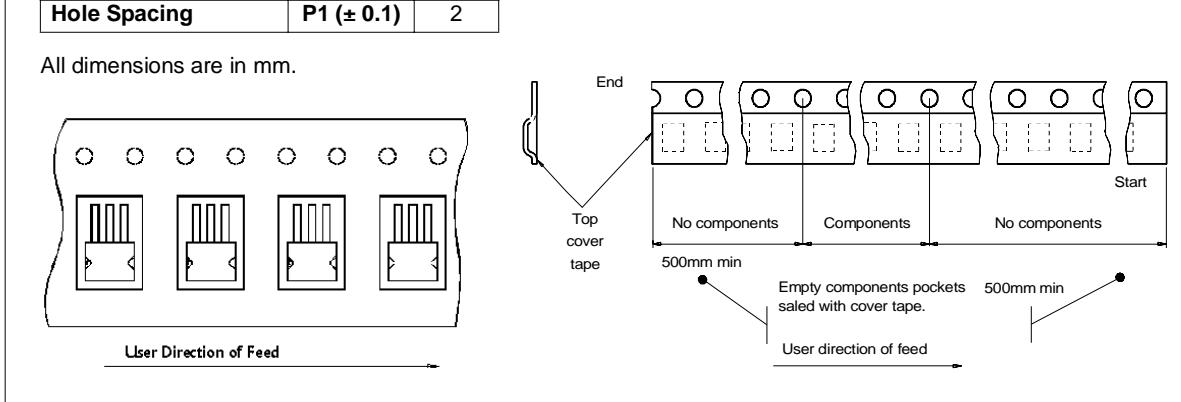
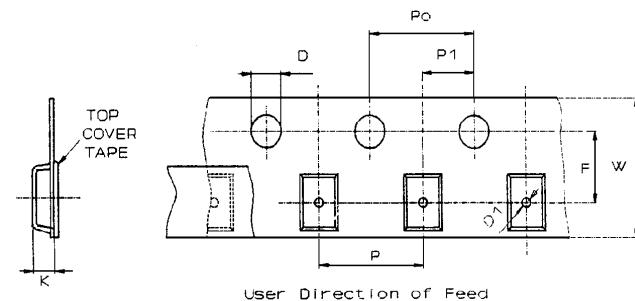
Base Q.ty	75
Bulk Q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")

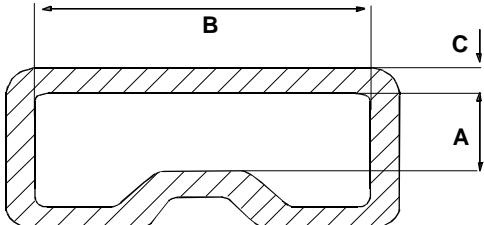


All dimensions are in mm.



VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

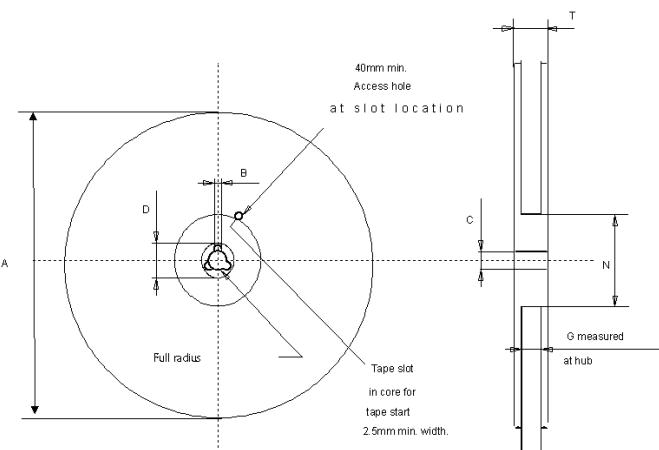
SO-8 TUBE SHIPMENT (no suffix)



A	3.2
B	6
C (± 0.1)	0.6
Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS	
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

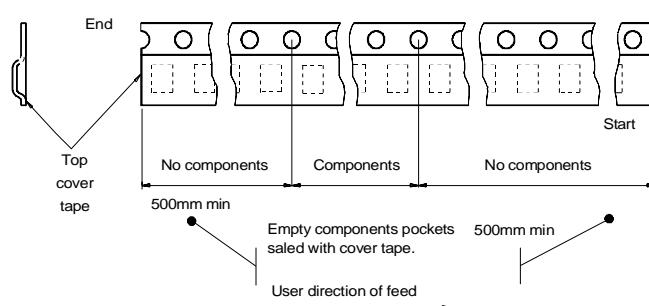
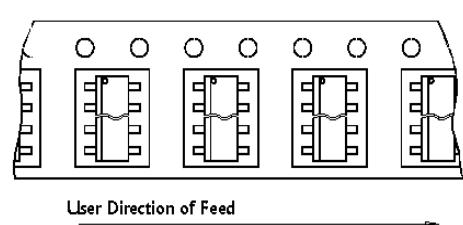
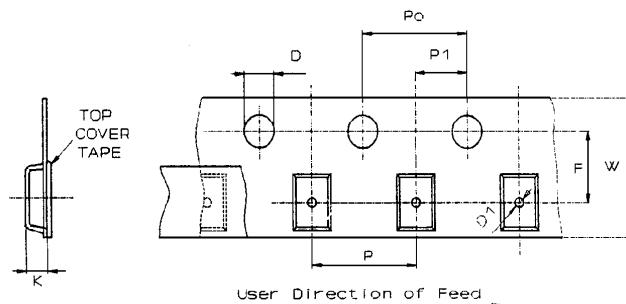
All dimensions are in mm.

TAPE DIMENSIONS

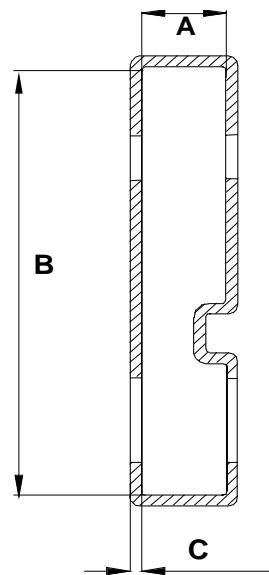
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



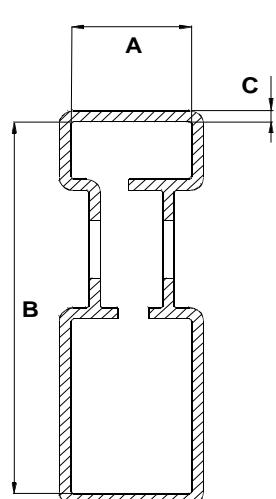
TO-220 TUBE SHIPMENT (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	5.5
B	31.4
C (± 0.1)	0.75

All dimensions are in mm.

VNB14NV04 / VND14NV04 / VND14NV04-1 / VNP14NV04 / VNS14NV04

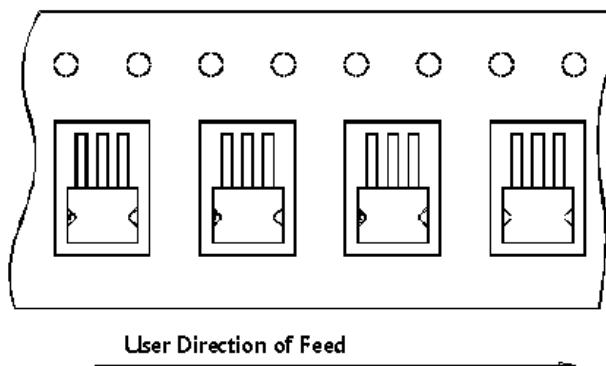


IPAk TUBE SHIPMENT (no suffix)

Base Q.ty	75
Bulk Q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

MECHANICAL POLARIZATION



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