



VND830PEP-E

DOUBLE CHANNEL HIGH SIDE DRIVER

Table 1. General Features

TYPE	R _{DS(on)}	I _{OUT}	V _{CC}
VND830PEP-E	60 mΩ (*)	6.0 A (*)	36 V

(*) Per each channel

- CMOS COMPATIBLE INPUTS
- OPEN DRAIN STATUS OUTPUTS
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (**)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

DESCRIPTION

The VND830PEP-E is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Figure 1. Package



Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects open load condition both in on and off state. Output shorted to V_{CC} is detected in the off state. Device automatically turns off in case of ground pin disconnection.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSSO-24	VND830PEP-E	VND830PEPTR-E

Note: (**) See application schematic at page 9

Figure 2. Block Diagram

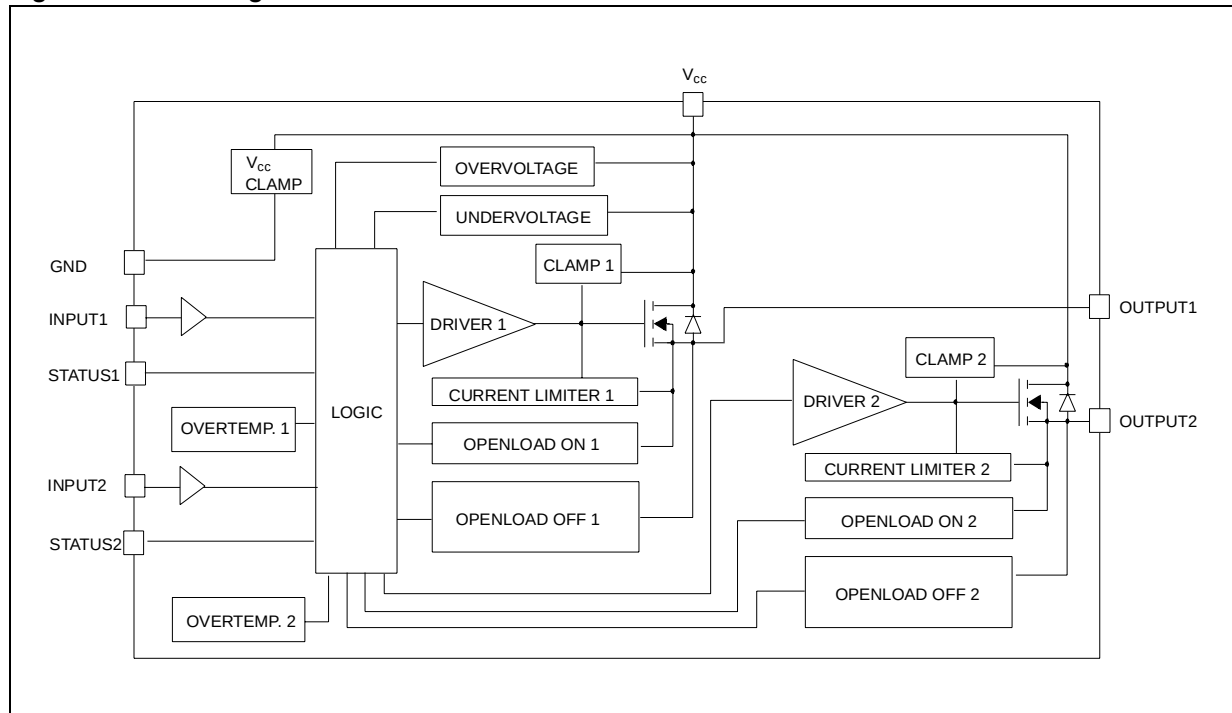
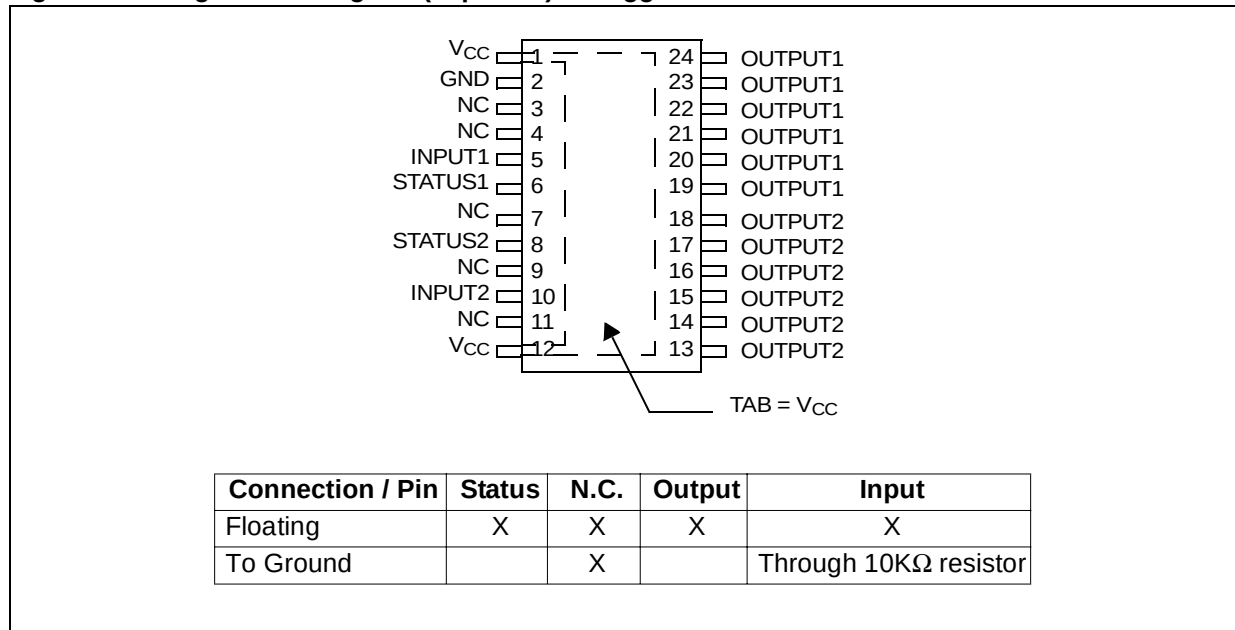
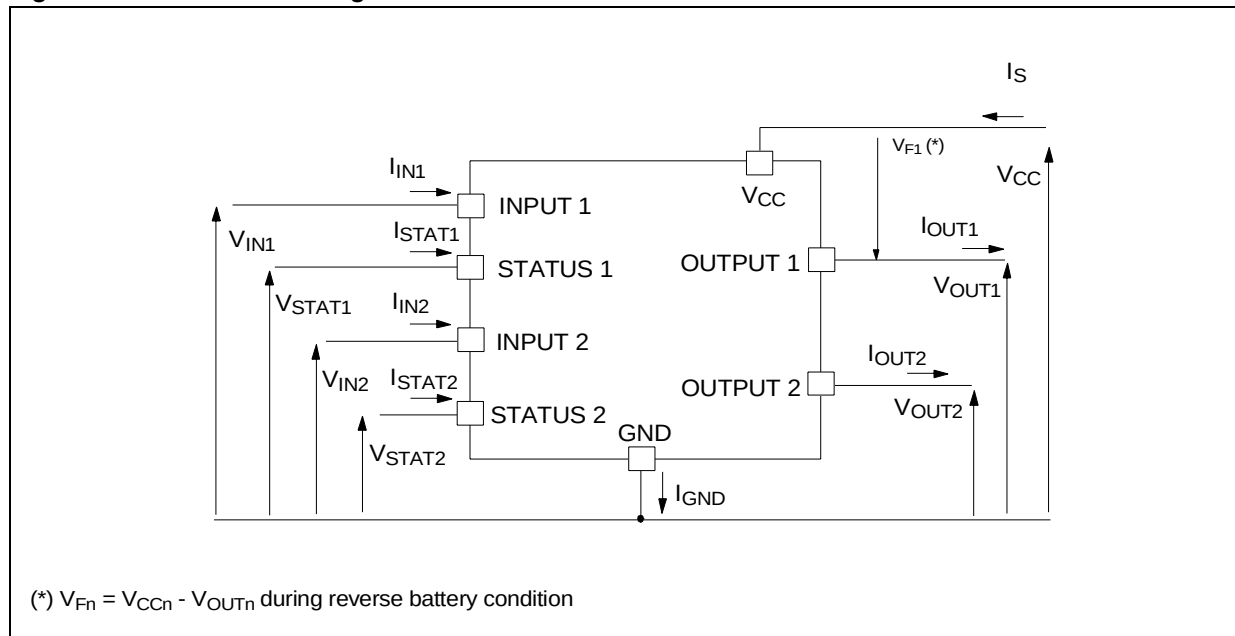


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	41	V
$-V_{CC}$	Reverse DC Supply Voltage	- 0.3	V
$-I_{GND}$	DC Reverse Ground Pin Current	- 200	mA
I_{OUT}	DC Output Current	Internally Limited	A
$-I_{OUT}$	Reverse DC Output Current	- 6	A
I_{IN}	DC Input Current	+/- 10	mA
I_{stat}	DC Status Current	+/- 10	mA
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5K Ω ; C=100pF)		
	- INPUT	4000	V
	- STATUS	4000	V
	- OUTPUT	5000	V
	- V_{CC}	5000	V
P_{tot}	Power Dissipation $T_C=25^{\circ}C$	54	W
T_j	Junction Operating Temperature	Internally Limited	$^{\circ}C$
T_C	Case Operating Temperature	- 40 to 150	$^{\circ}C$
T_{stg}	Storage Temperature	- 55 to 150	$^{\circ}C$

Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins**Figure 4. Current and Voltage Conventions****Table 4. Thermal Data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX)	2.3	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (MAX)	57 (*) 42 (**)	°C/W

Note: (*) When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick) connected to all V_{CC} pins.

Note: (**) When mounted on a standard single-sided FR-4 board with 8cm² of Cu (at least 35μm thick) connected to all V_{CC} pins.

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C unless otherwise specified)

(Per each channel)

Table 5. Power Outputs

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{CC}	Operating Supply Voltage		5.5	13	36	V
V _{USD}	Undervoltage Shut-down		3	4	5.5	V
V _{OV}	Overvoltage Shut-down		36			V
R _{ON}	On State Resistance	I _{OUT} =2A; T _j =25°C I _{OUT} =2A; V _{CC} >8V			60 120	mΩ mΩ
I _S	Supply Current	Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V; T _j =25°C On State; V _{CC} =13V; V _{IN} =5V; I _{OUT} =0A		12 12 5	40 25 7	μA μA mA
I _{L(off1)}	Off State Output Current	V _{IN} =V _{OUT} =0V	0		50	μA
I _{L(off2)}	Off State Output Current	V _{IN} =0V; V _{OUT} =3.5V	-75		0	μA
I _{L(off3)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =125°C			5	μA
I _{L(off4)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =25°C			3	μA

Table 6. Switching (V_{CC} =13V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	R _L =6.5Ω from V _{IN} rising edge to V _{OUT} =1.3V		30		μs
t _{d(off)}	Turn-on delay time	R _L =6.5Ω from V _{IN} falling edge to V _{OUT} =11.7V		30		μs
(dV _{OUT} /dt) _{on}	Turn-on voltage slope	R _L =6.5Ω from V _{OUT} =1.3V to V _{OUT} =10.4V		See relative diagram		V/μs
(dV _{OUT} /dt) _{off}	Turn-off voltage slope	R _L =6.5Ω from V _{OUT} =11.7V to V _{OUT} =1.3V		See relative diagram		V/μs

Table 7. V_{CC} - Output Diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _F	Forward on Voltage	-I _{OUT} =1.3A; T _j =150°C			0.6	V

Table 8. Status Pin

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{STAT}	Status Low Output Voltage	I _{STAT} = 1.6 mA			0.5	V
I _{LSTAT}	Status Leakage Current	Normal Operation; V _{STAT} = 5V			10	μA
C _{STAT}	Status Pin Input Capacitance	Normal Operation; V _{STAT} = 5V			100	pF
V _{SCL}	Status Clamp Voltage	I _{STAT} = 1mA I _{STAT} = - 1mA	6	6.8 -0.7	8	V V

ELECTRICAL CHARACTERISTICS (continued)**Table 9. Logic Input**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	$V_{IN} = 1.25V$	1			μA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	$V_{IN} = 3.25V$			10	μA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
V_{ICL}	Input Clamp Voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	6	6.8 -0.7	8	V V

Table 10. Protections (See note 1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shut-down Temperature		150	175	200	$^{\circ}C$
T_R	Reset Temperature		135			$^{\circ}C$
T_{hyst}	Thermal Hysteresis		7	15		$^{\circ}C$
t_{SDL}	Status Delay in Overload Conditions	$T_j > T_{TSD}$			20	μs
I_{lim}	Current limitation	$5.5V < V_{CC} < 36V$	6	9	15 15	A A
V_{demag}	Turn-off Output Clamp Voltage	$I_{OUT} = 2A$; $L = 6mH$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V

Note: 1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 11. Openload Detection

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	$V_{IN} = 5V$	50	100	200	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	$I_{OUT} = 0A$			200	μs
V_{OL}	Openload OFF State Voltage Detection Threshold	$V_{IN} = 0V$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	μs

Figure 5.

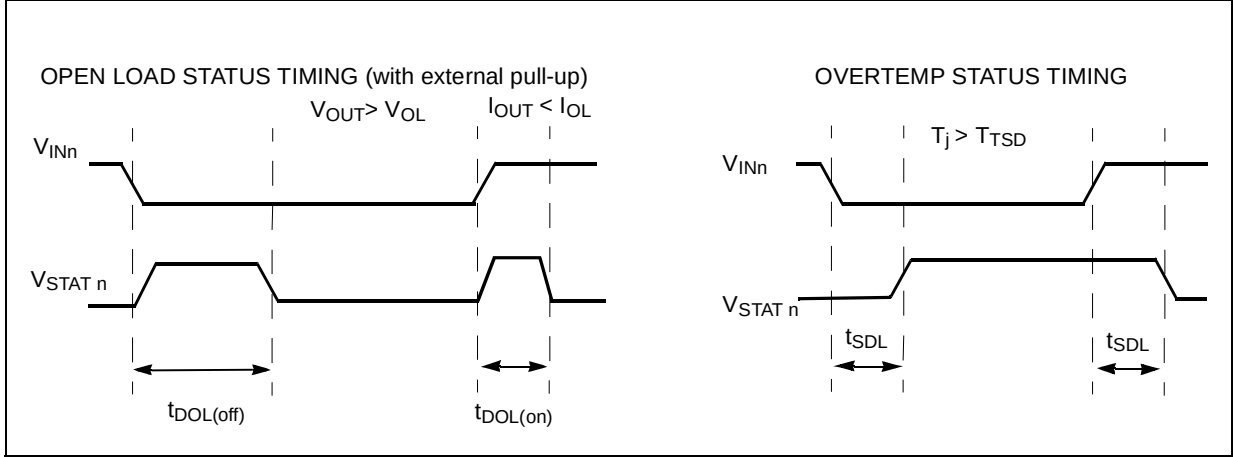


Figure 6. Switching time Waveforms

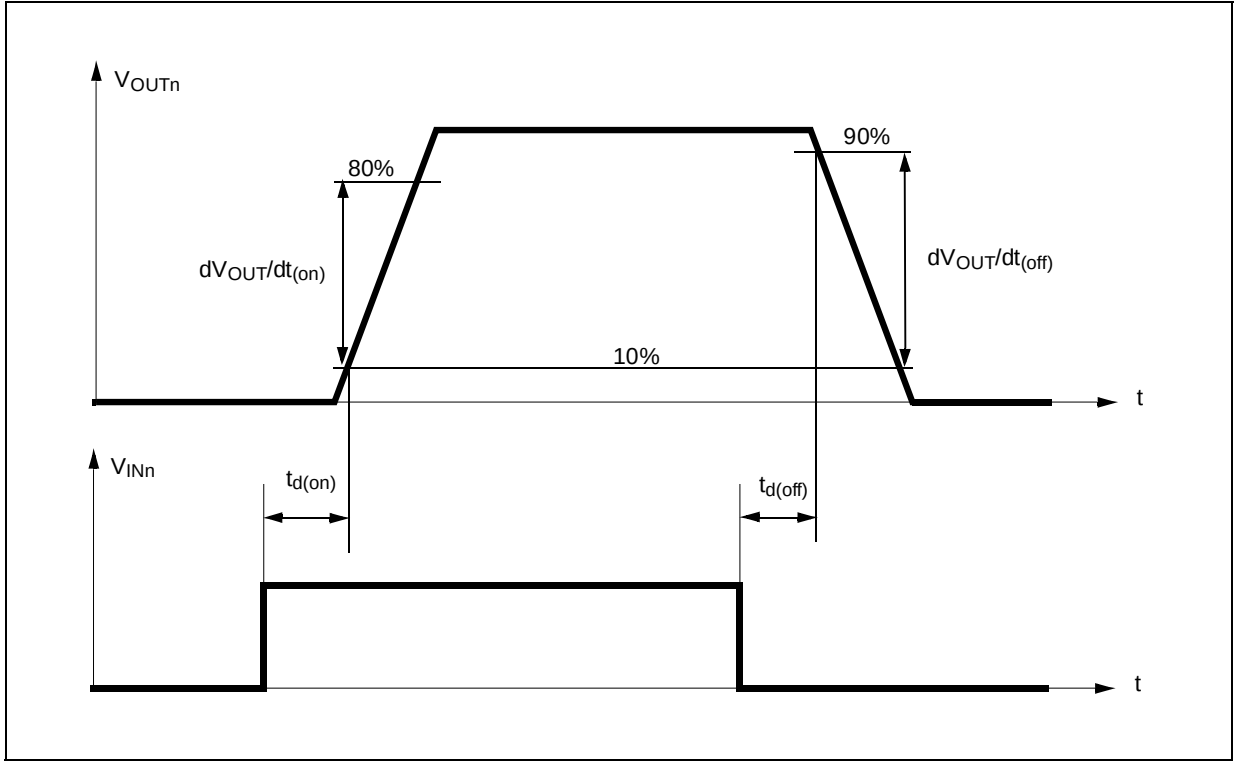


Table 12. Truth Table

CONDITIONS	INPUT _n	OUTPUT _n	STATUS _n
Normal Operation	L H	L H	H H
Current Limitation	L H H	L X X	H (T _j < T _{TSD}) H (T _j > T _{TSD}) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output Voltage > V _{OLn}	L H	H H	L H
Output Current < I _{OLn}	L H	L H	H L

Table 13. Electrical Transient Requirements on V_{CC} Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms

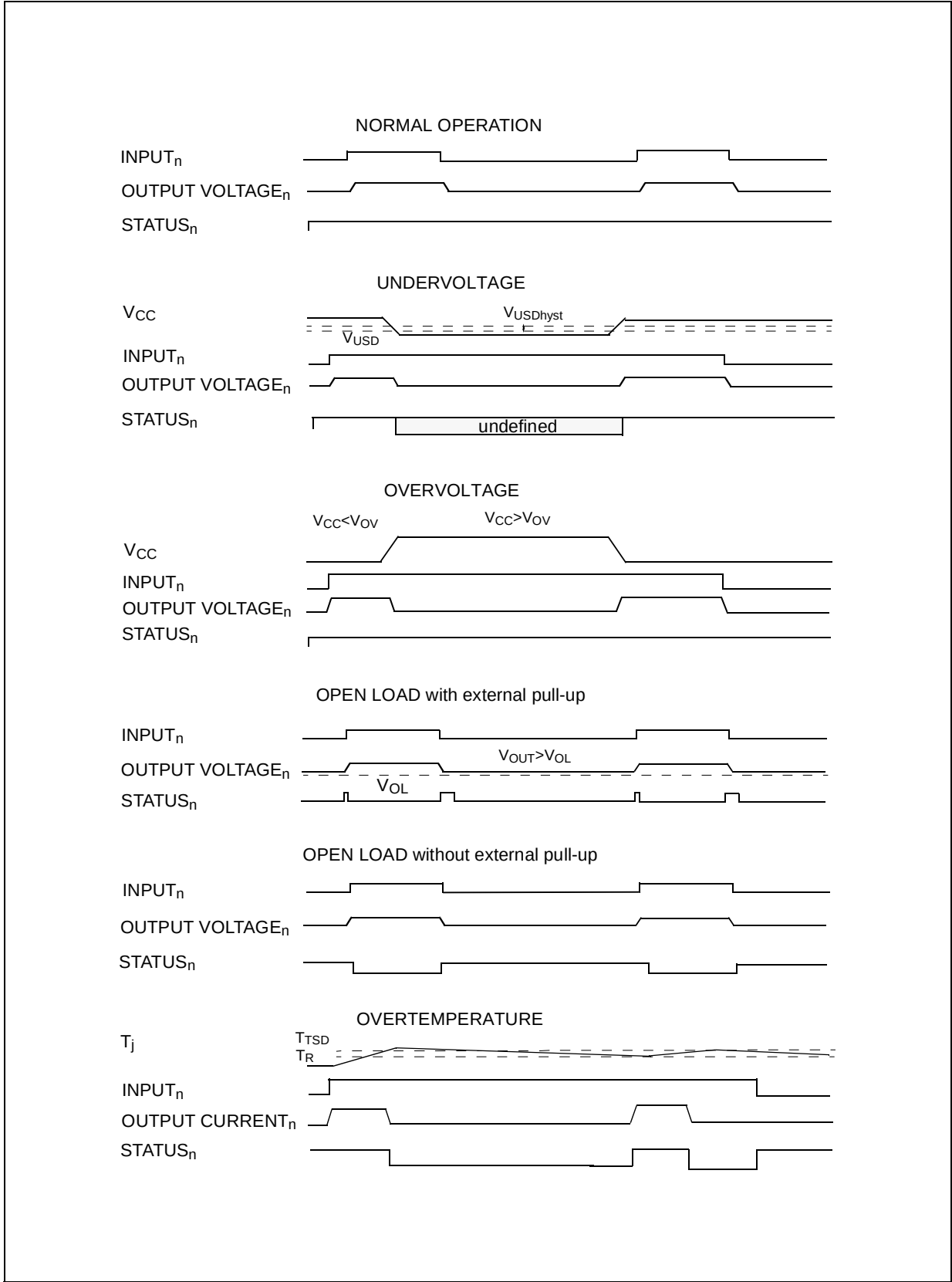
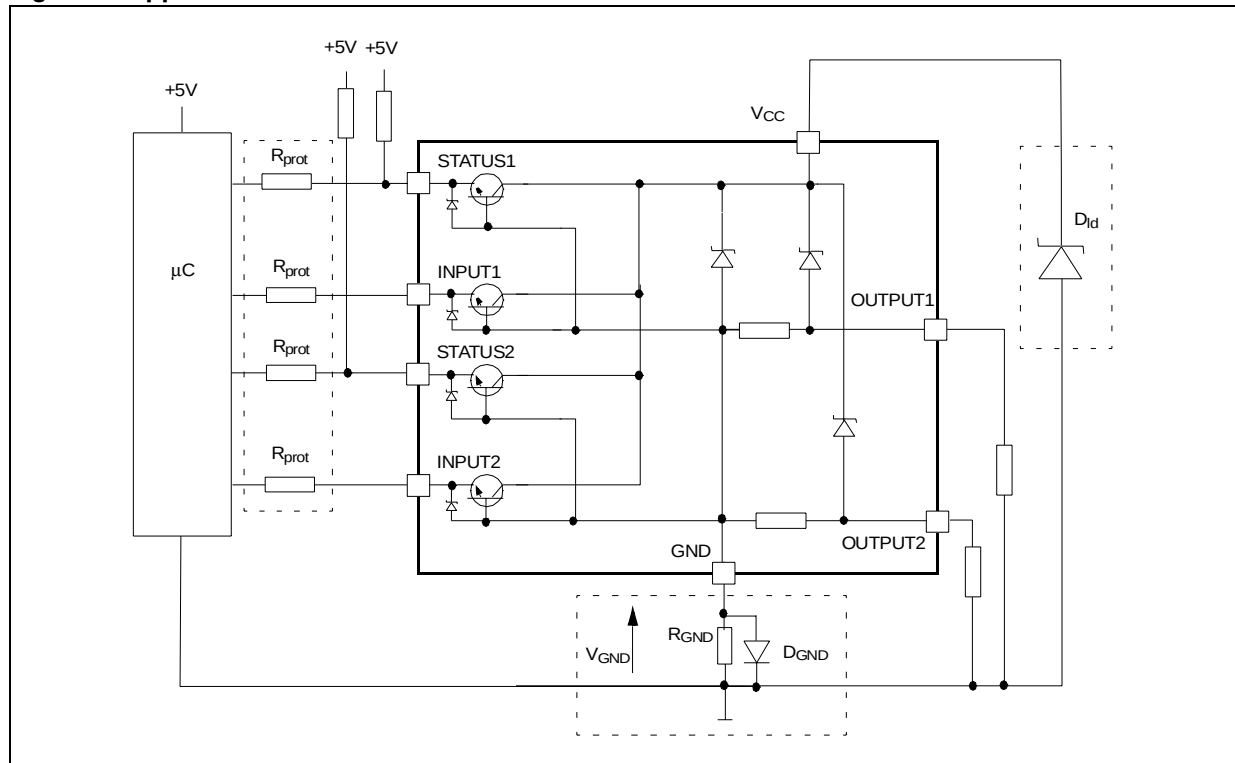


Figure 8. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND}=1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of

the ground network will produce a shift ($\approx 600\text{mV}$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

LOAD DUMP PROTECTION

D_{id} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

μC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$
 $5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega$.

Recommended R_{prot} value is $10\text{k}\Omega$.

1) no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{OLmin} ; this results in the following condition $V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$.

The values of V_{OLmin} , V_{OLmax} and $I_{L(off2)}$ are available in the Electrical Characteristics section.

Figure 9. Open Load detection in off state

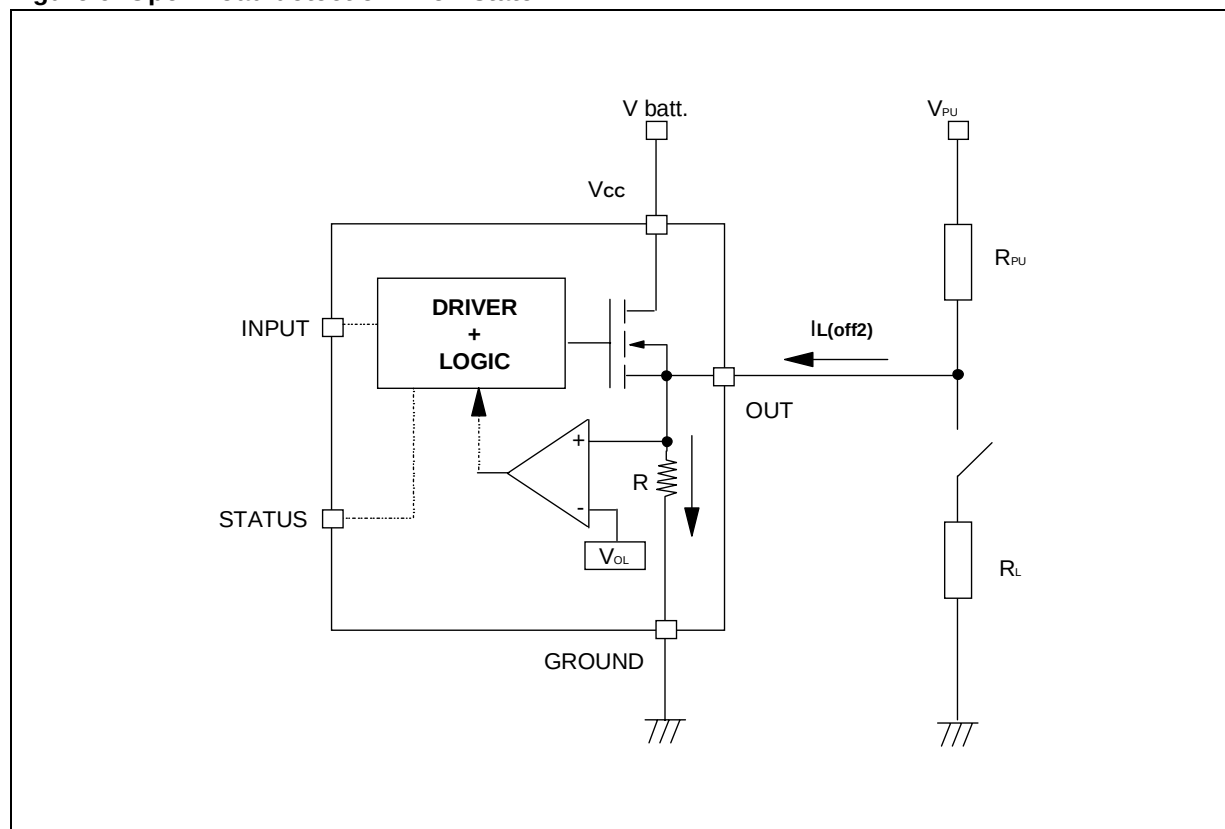


Figure 10. Off State Output Current

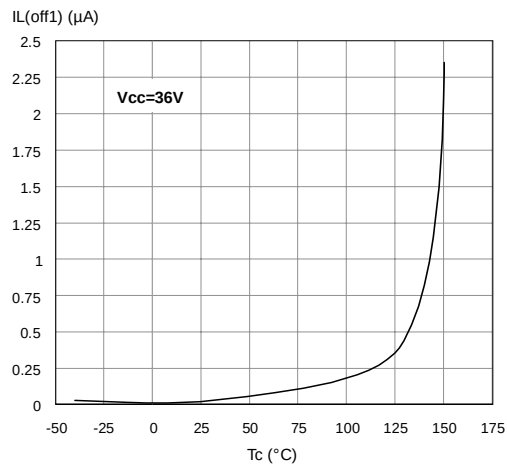


Figure 11. High Level Input Current

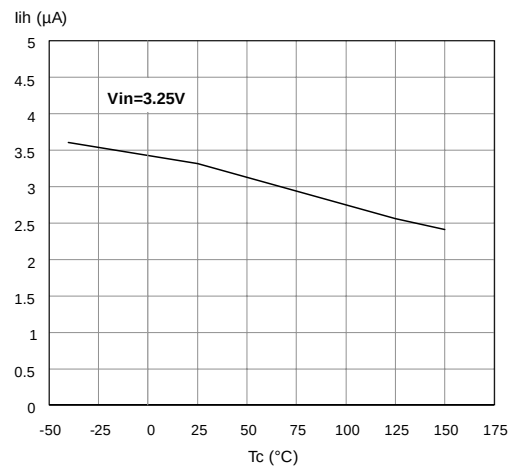


Figure 12. Input Clamp Voltage

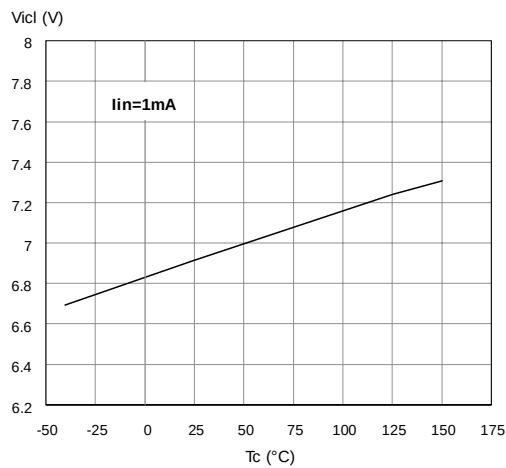


Figure 14. Status Leakage Current

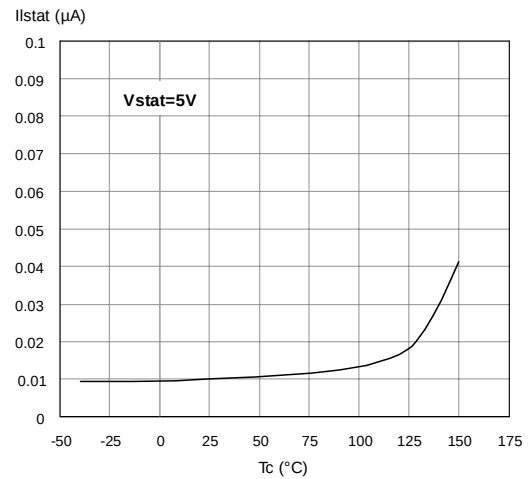


Figure 13. Status Low Output Voltage

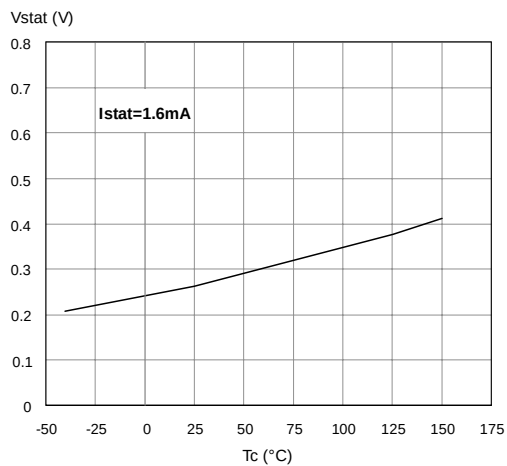


Figure 15. Status Clamp Voltage

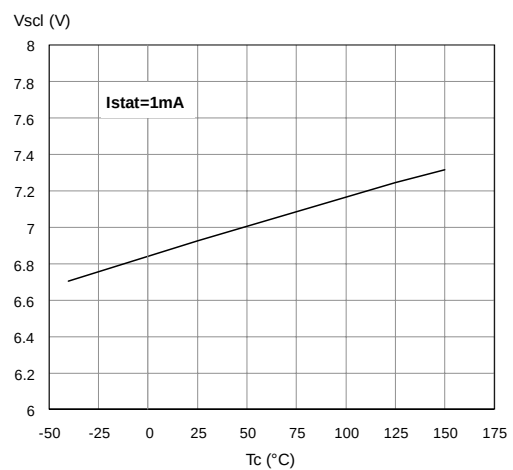


Figure 16. Turn-on Voltage Slope

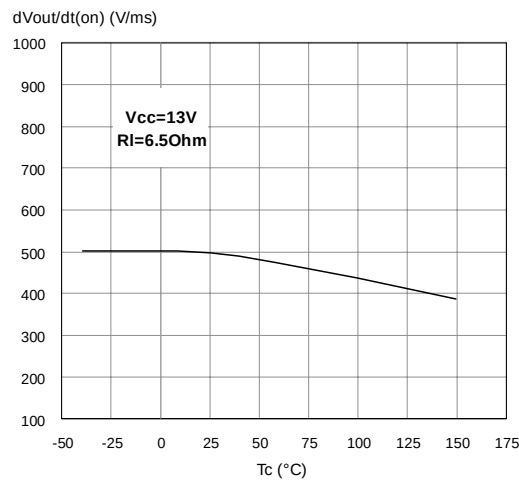


Figure 19. Turn-off Voltage Slope

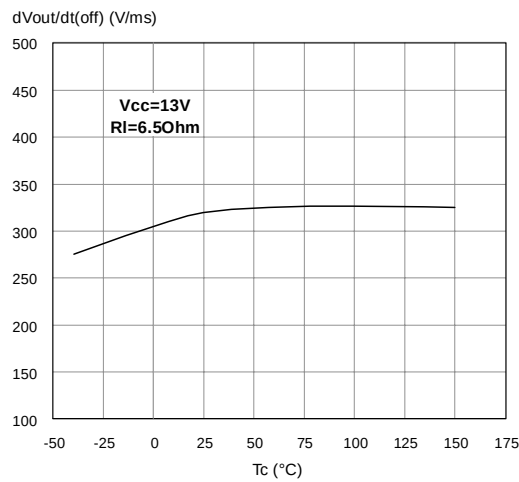


Figure 17. On State Resistance Vs T_{case}

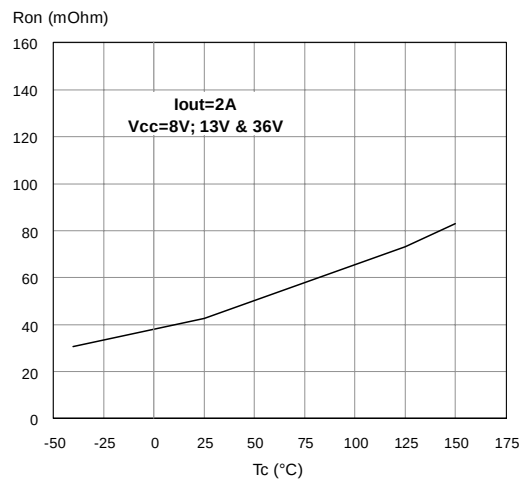


Figure 20. On State Resistance Vs V_{CC}

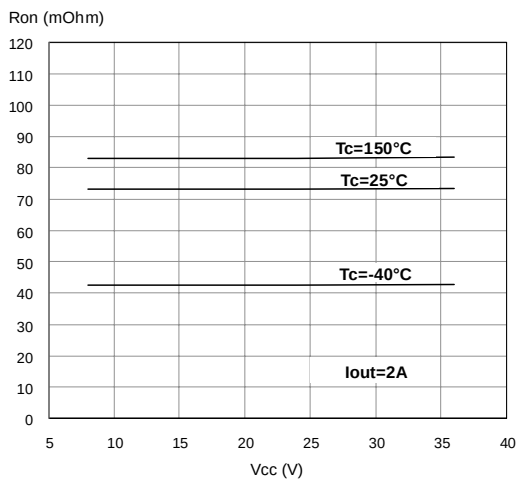


Figure 18. I_{LIM} Vs T_{case}

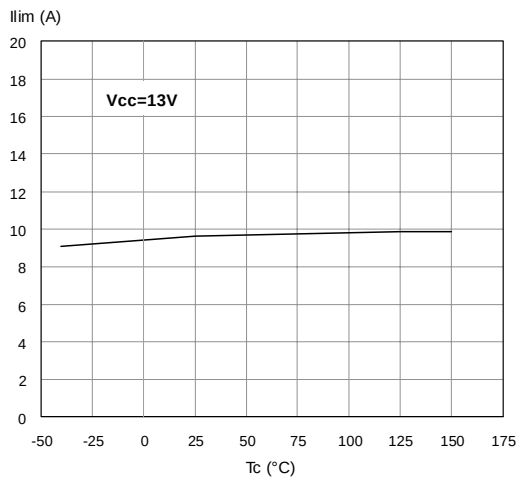


Figure 21. Input High Level

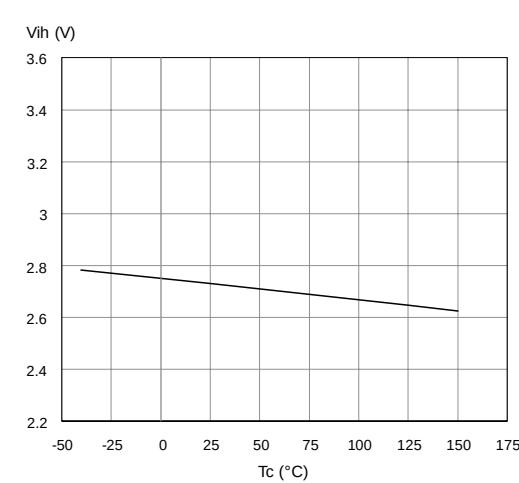
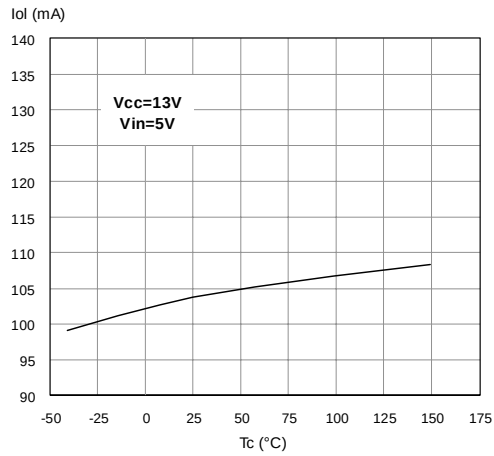
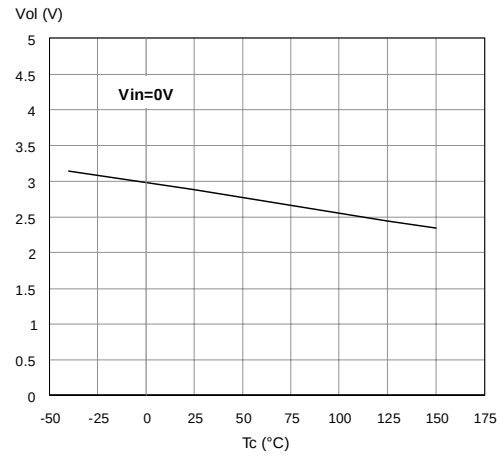
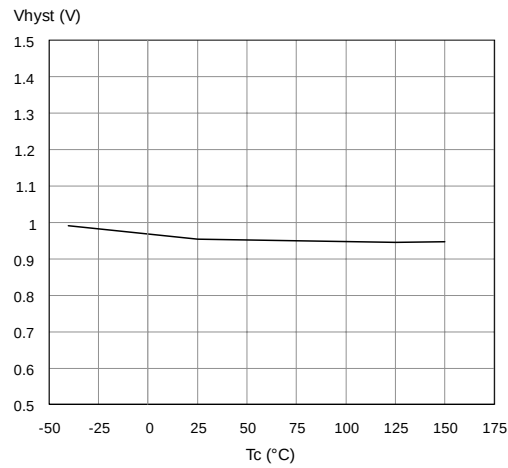
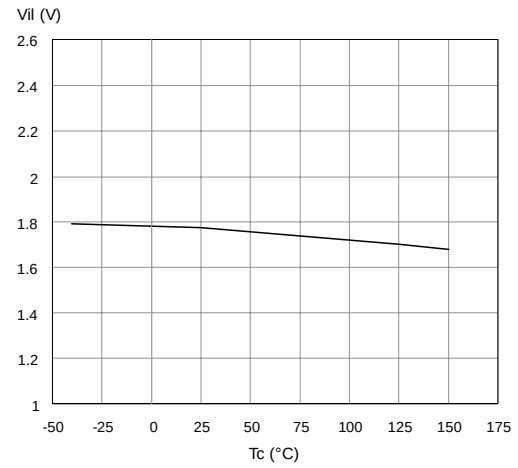
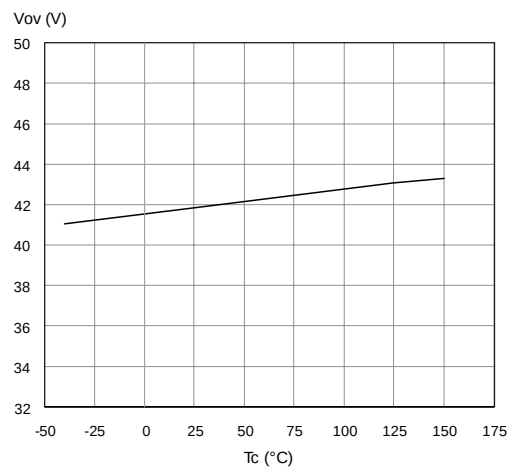
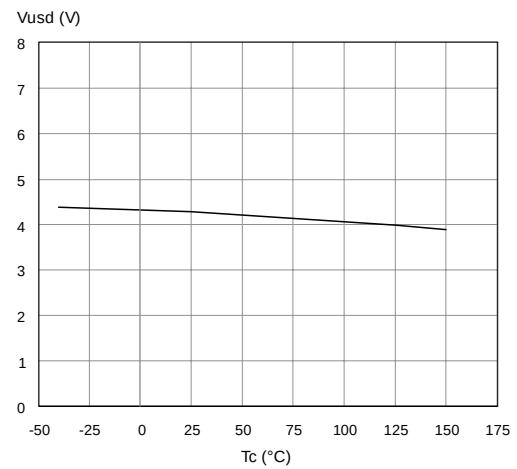


Figure 22. Openload On State Detection Threshold**Figure 25. Openload Off State Detection Threshold****Figure 23. Input Hysteresis Voltage****Figure 26. Input Low Level****Figure 24. Overvoltage Shutdown****Figure 27. Undervoltage Shutdown**

PowerSSO-24 Thermal Data

Figure 28. PowerSSO-24 PC Board

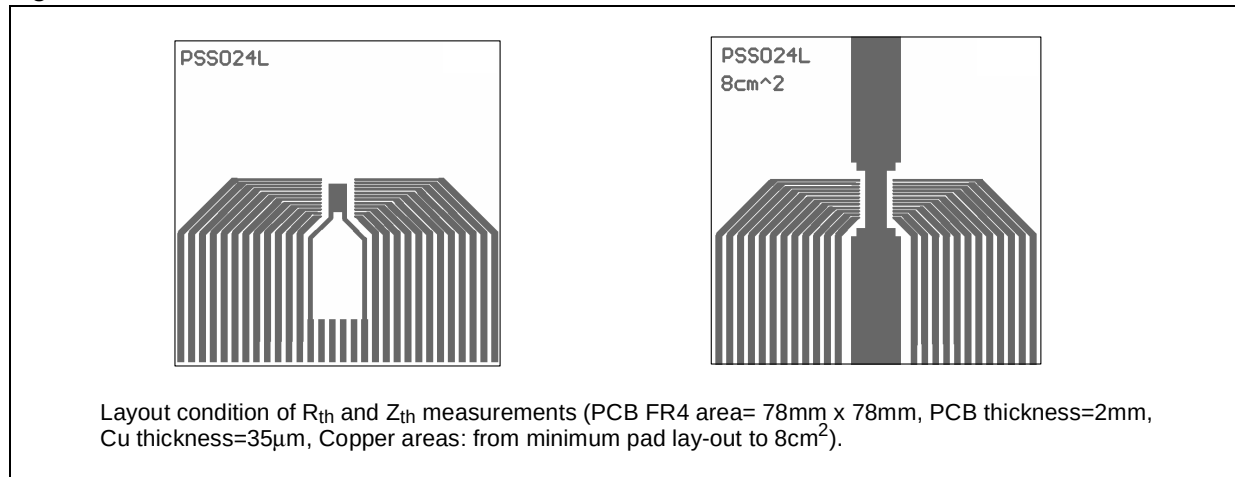
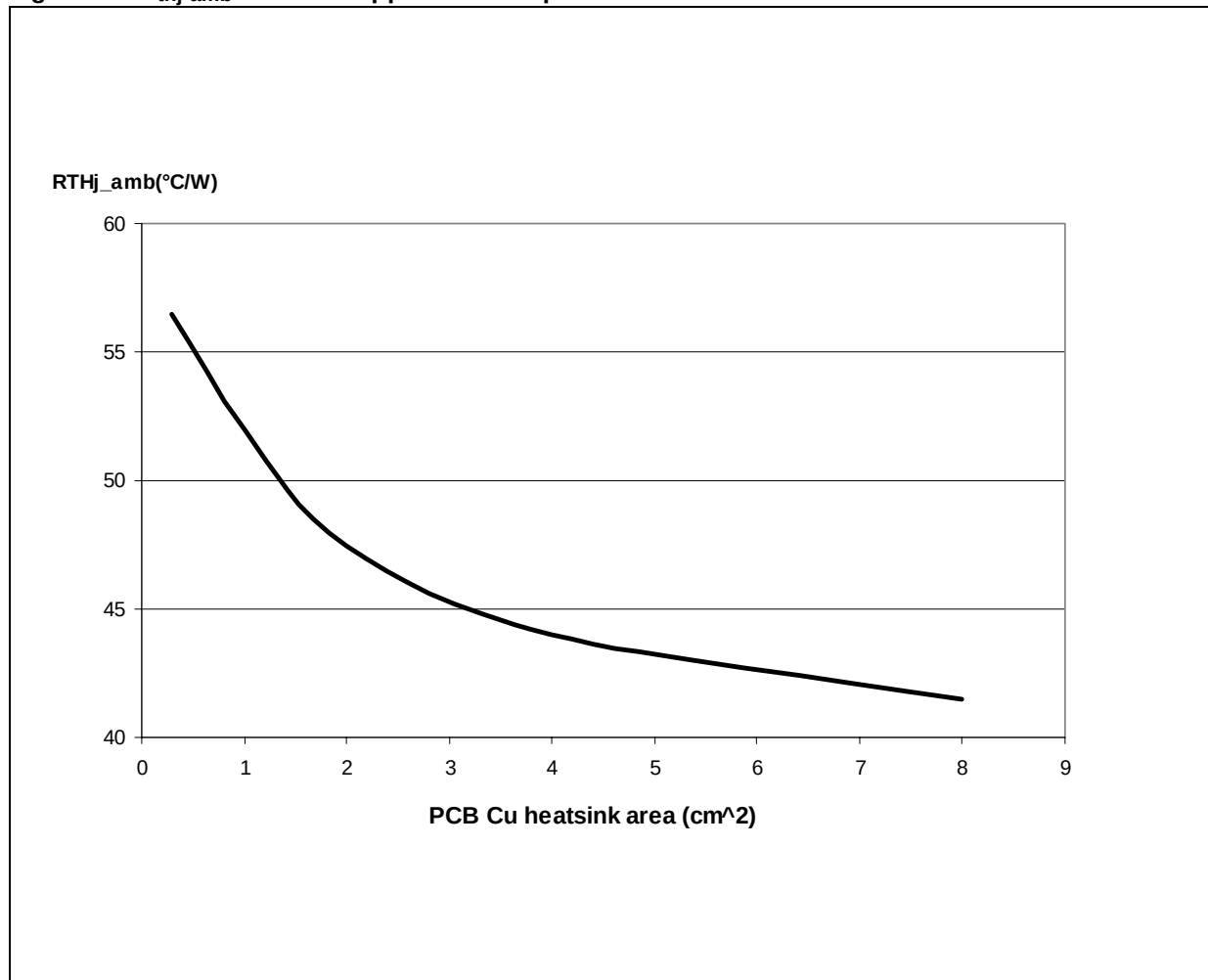
Figure 29. $R_{thj-amb}$ Vs PCB copper area in open box free air condition

Figure 30. PowerSSO-24 Thermal Impedance Junction Ambient Single Pulse

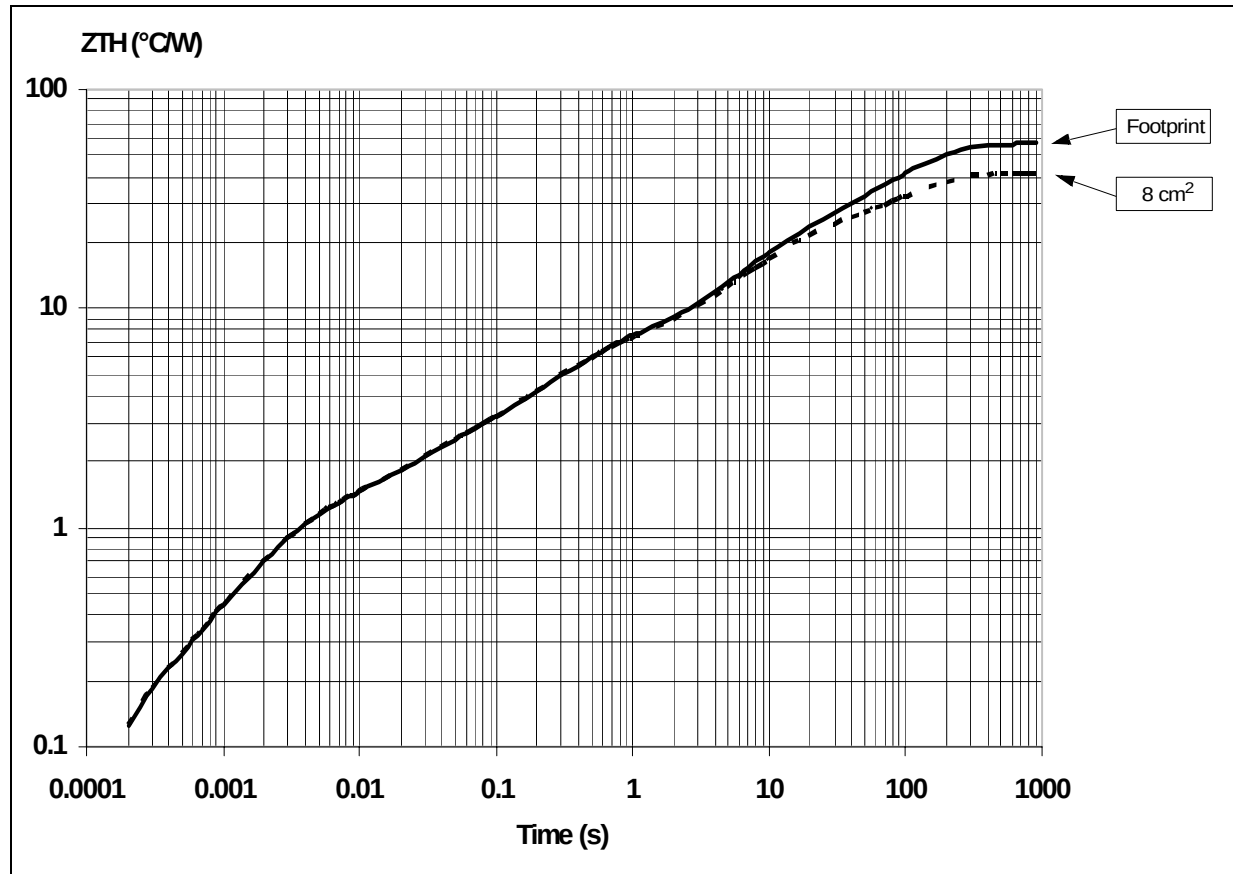
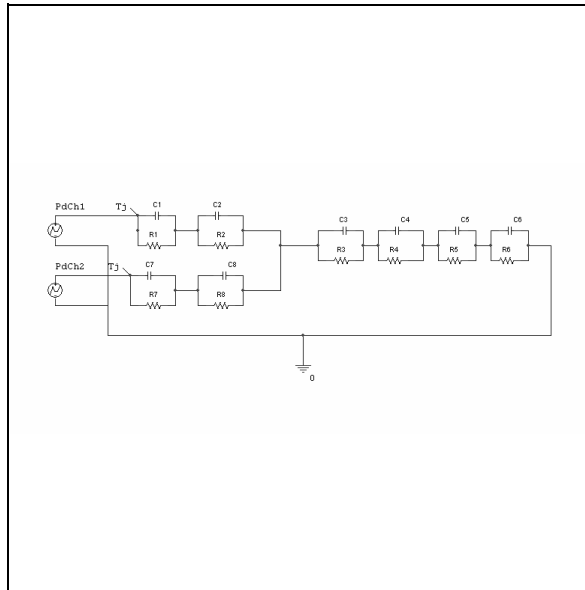


Figure 31. Thermal Fitting Model of a Double Channel HSD in PowerSSO-24

**Pulse Calculation Formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

Table 14. Thermal Parameter

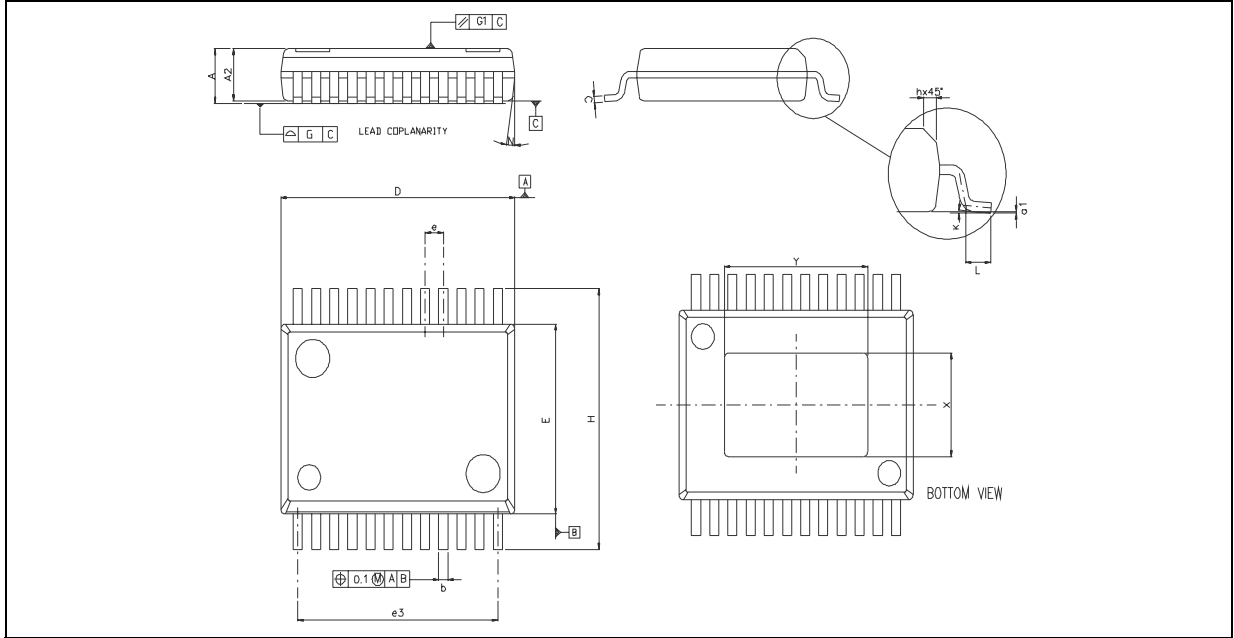
Area/island (cm ²)	Footprint	8
R1/R7(°C/W)	0.1	
R2/R8(°C/W)	0.9	
R3(°C/W)	1	
R4(°C/W)	4	
R5(°C/W)	13.5	
R6(°C/W)	37	22
C1/C7(W.s/°C)	0.0006	
C2/C8(W.s/°C)	0.0025	
C3(W.s/°C)	0.025	
C4(W.s/°C)	0.08	
C5(W.s/°C)	0.7	
C6(W.s/°C)	3	5

PACKAGE MECHANICAL

Table 15. PowerSSO-24™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

Figure 32. PowerSSO-24™ Package Dimensions



REVISION HISTORY**Table 16. Revision History**

Date	Revision	Description of Changes
Oct. 2004	1	- First Issue.
Nov. 2004	2	- Mechanical data updating. - PowerSSO-24 Thermal Charact. insertion
Nov. 2004	3	- PC Board copper area correction.
Dec. 2004	4	- Electrical Charact. insertion. - Absolute maximum ratings modification.

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