



VN920PEP-E

SINGLE CHANNEL HIGH SIDE DRIVER

Table 1. General Features

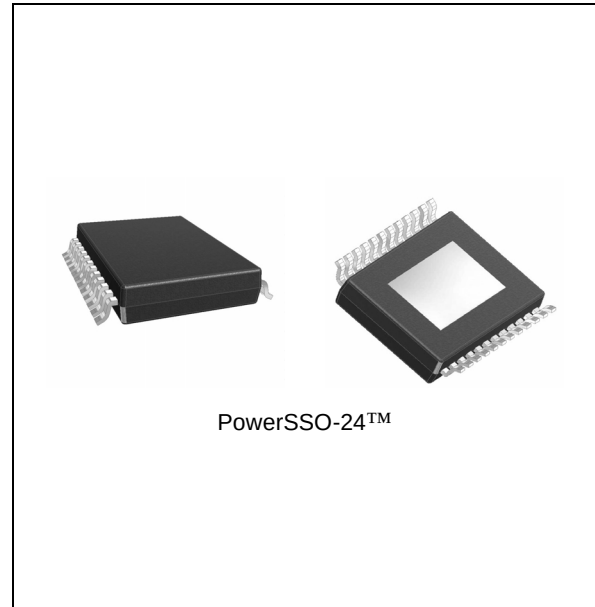
TYPE	R _{DS(on)}	I _{OUT}	V _{CC}
VN920PEP-E	15mΩ	30 A	36 V

- CMOS COMPATIBLE INPUT
- PROPORTIONAL LOAD CURRENT SENSE
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUTDOWN
- CURRENT LIMITATION
- PROTECTION AGAINST LOSS OF GROUND AND LOSS V_{CC}
- VERY LOW STAND-BY POWER DISSIPATION
- REVERSE BATTERY PROTECTION (*)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

DESCRIPTION

The VN920PEP-E is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Figure 1. Package



Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device integrates an analog current sense output which delivers a current proportional to the load current. Device automatically turns off in case of ground pin disconnection.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSSO-24	VN920PEP-E	VN920PEPTR-E

Note: (*) See application schematic at page 10

Figure 2. Block Diagram

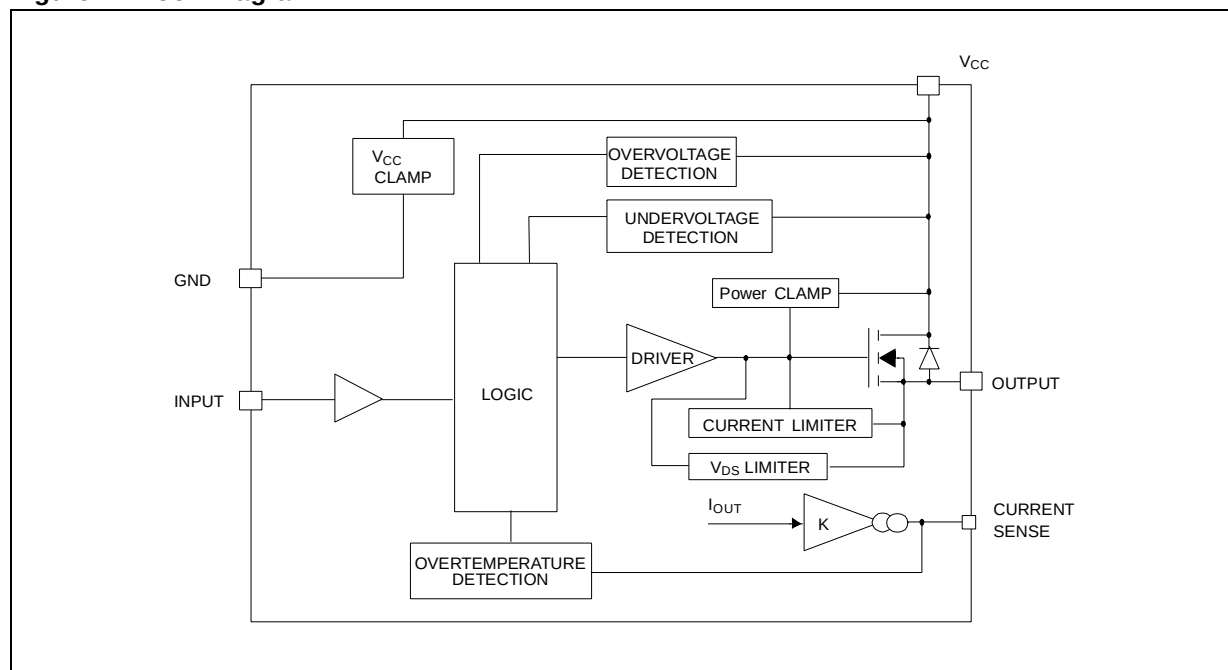
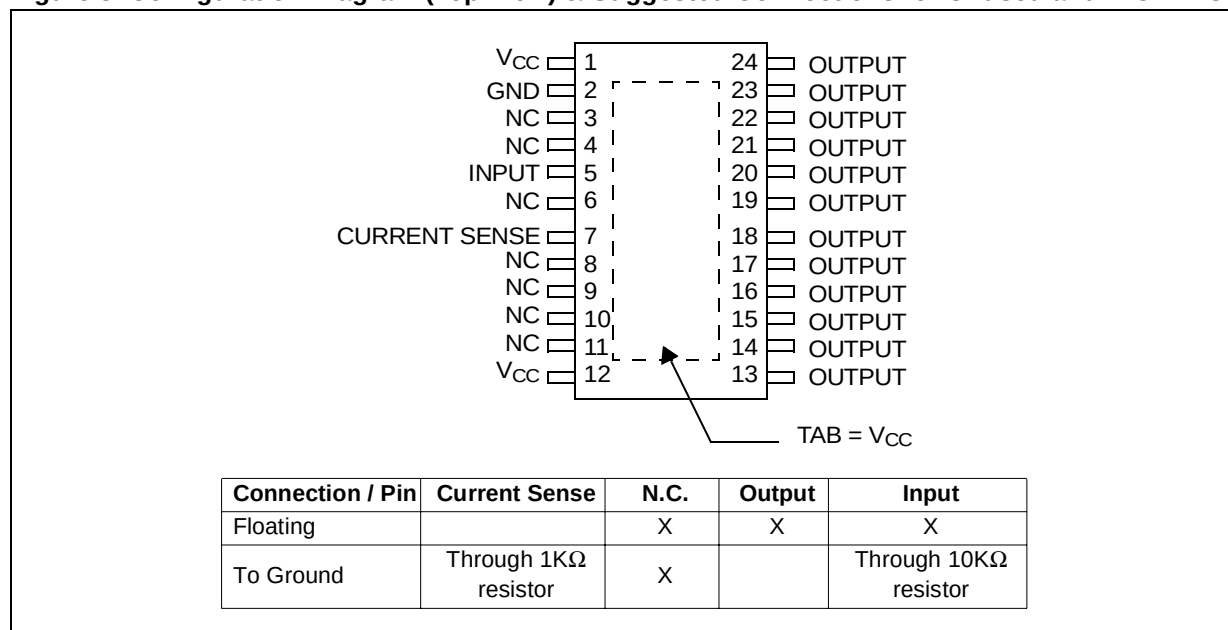
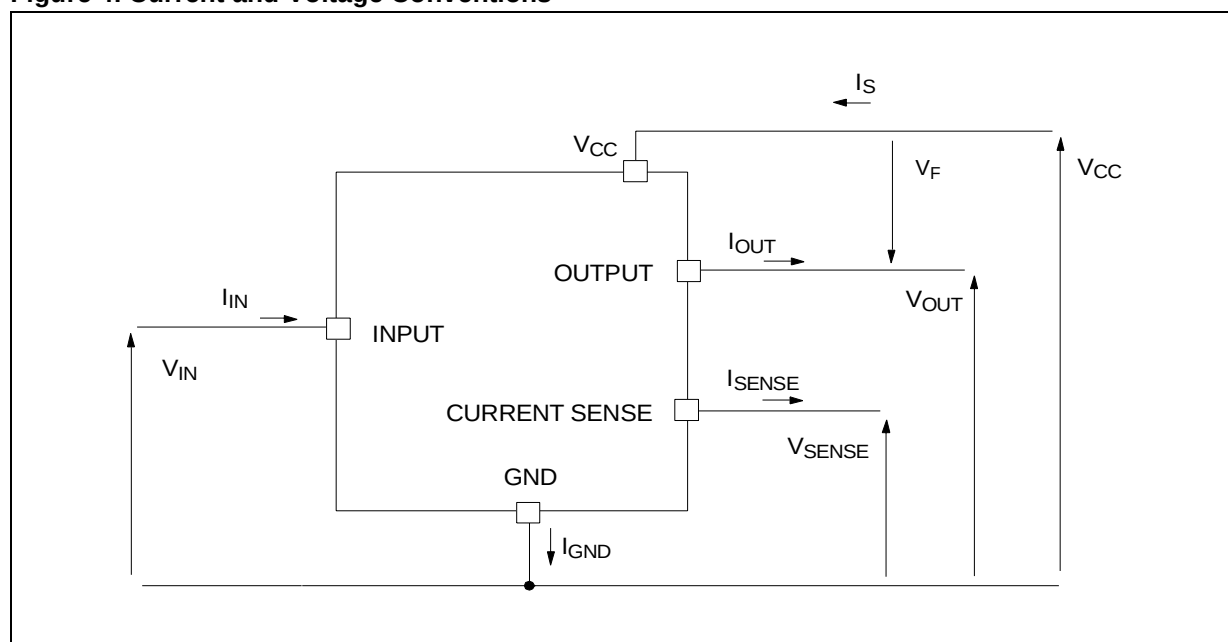


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	41	V
- V _{CC}	Reverse DC Supply Voltage	- 0.3	V
- I _{GND}	DC Reverse Ground Pin Current	- 200	mA
I _{OUT}	DC Output Current	Internally Limited	A
- I _{OUT}	Reverse DC Output Current	- 40	A
I _{IN}	DC Input Current	+/- 10	mA
V _{CSense}	Current Sense Maximum Voltage	-3 +15	V V
V _{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - CURRENT SENSE - OUTPUT - V _{CC}	4000 2000 5000 5000	V V V V
E _{MAX}	Maximum Switching Energy (L=0.3mH; R _L =0Ω; V _{bat} =13.5V; T _{jstart} =150°C; I _L =45A)	462	mJ
P _{tot}	Power Dissipation T _C ≤25°C	96	W
T _j	Junction Operating Temperature	Internally limited	°C
T _C	Case Operating Temperature	- 40 to 150	°C
T _{STG}	Storage Temperature	- 55 to 150	°C

Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins**Figure 4. Current and Voltage Conventions****Table 4. Thermal Data**

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal Resistance Junction-case	Max 1.3	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max 55 ⁽¹⁾ 40 ⁽²⁾	°C/W

Note: (1) When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35 μ m thick).

Note: (2) When mounted on a standard single-sided FR-4 board with 8cm² of Cu (at least 35 μ m thick).

ELECTRICAL CHARACTERISTICS ($8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$ unless otherwise specified)**Table 5. Power**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Supply Voltage		5.5	13	36	V
V_{USD}	Undervoltage Shut-down		3	4	5.5	V
V_{OV}	Overvoltage Shut-down		36			V
R_{ON}	On State Resistance	$I_{OUT}=10A$; $T_j=25^{\circ}C$			15	m Ω
		$I_{OUT}=10A$			30	m Ω
		$I_{OUT}=3A$; $V_{CC}=6V$			50	m Ω
V_{clamp}	Clamp Voltage	$I_{CC}=20mA$ (See note 1)	41	48	55	V
I_S	Supply Current	Off State; $V_{CC}=13V$; $V_{IN}=V_{OUT}=0V$		10	25	μA
		Off State; $V_{CC}=13V$; $T_j=25^{\circ}C$; $V_{IN}=V_{OUT}=0V$		10	20	μA
		On State; $V_{CC}=13V$; $V_{IN}=5V$; $I_{OUT}=0$; $R_{SENSE}=3.9K\Omega$			5	mA
$I_{L(off1)}$	Off State Output Current	$V_{IN}=V_{OUT}=V_{SENSE}=0V$	0		50	μA
$I_{L(off3)}$	Off State Output Current	$V_{IN}=V_{OUT}=V_{SENSE}=0V$; $V_{CC}=13V$; $T_j=125^{\circ}C$			5	μA
$I_{L(off4)}$	Off State Output Current	$V_{IN}=V_{OUT}=V_{SENSE}=0V$; $V_{CC}=13V$; $T_j=25^{\circ}C$			3	μA

Note: 1. V_{clamp} and V_{OV} are correlated. Typical difference is 5V.**Table 6. Switching** ($V_{CC}=13V$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$R_L=1.3\Omega$ (see figure 2)		50		μs
$t_{d(off)}$	Turn-off Delay Time	$R_L=1.3\Omega$ (see figure 2)		50		μs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	$R_L=1.3\Omega$ (see figure 2)		See relative diagram		V/ μs
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	$R_L=1.3\Omega$ (see figure 2)		See relative diagram		V/ μs

Table 7. Logic Input

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	$V_{IN}=1.25V$	1			μA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	$V_{IN}=3.25V$			10	μA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
V_{ICL}	Input Clamp Voltage	$I_{IN}=1mA$	6	6.8	8	V
		$I_{IN}=-1mA$		-0.7		V

ELECTRICAL CHARACTERISTICS (continued)**Table 8. Current Sense** ($9V \leq V_{CC} \leq 16V$) (See figure 5)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	$I_{OUT}=1A$; $V_{SENSE}=0.5V$; $T_j = -40^\circ C \dots 150^\circ C$	3300	4400	6000	
dK_1/K_1	Current Sense Ratio Drift	$I_{OUT}=1A$; $V_{SENSE}=0.5V$; $T_j = -40^\circ C \dots +150^\circ C$	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	$I_{OUT}=10A$; $V_{SENSE}=4V$; $T_j = -40^\circ C$ $T_j = 25^\circ C \dots 150^\circ C$	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current Sense Ratio Drift	$I_{OUT}=10A$; $V_{SENSE}=4V$; $T_j = -40^\circ C \dots +150^\circ C$	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	$I_{OUT}=30A$; $V_{SENSE}=4V$; $T_j = -40^\circ C$ $T_j = 25^\circ C \dots 150^\circ C$	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current Sense Ratio Drift	$I_{OUT}=30A$; $V_{SENSE}=4V$; $T_j = -40^\circ C \dots +150^\circ C$	-6		+6	%
I_{SENSEO}	Analog Sense Leakage Current	$V_{CC}=6 \dots 16V$; $I_{OUT}=0A$; $V_{SENSE}=0V$; $T_j = -40^\circ C \dots +150^\circ C$	0		10	μA
V_{SENSE}	Max Analog Sense Output Voltage	$V_{CC}=5.5V$; $I_{OUT}=5A$; $R_{SENSE}=10K\Omega$ $V_{CC}>8V$; $I_{OUT}=10A$; $R_{SENSE}=10K\Omega$	2 4			V V
V_{SENSEH}	Sense Voltage in Overtemperature conditions	$V_{CC}=13V$; $R_{SENSE}=3.9K\Omega$		5.5		V
$R_{VSENSEH}$	Analog sense output impedance in overtemperature condition	$V_{CC}=13V$; $T_j > T_{TSD}$; Output Open		400		Ω
t_{DSENSE}	Current sense delay response	to 90% I_{SENSE} (see note 2)			500	μs

Note: 2. Current sense signal delay after positive input slope

Table 9. Protections (See note 3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shut-down Temperature		150	175	200	$^\circ C$
T_R	Reset Temperature		135			$^\circ C$
T_{hyst}	Thermal Hysteresis		7	15		$^\circ C$
I_{lim}	DC Short Circuit Current	$V_{CC}=13V$ $5V < V_{CC} < 36V$	30	45	75 75	A A
V_{demag}	Turn-off Output Clamp Voltage	$I_{OUT}=2A$; $V_{IN}=0V$; $L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V
V_{ON}	Output Voltage Drop Limitation	$I_{OUT}=1A$; $T_j = -40^\circ C \dots +150^\circ C$		50		mV

Note: 3. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

ELECTRICAL CHARACTERISTICS (continued)

Table 10. V_{CC} - Output Diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_F	Forward on Voltage	$-I_{OUT}=5.3A$; $T_J=150^{\circ}C$			0.6	V

Figure 5. I_{OUT}/I_{SENSE} versus I_{OUT}

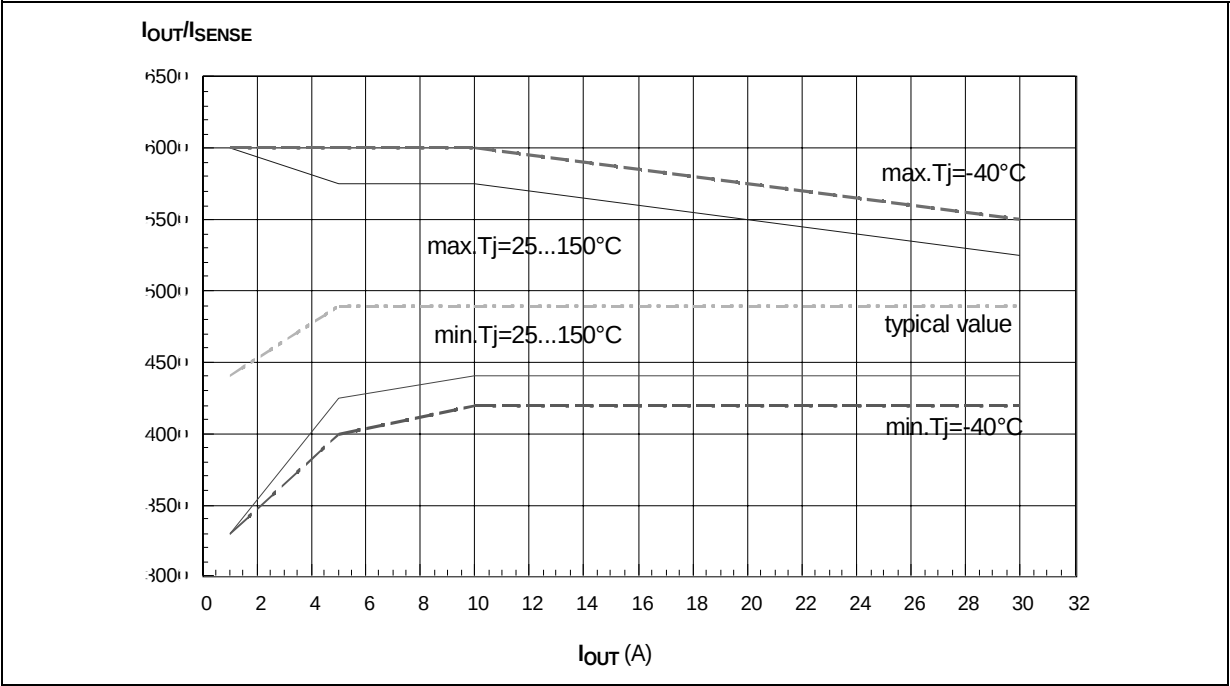


Figure 6. Switching Characteristics (Resistive load $R_L=1.3\Omega$)

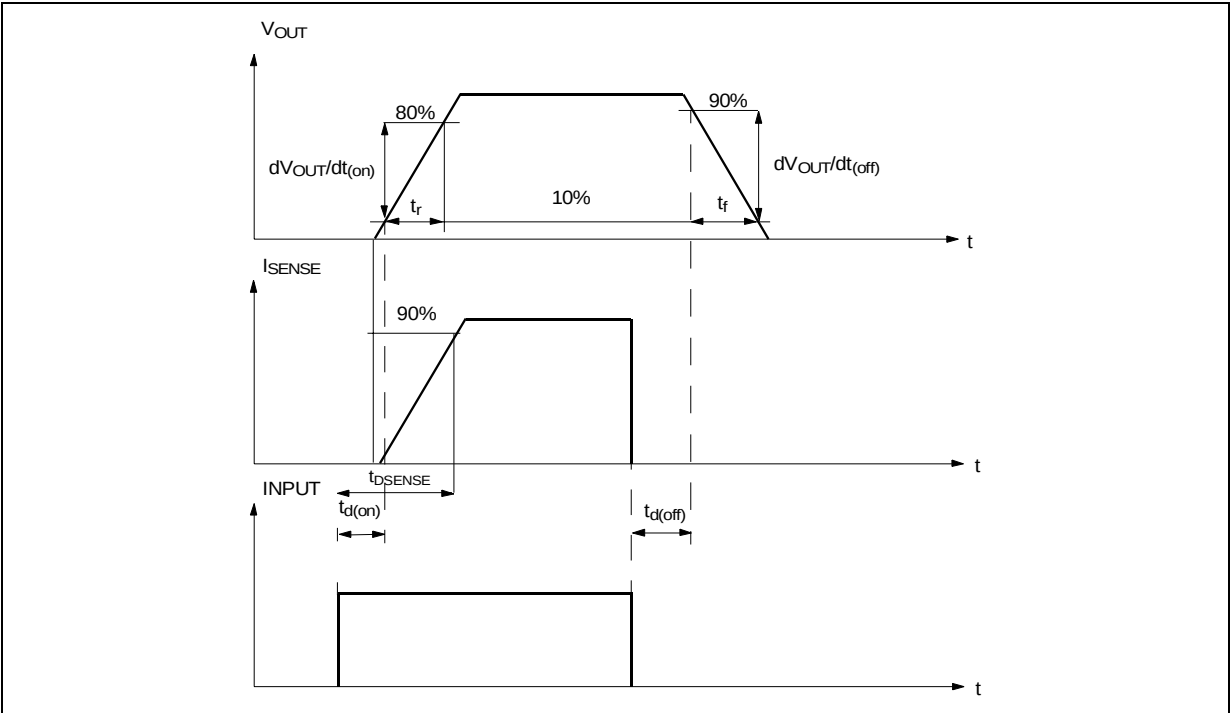


Table 11. Truth Table

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 ($T_J < T_{TSD}$) 0 ($T_J > T_{TSD}$) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Figure 7. Switching time Waveforms

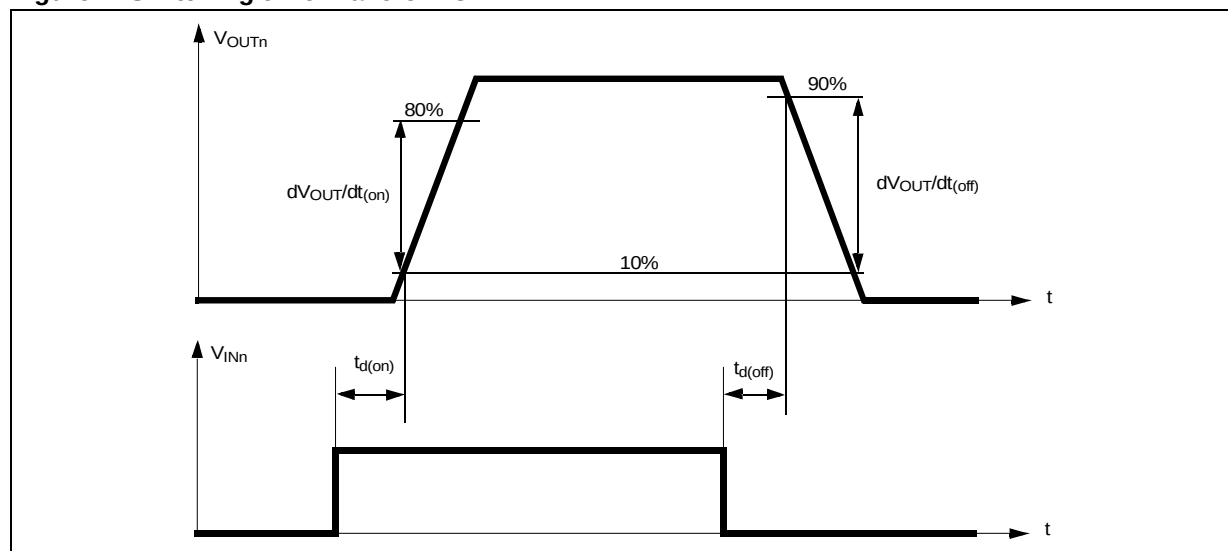


Table 12. Electrical Transient Requirements on V_{CC} Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μ s 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μ s 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 8. Waveforms

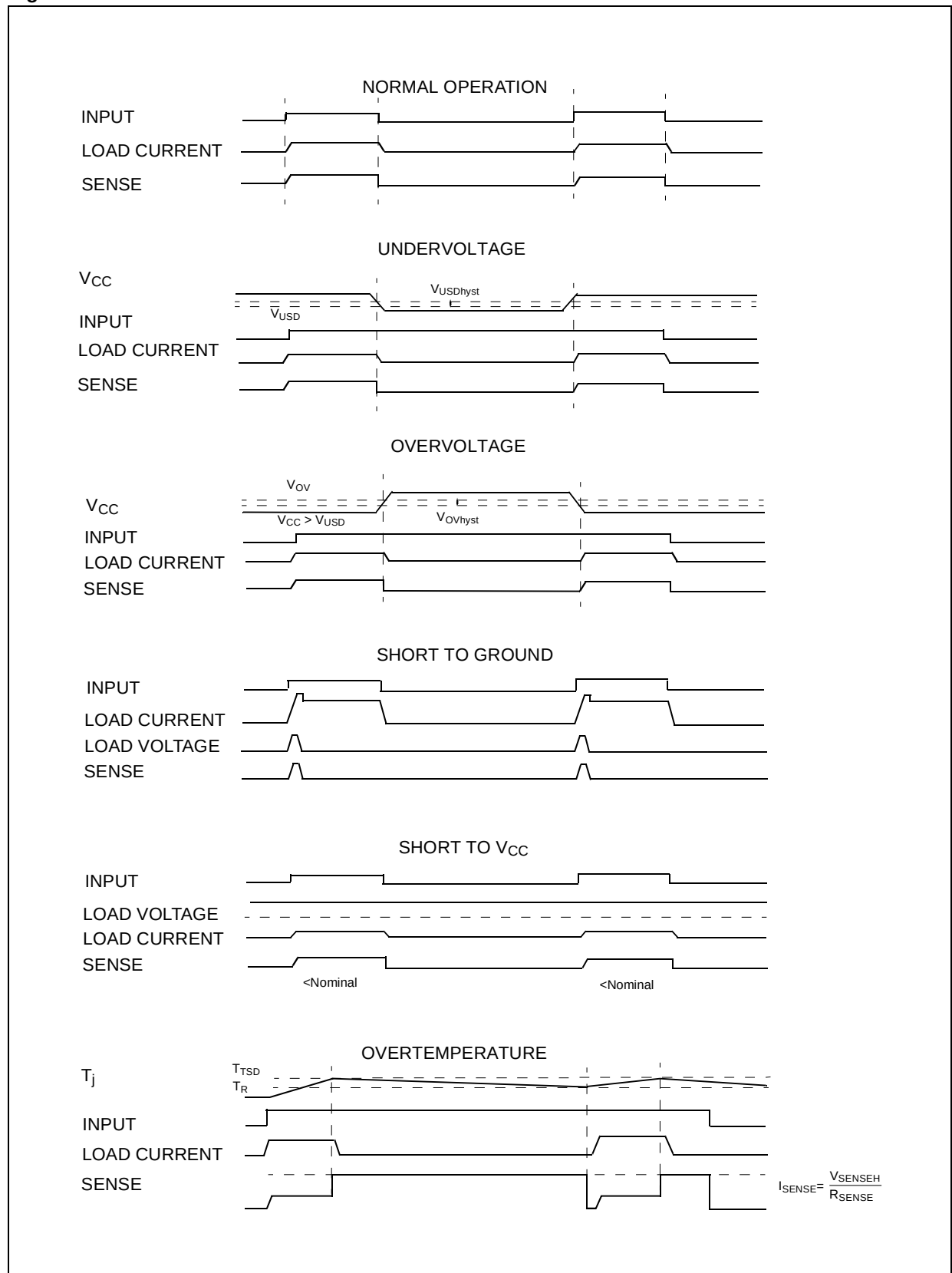
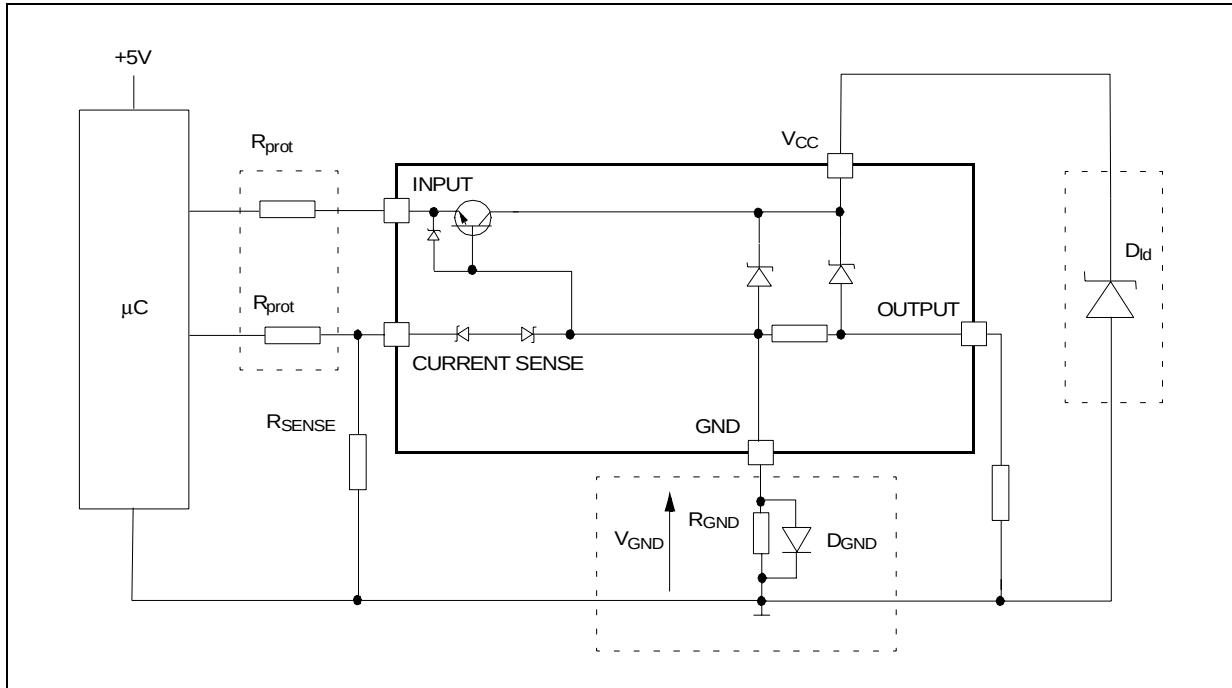


Figure 9. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND} = 1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ($\approx 600\text{mV}$) in the

input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT line is also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT pin is to leave it unconnected, while unused SENSE pin has to be connected to Ground pin.

LOAD DUMP PROTECTION

D_{Id} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$
 $5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega$.

Recommended R_{prot} value is $10\text{k}\Omega$.

Figure 10. Off State Output Current

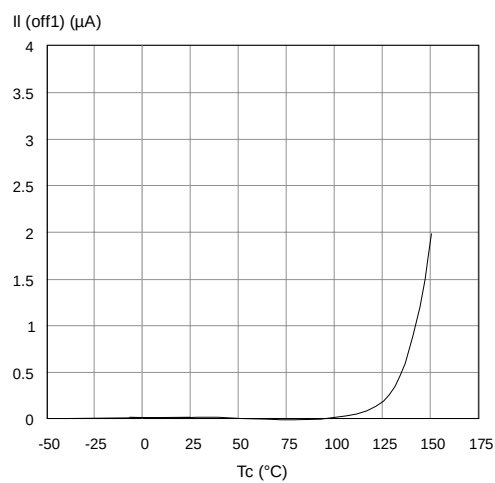


Figure 11. High Level Input Current

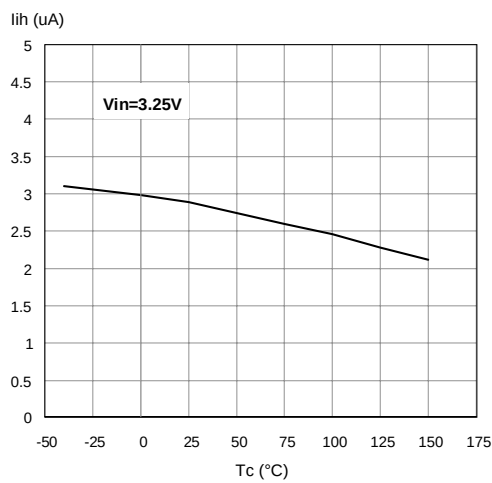


Figure 12. Input Clamp Voltage

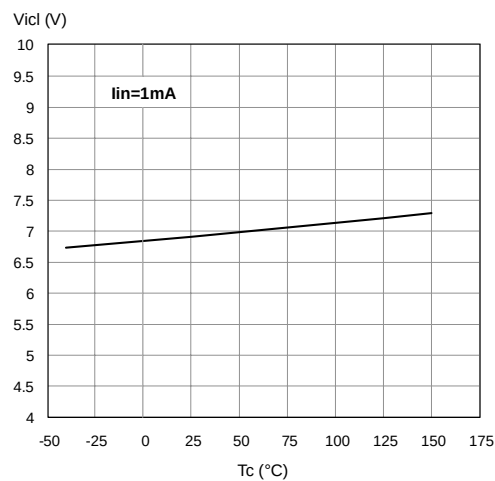


Figure 14. Input High Level

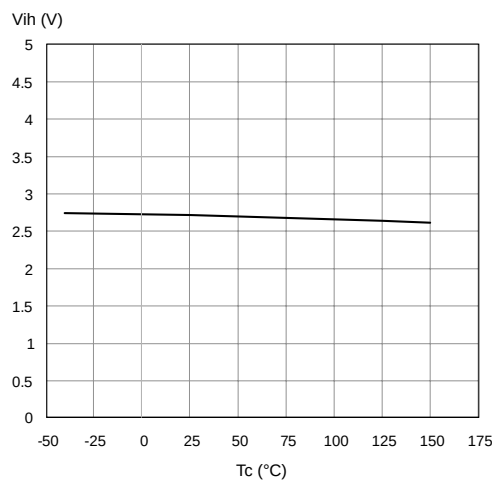


Figure 13. Input Low Level

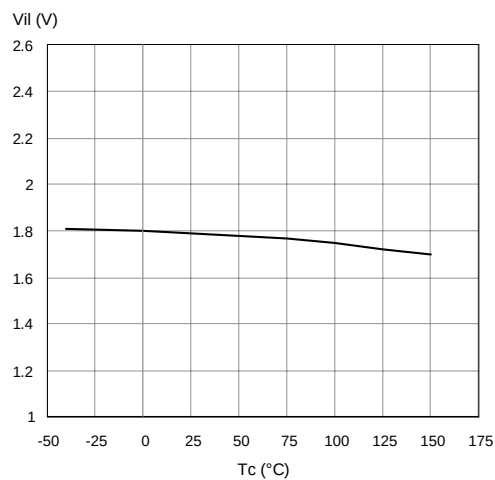


Figure 15. Input Hysteresis Voltage

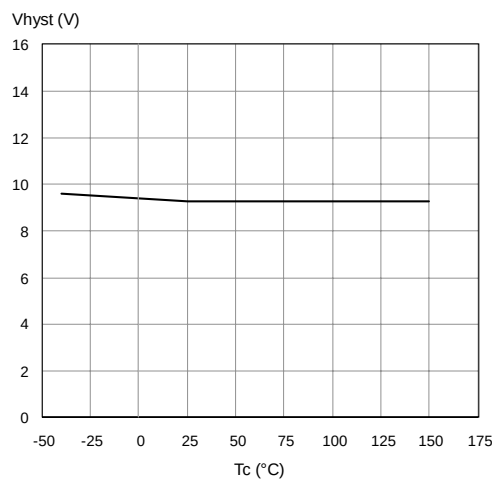


Figure 16. Overvoltage Shutdown

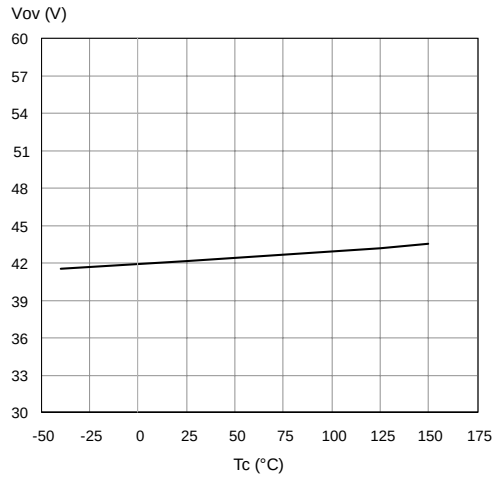


Figure 19. I_{LIM} Vs T_{case}

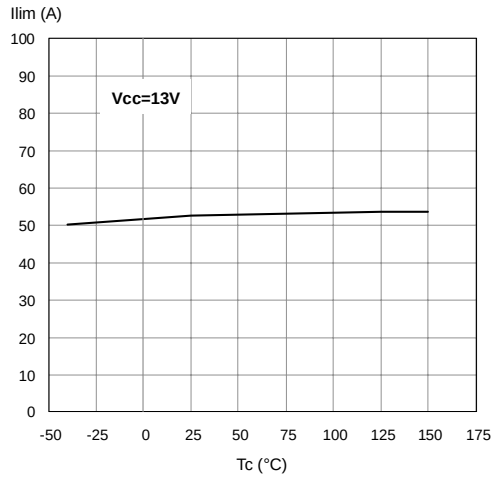


Figure 17. Turn-on Voltage Slope

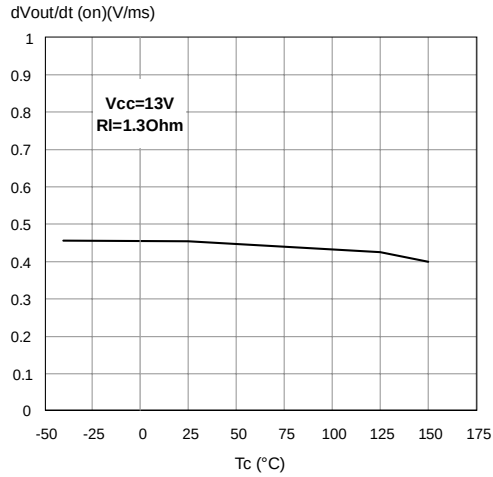


Figure 20. Turn-off Voltage Slope

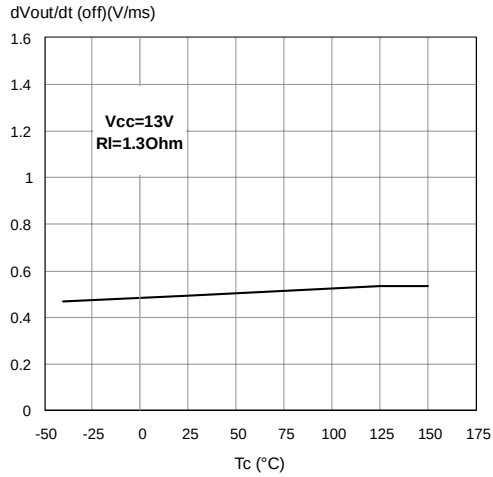
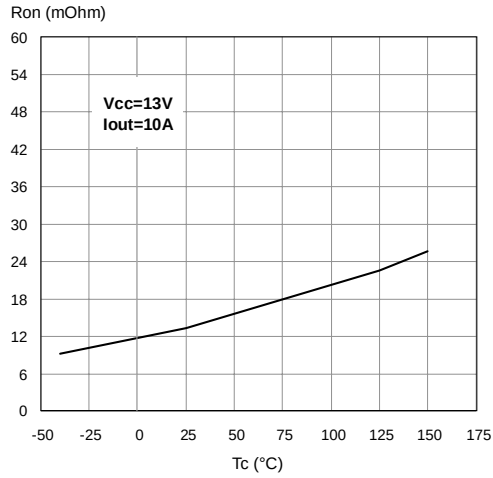


Figure 18. On State Resistance Vs T_{case}



PowerSSO-24 Thermal Data

Figure 21. PowerSSO-24 PC Board

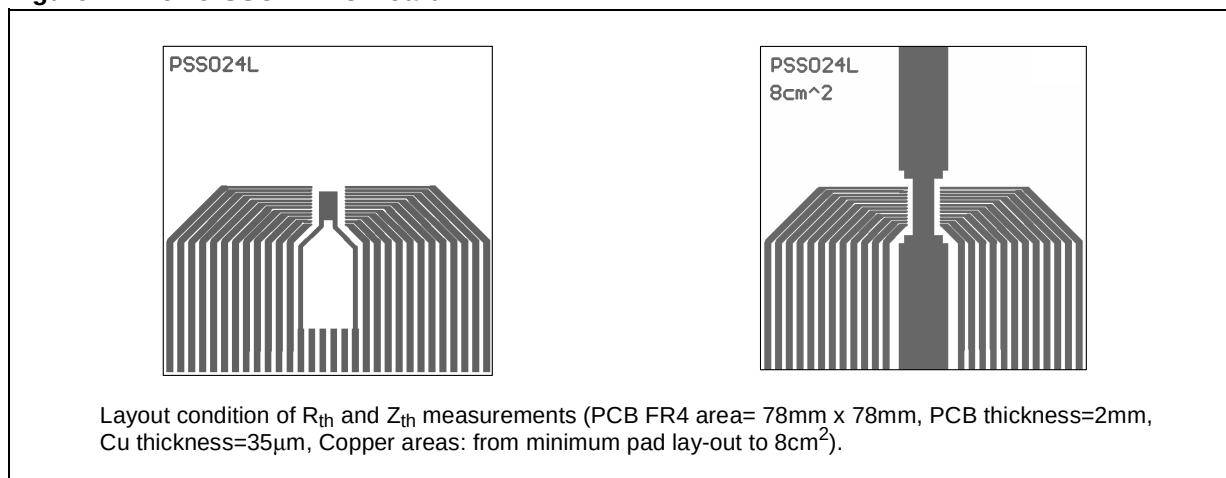
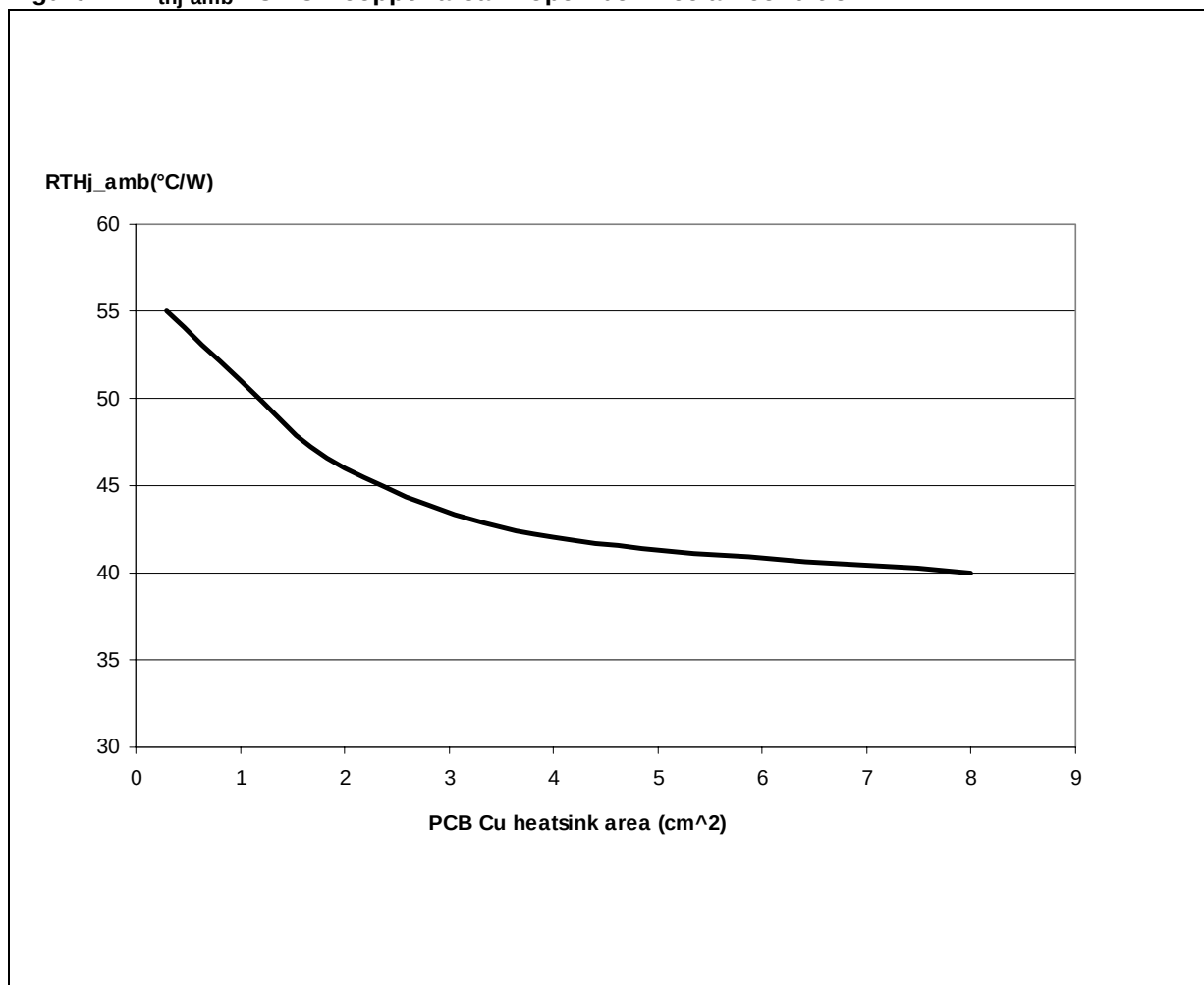
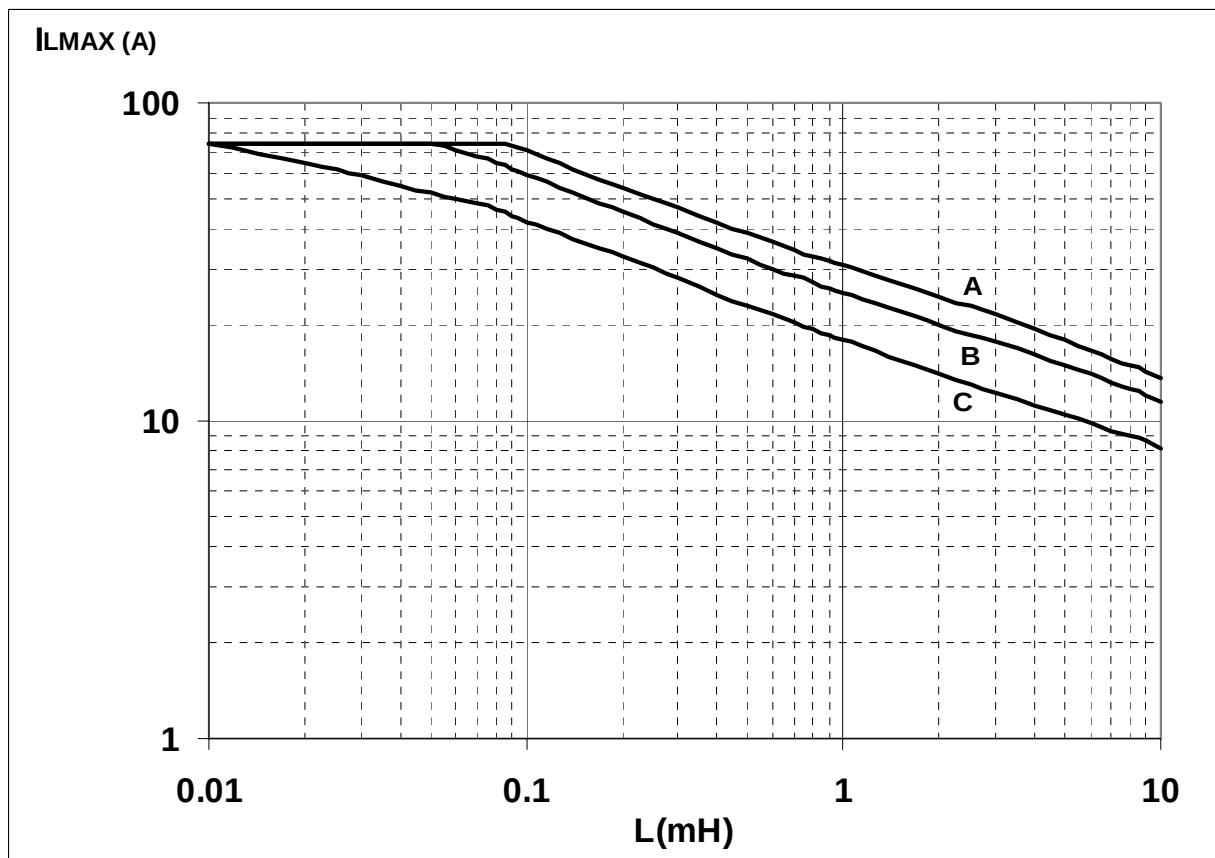
Figure 22. $R_{thj-amb}$ Vs PCB copper area in open box free air condition

Figure 23. Maximum turn off current versus load inductance



A = Single Pulse at $T_{Jstart}=150^{\circ}\text{C}$

B= Repetitive pulse at $T_{Jstart}=100^{\circ}\text{C}$

C= Repetitive Pulse at $T_{Jstart}=125^{\circ}\text{C}$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions:

$V_{CC}=13.5\text{V}$

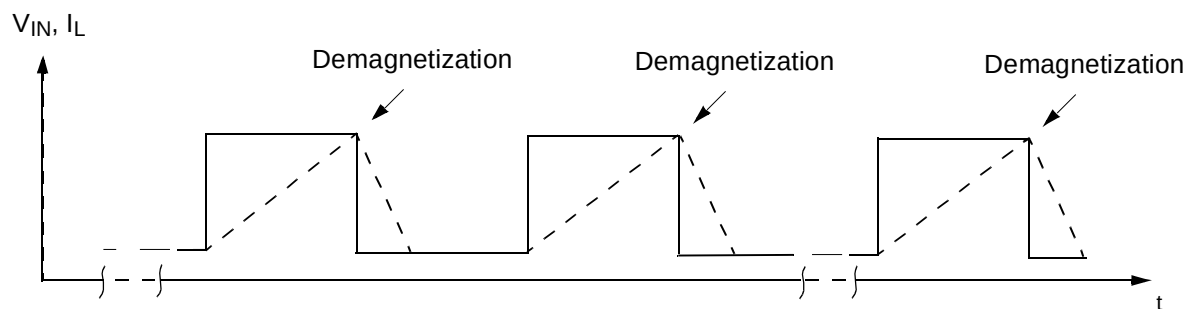


Figure 24. PowerSSO-24 Thermal Impedance Junction Ambient Single Pulse

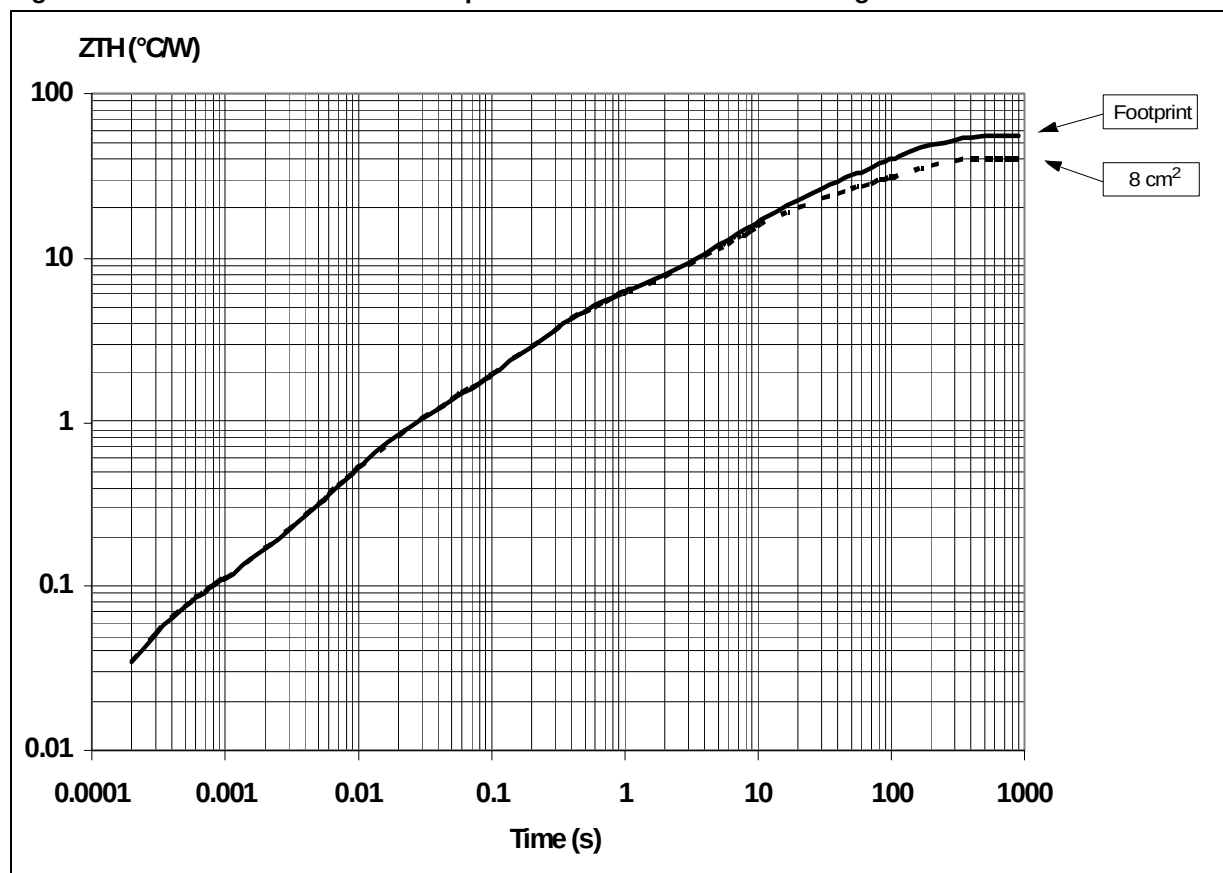
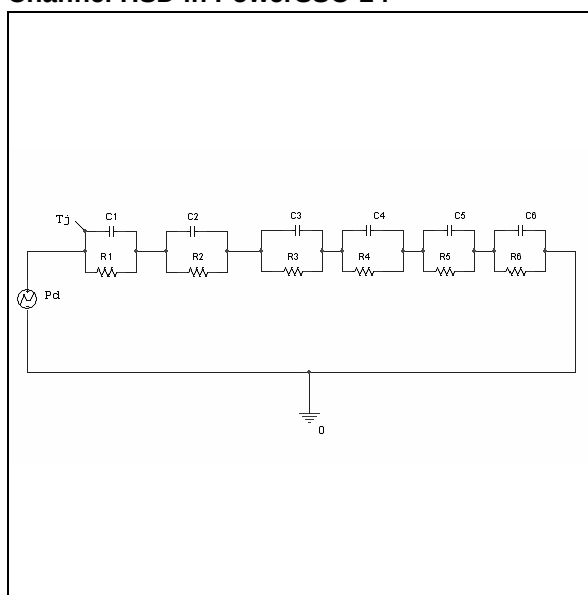


Figure 25. Thermal Fitting Model of a Single Channel HSD in PowerSSO-24

**Pulse Calculation Formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

Table 13. Thermal Parameter

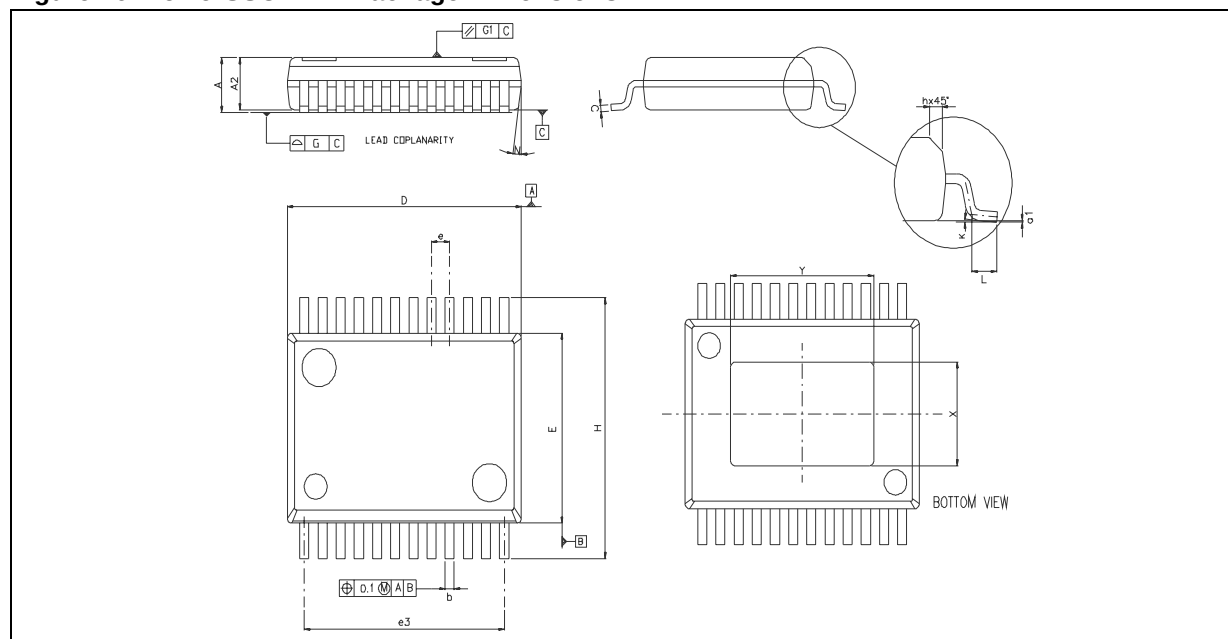
Area/island (cm ²)	Footprint	8
R1(°C/W)	0.012	
R2(°C/W)	0.05	
R3(°C/W)	0.65	
R4(°C/W)	4	
R5(°C/W)	13.5	
R6(°C/W)	37	22
C1(W.s/°C)	0.0004	
C2(W.s/°C)	0.005	
C3(W.s/°C)	0.022	
C4(W.s/°C)	0.08	
C5(W.s/°C)	0.7	
C6(W.s/°C)	3	5

PACKAGE MECHANICAL

Table 14. PowerSSO-24™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

Figure 26. PowerSSO-24™ Package Dimensions



REVISION HISTORY**Table 15. Revision History**

Date	Revision	Description of Changes
Oct. 2004	1	- First Issue.
Nov. 2004	2	- Mechanical data updating. - PowerSSO-24 Thermal Charact. insertion
Dec. 2004	3	- PC Board copper area correction.
Dec. 2004	4	- $IL_{(off2)}$ removal.
Mar. 2005	5	- Maximum Switching Energy value insertion. - Maximum turn off current versus load inductance curve insertion. - Minor changes.

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