

Low cost triple video buffer/filter for standard video

Features

- Triple channels
- Internal 6MHz-reconstruction filter (4th order)
- 6dB-gain buffer for 75Ω lines
- 5V single supply
- Bottom of video signal close to 0V
- Data min. and max. are physically tested and guaranteed during production

Applications

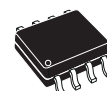
- Standard definition TV
- Set-top box
- DVD player/recorder

Description

The TSH103 is a low cost video buffer. It is dedicated to drive video signals from any video DACs output on 75Ω video lines in standard definition. With a real benefit in terms of integration and cost saving, this product is particularly efficient for the replacement of current discrete solutions using transistors, coil and capacitors for buffering and filtering.

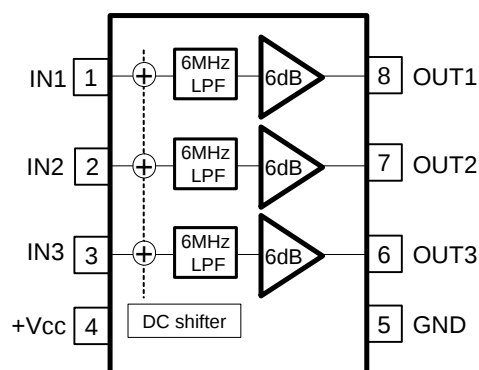
This triple channel is designed to drive either CVBS/Y-C or RGB or YPbPr or YUV formats. Each channel features an internal 6MHz reconstruction filter and a 6dB buffer (attenuation of 27MHz sampling and good output impedance matching with the video line).

The TSH103 requires a single 5V power supply. It is available in SO-8 plastic package.



SO-8 plastic package

Pin connections



1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	6	V
V_{in}	Maximum input voltage swing	0 to 3	V
T_{oper}	Operating free air temperature range	-40 to +85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thjc}	SO-8 thermal resistance junction to case	28	°C/W
R_{thja}	SO-8 thermal resistance junction to ambient area	157	°C/W
ESD	HBM: human body model	3.5	kV
	CDM: charged device model	1.5	kV
	MM: machine model	200	V
	Output short-circuit	(2)	

1. All voltage values are with respect to network terminal.
2. An output current limitation protects the circuit from transient currents. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on amplifiers.

2 Operating conditions

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	4.5 to 5.5 ⁽¹⁾	V

1. This range is guaranteed by design (the product is tested in full production at 5V single power supply).

3 Electrical characteristics

Table 3. $V_{CC} = +5V$ single supply, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{DC}	Output DC shift	$R_L = 150\Omega$	100	310	430	mV
		$-40^{\circ}C < T_{amb} < +85^{\circ}C$		312		
I_{ib}	Input bias current	$V_{in} = 0V$		1.2		μA
		$-40^{\circ}C < T_{amb} < +85^{\circ}C$		1.4		
I_{CC}	Supply current per channel	$V_{in} = 0.5V$ DC		5.5	7.1	mA
		$-40^{\circ}C < T_{amb} < +85^{\circ}C$		5.6		
G	DC voltage gain	$R_L = 150\Omega$	1.93	1.97	2	V/V
		$-40^{\circ}C < T_{amb} < +85^{\circ}C$		1.96		
V_{OH}	High level output voltage	$R_L = 150\Omega$		3.9		V
V_{OL}	Low level output voltage	$R_L = 150\Omega$		41	46	mV
I_{OUT}	I_{sink}/I_{source}			56		mA
Video performance						
F_{Cut}	-3dB bandwidth	Small signal, $R_L = 150\Omega$		9.4		MHz
	-1dB bandwidth	Small signal, $R_L = 150\Omega$	5.1	7.4		
F_{att}	Filter attenuation	Small signal, $F = 27MHz$		37		dB
gd	Group delay	0 to 5MHz		10		ns
dG	Differential gain	$R_L = 150\Omega$		0.5		%
dPh	Differential phase	$R_L = 150\Omega$		0.5		°
Noise						
e_n	Input voltage noise	100kHz		76		nV/VHz

Figure 1. Frequency response

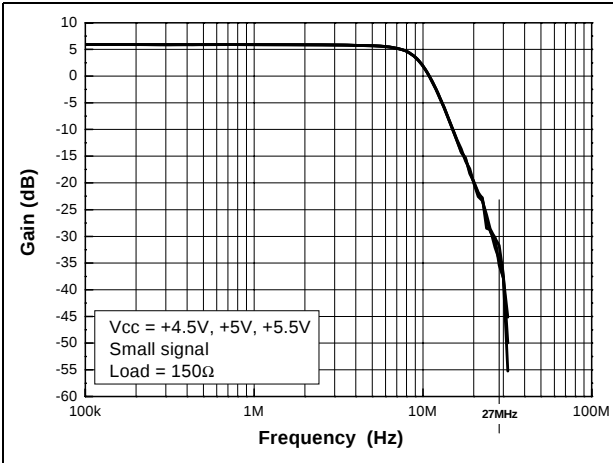


Figure 2. Gain flatness

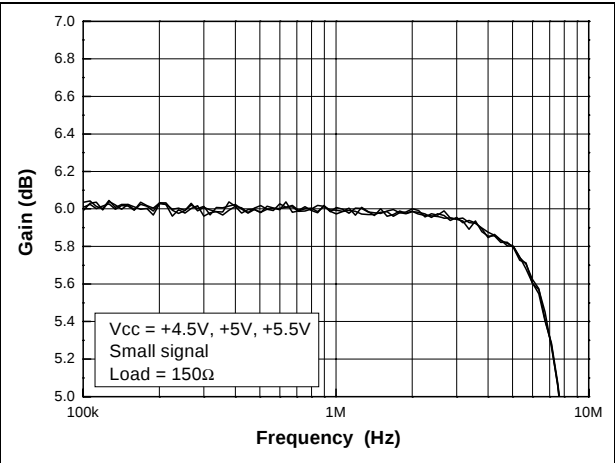


Figure 3. Frequency response (large signal)

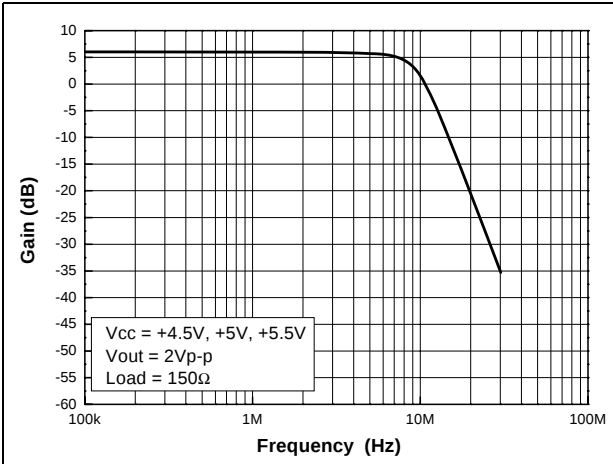


Figure 4. Distortion

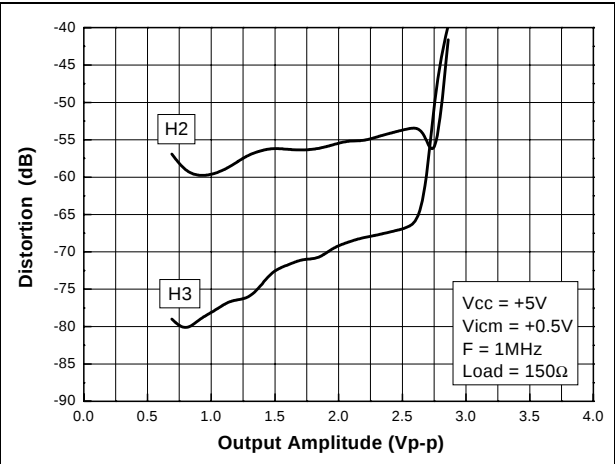


Figure 5. Quiescent current vs. Supply

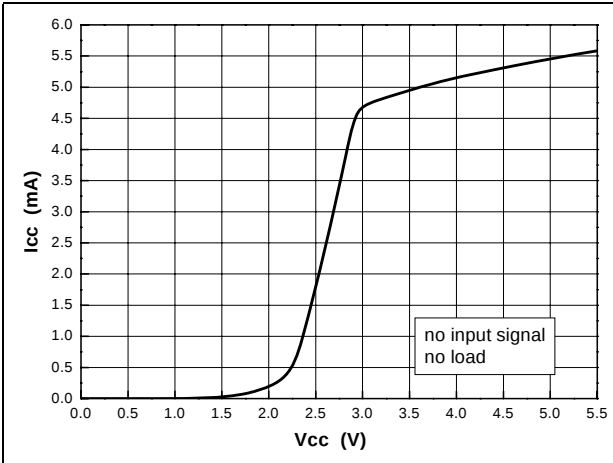
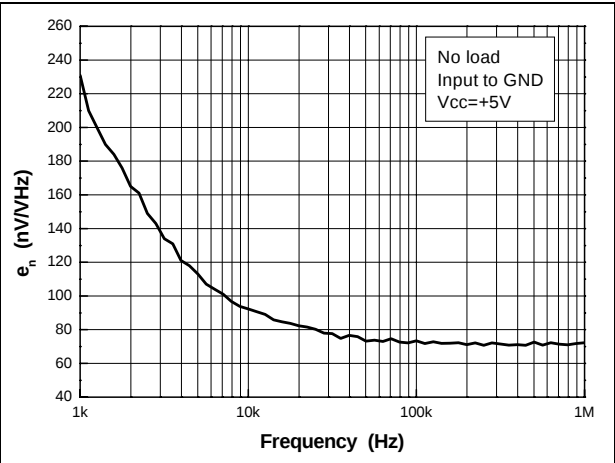


Figure 6. Input noise vs. frequency



4 Power supply considerations

Correct power supply bypassing is very important for optimizing performance in high-frequency ranges. Bypass capacitors should be placed as close as possible to the IC pins to improve high-frequency bypassing. A capacitor of 100 μ F is necessary to minimize the power supply noise in low frequency. For better quality bypassing, we recommend to add a CMS 100nF capacitor, also placed as close as possible to the IC pins.

Figure 7. Circuit for power supply bypassing

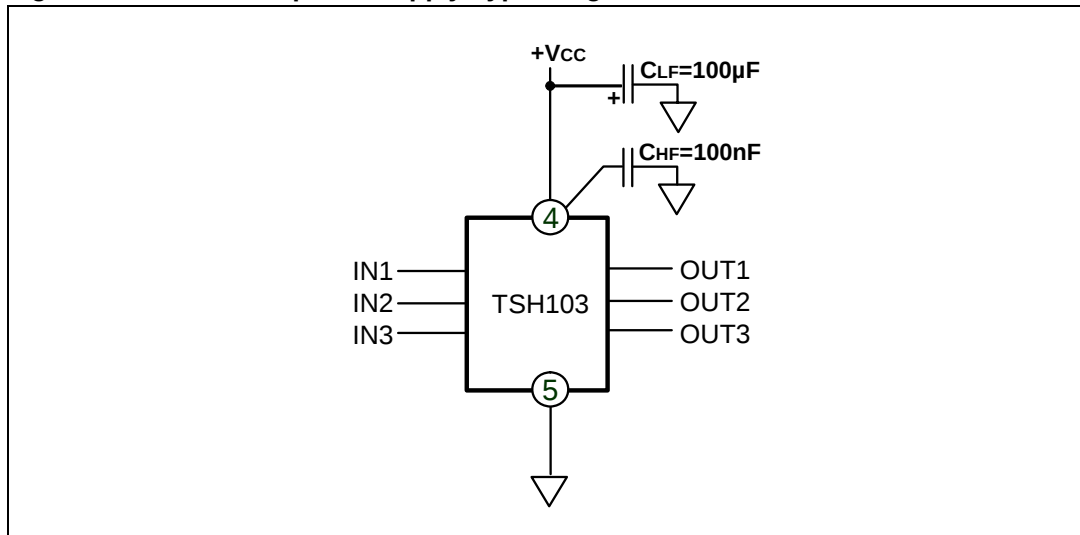
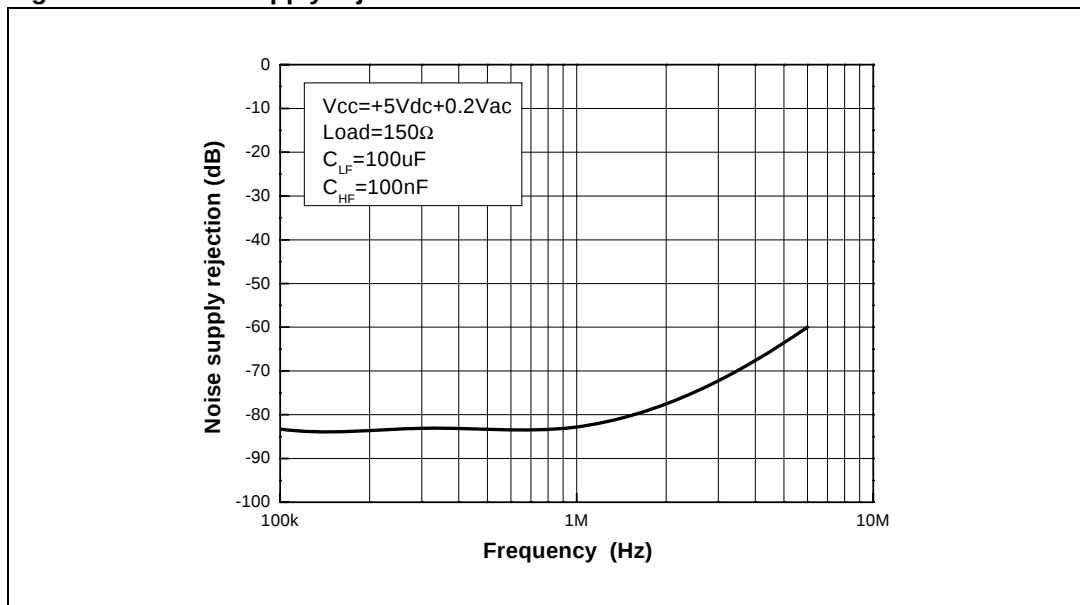
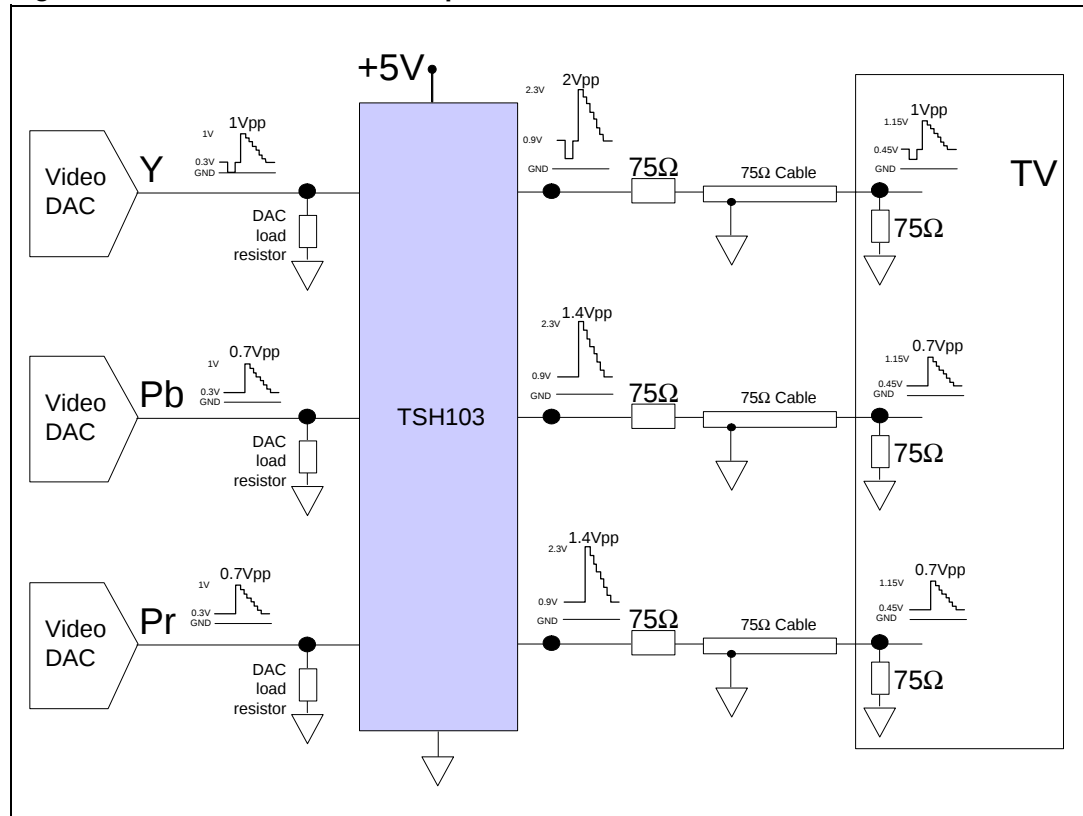


Figure 8. Noise supply rejection



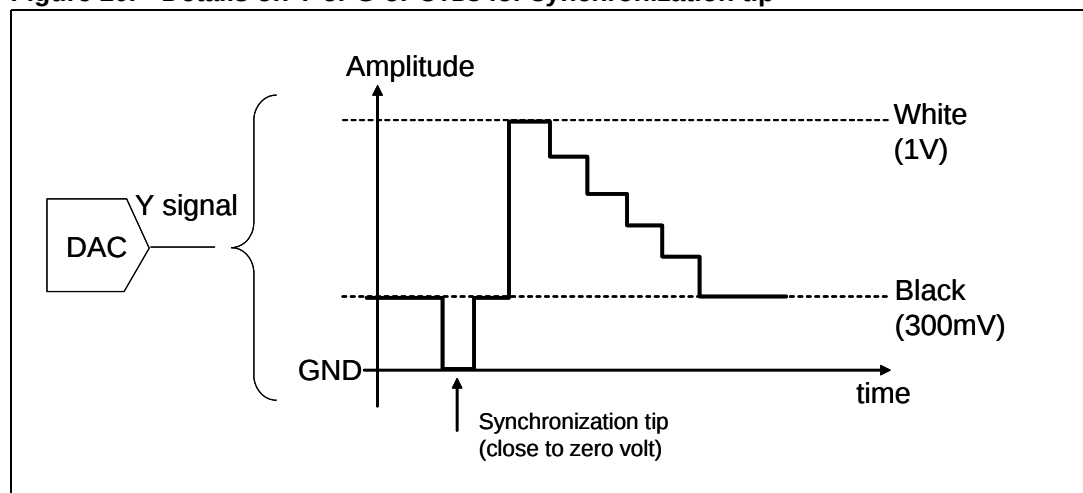
5 Using the TSH103 to drive video signals

Figure 9. Video line interface implementation schematics



The bottom of the synchronization tip at the DAC output can be as low as 0mV. In that case, the bottom is equal to 310mV typical at the TSH103 output (see values of the output DC shift in [Table 3](#)). The Y signal can be properly driven by the TSH103 because its low output rail (V_{OL}) is lower than 46mV ([Table 3](#)).

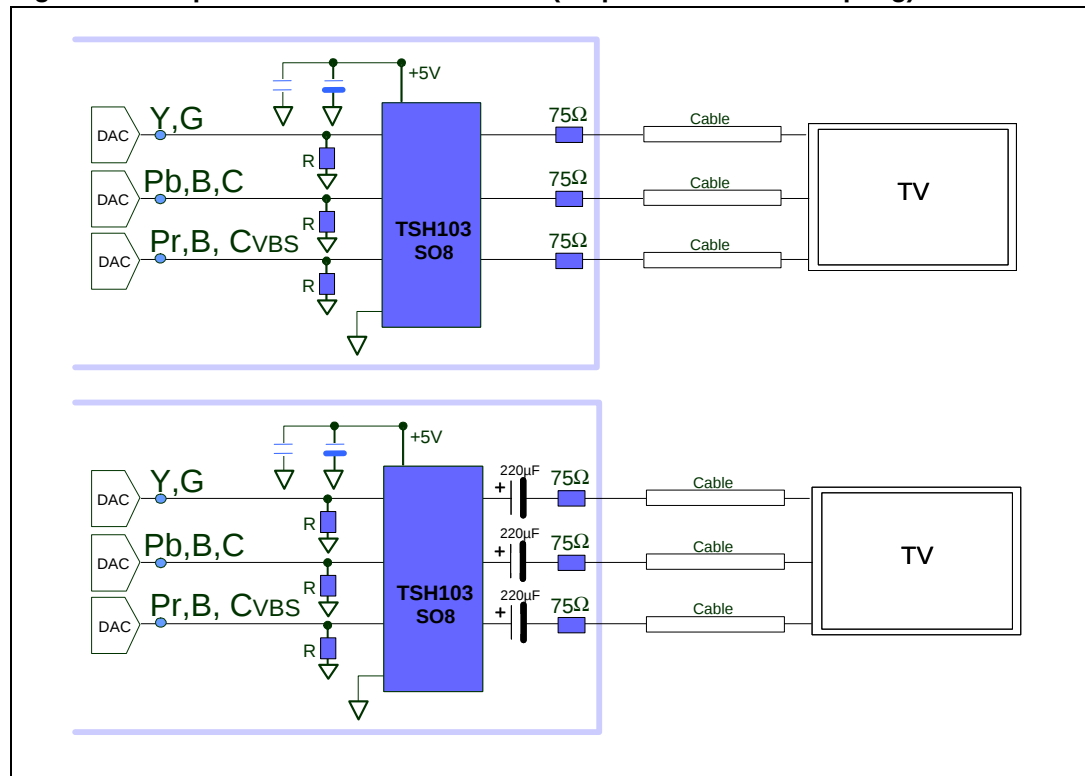
Figure 10. Details on Y or G or Cvsb for synchronization tip



The interface is illustrated in [Figure 11](#). It is composed of:

- Three 75-ohm resistors
- Three matching resistors
- One 10 μ F power supply decoupling capacitor
- One 10nF power supply decoupling capacitor

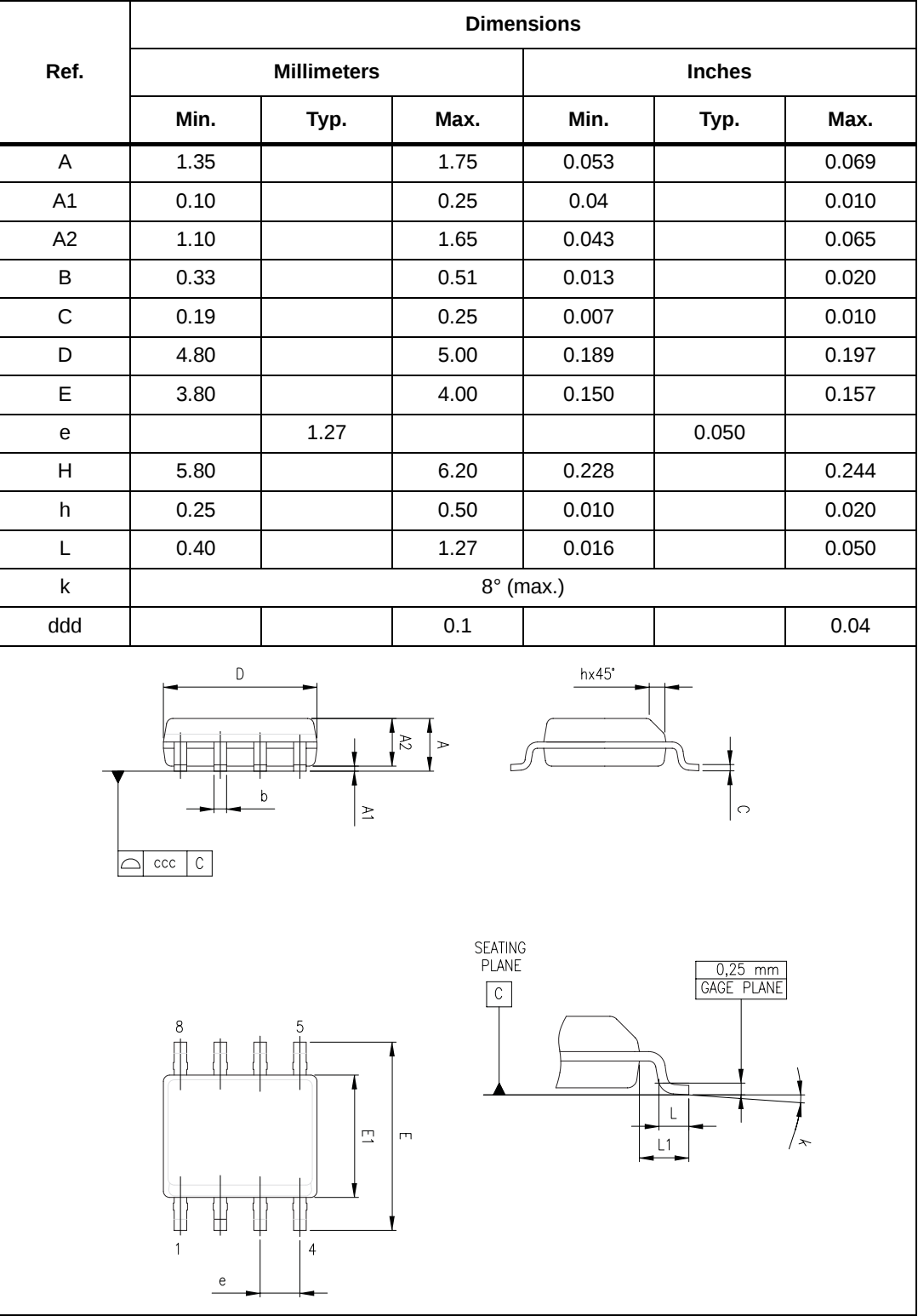
Figure 11. Implementation of the TSH103 (output DC and AC coupling)



1. Note that the TSH103 is input DC coupling only. It is not AC coupling.

6 Package information

Figure 12. SO-8 package mechanical data



7 Ordering information

Table 4. Order codes

Part number	Temperature range	Package	Packaging	Marking
TSH103ID	-40°C to +85°C	SO-8	Tube	TSH103I
TSH103IDT	-40°C to +85°C	SO-8	Tape & reel	TSH103I

8 Revision history

Date	Revision	Changes
19-Sep-2007	1	Initial release.

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