

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSIV)

# TPCP8301

Lithium Ion Battery Applications  
Notebook PC Applications  
Portable Equipment Applications

Unit: mm

- Lead (Pb)-free
- Small footprint due to small and thin package
- Low drain-source ON-resistance:  $R_{DS(ON)} = 25 \text{ m}\Omega$  (typ.)
- High forward transfer admittance:  $|Y_{fs}| = 14 \text{ S}$  (typ.)
- Low leakage current:  $I_{DSS} = -10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = -20 \text{ V}$ )
- Enhancement model:  $V_{th} = -0.5 \text{ to } -1.2 \text{ V}$  ( $V_{DS} = -10 \text{ V}$ ,  $I_D = -200 \text{ }\mu\text{A}$ )

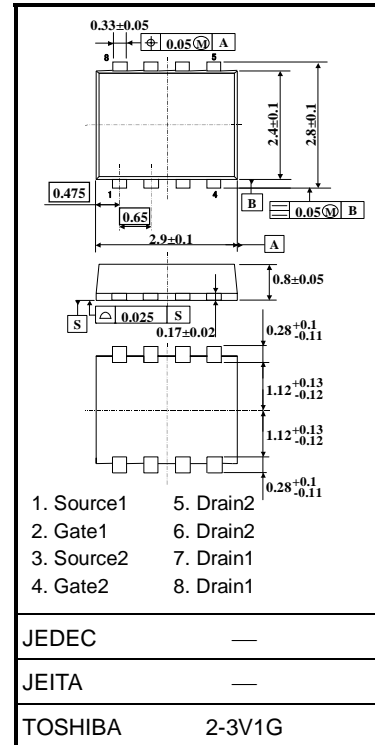
## Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristic		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	-20	V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )		$V_{DGR}$	-20	V
Gate-source voltage		$V_{GSS}$	$\pm 12$	V
Drain current	DC (Note 1)	$I_D$	-5	A
	Pulse (Note 1)	$I_{DP}$	-20	
Drain power dissipation ( $t = 5 \text{ s}$ ) (Note 2a)	Single-device operation (Note 3a)	$P_D$ (1)	1.48	W
	Single-device value at dual operation (Note 3b)	$P_D$ (2)	1.23	
Drain power dissipation ( $t = 5 \text{ s}$ ) (Note 2b)	Single-device operation (Note 3a)	$P_D$ (1)	0.58	
	Single-device value at dual operation (Note 3b)	$P_D$ (2)	0.36	
Single-pulse avalanche energy (Note 4)		$E_{AS}$	6.5	mJ
Avalanche current		$I_{AR}$	-5	A
Repetitive avalanche energy Single-device value at dual operation (Note 2a, 3b, 5)		$E_{AR}$	0.12	mJ
Channel temperature		$T_{ch}$	150	$^\circ\text{C}$
Storage temperature range		$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: For Notes 1 to 6, see the next page.

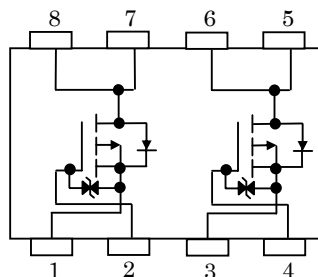
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

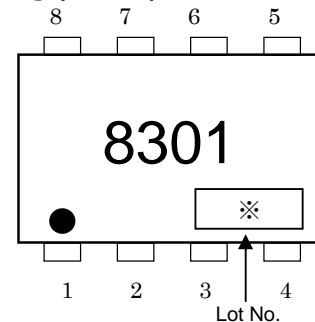


Weight: 0.017 g (typ.)

## Circuit Configuration



## Marking (Note 6)

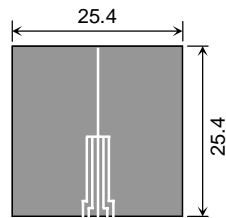


## Thermal Characteristics

Characteristic		Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 5 s) (Note 2a)	Single-device operation (Note 3a)	$R_{th (ch-a) (1)}$	84.5	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th (ch-a) (2)}$	101.6	
Thermal resistance, channel to ambient (t = 5 s) (Note 2b)	Single-device operation (Note 3a)	$R_{th (ch-a) (1)}$	215.5	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th (ch-a) (2)}$	347.2	

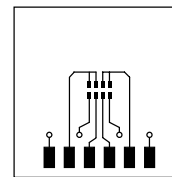
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



(a)

FR-4  
25.4 × 25.4 × 0.8  
(Unit: mm)



(b)

FR-4  
25.4 × 25.4 × 0.8  
(Unit: mm)

Note 3: a) The power dissipation and thermal resistance values shown are for a single device. (During single-device operation, power is applied to one device only.)

b) The power dissipation and thermal resistance values shown are for a single device. (During dual operation, power is applied to both devices evenly.).

Note 4:  $V_{DD} = -16$  V,  $T_{ch} = 25^{\circ}\text{C}$  (initial),  $L = 0.2$  mH,  $R_G = 25\ \Omega$ ,  $I_{AR} = -5$  A

Note 5: Repetitive rating: Pulse width limited by Max. Channel temperature.

Note 6: ● on the lower left of the marking indicates Pin 1.

\* Weekly code (3 digits):



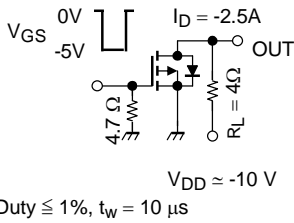
Week of manufacture

(01 for the first week of the year, continuing up to 52 or 53)

Year of manufacture

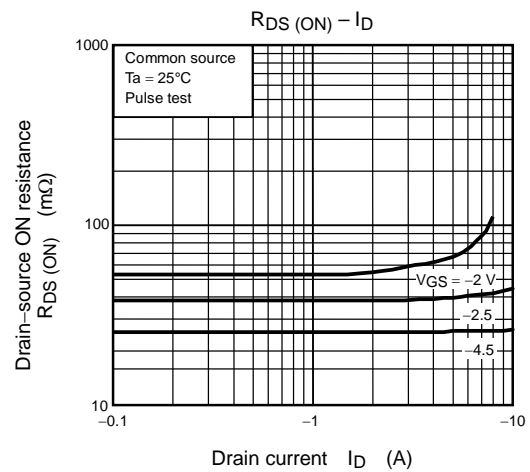
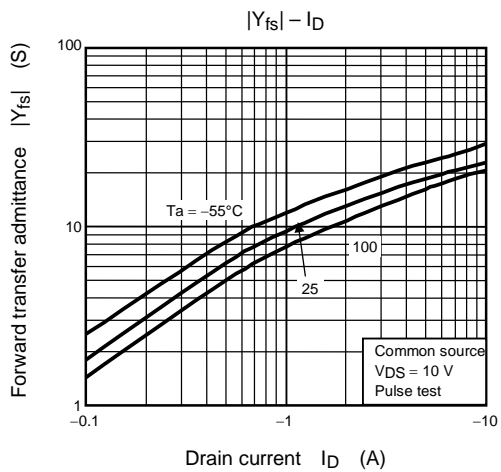
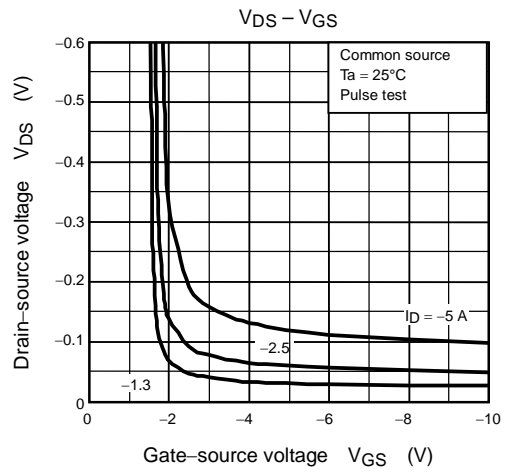
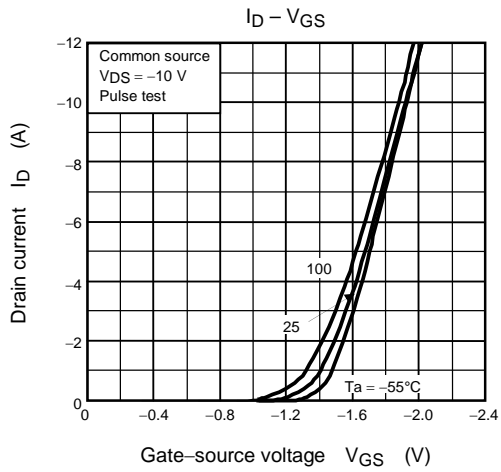
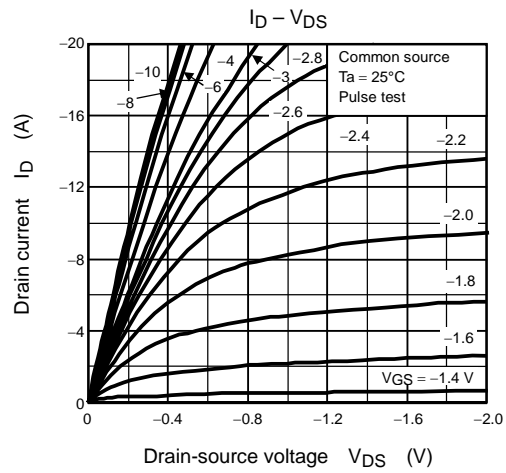
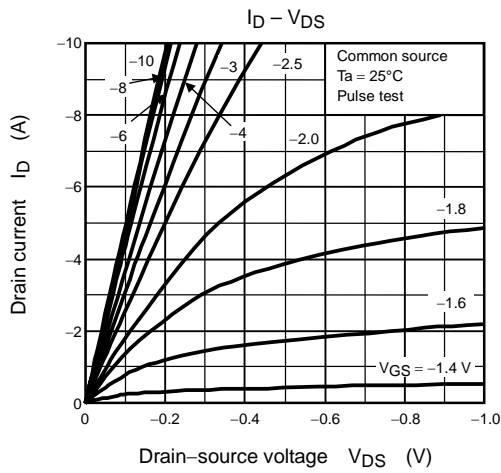
(The last digit of the calendar year)

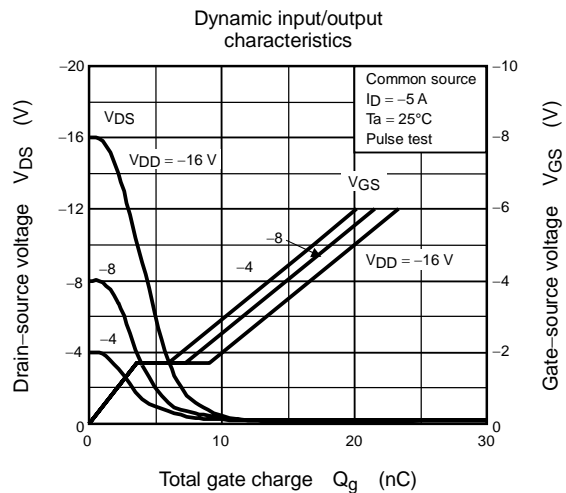
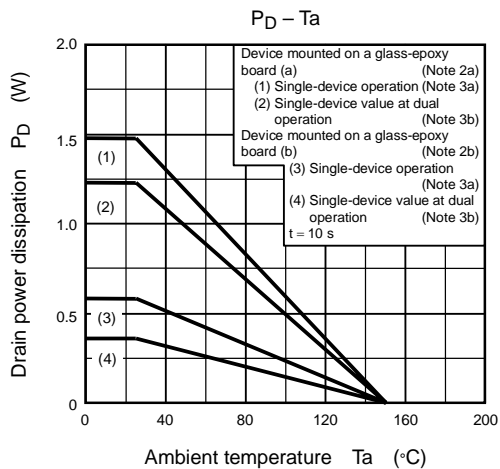
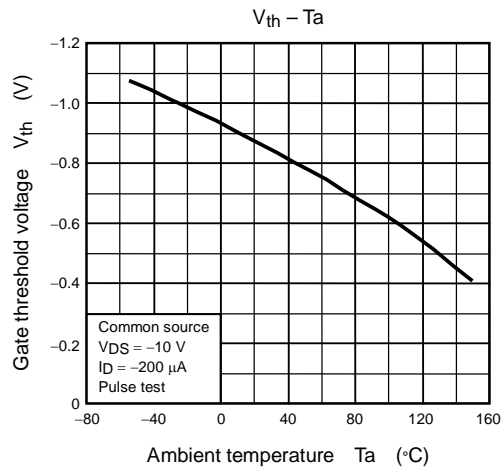
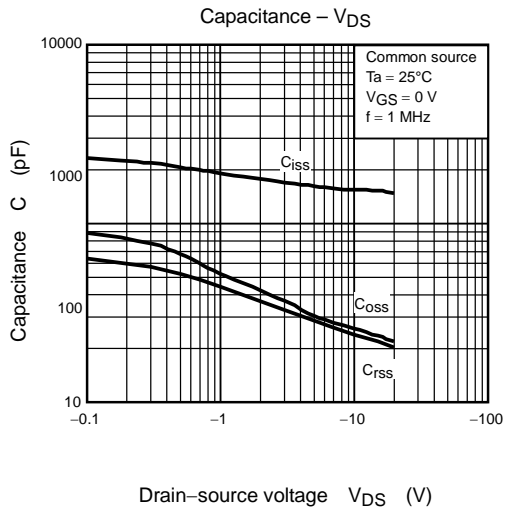
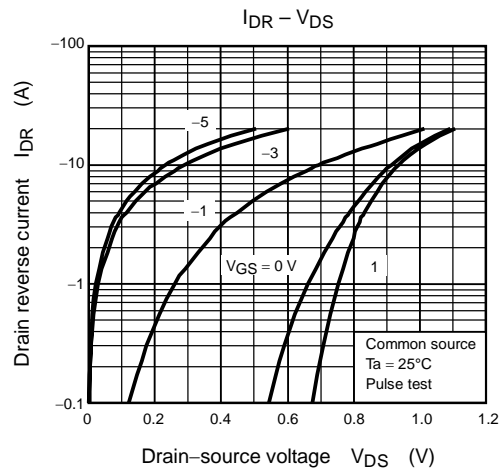
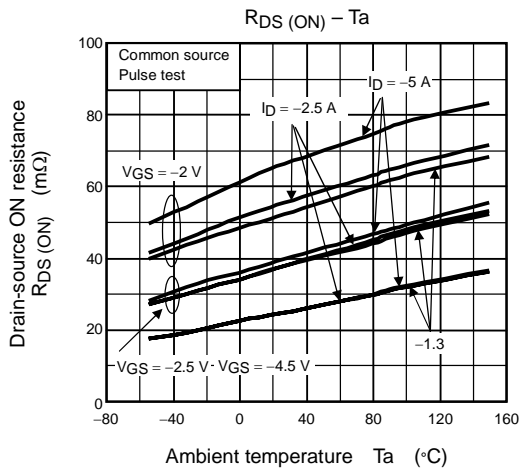
## Electrical Characteristics (Ta = 25°C)

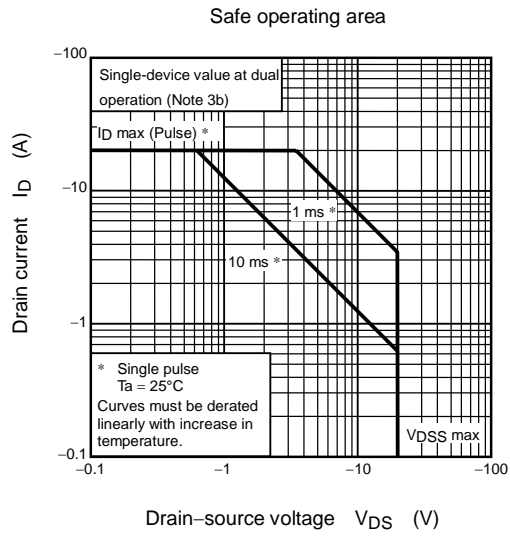
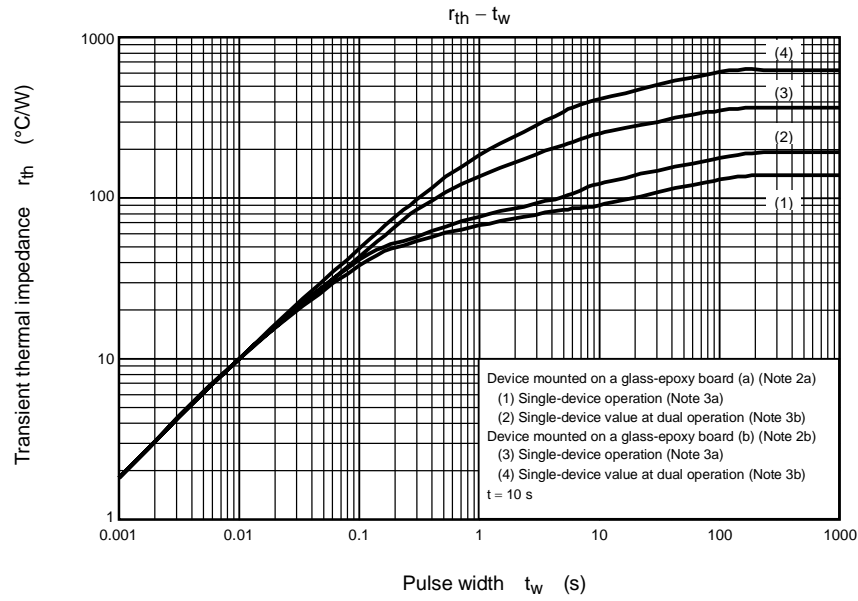
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		$I_{GSS}$	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain cutoff current		$I_{DSS}$	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	-10	$\mu\text{A}$
Drain-source breakdown voltage	$V_{(BR)DSS}$		$I_D = -10 \text{ mA}, V_{GS} = 0 \text{ V}$	-20	—	—	V
	$V_{(BR)DSX}$		$I_D = -10 \text{ mA}, V_{GS} = -12 \text{ V}$	-8	—	—	
Gate threshold voltage		$V_{th}$	$V_{DS} = -10 \text{ V}, I_D = -200 \mu\text{A}$	-0.5	—	-1.2	V
Drain-source ON-resistance	$R_{DS(ON)}$		$V_{GS} = -2.0 \text{ V}, I_D = -1.3 \text{ A}$	—	55	130	$\text{m}\Omega$
	$R_{DS(ON)}$		$V_{GS} = -2.5 \text{ V}, I_D = -2.5 \text{ A}$	—	38	60	
	$R_{DS(ON)}$		$V_{GS} = -4.5 \text{ V}, I_D = -2.5 \text{ A}$	—	25	31	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = -10 \text{ V}, I_D = 2.5 \text{ A}$	7	14	—	S
Input capacitance		$C_{iss}$	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	1500	—	pF
Reverse transfer capacitance		$C_{rss}$		—	240	—	
Output capacitance		$C_{oss}$		—	220	—	
Switching time	Rise time	$t_r$		—	10	—	ns
	Turn-on time	$t_{on}$		—	20	—	
	Fall time	$t_f$		—	50	—	
	Turn-off time	$t_{off}$		—	170	—	
Total gate charge (gate-source plus gate-drain)		$Q_g$	$V_{DD} \approx -16 \text{ V}, V_{GS} = -5 \text{ V}, I_D = -5 \text{ A}$	—	20	—	nC
Gate-source charge <sup>1</sup>		$Q_{gs1}$		—	3.6	—	
Gate-drain ("Miller") charge		$Q_{gd}$		—	5.5	—	

## Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	$I_{DRP}$	—	—	—	-20	A
Forward voltage (diode)		$V_{DSF}$	$I_{DR} = -5 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	1.2	V







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