

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (Ultra-High-Speed U-MOSⅢ)

## TK55D10J1

### Switching Regulator Applications

- High-Speed switching
- Low gate charge:  $Q_g = 110 \text{ nC}$  (typ.)
- Low drain-source ON resistance:  $R_{DS(ON)} = 8.4 \text{ m}\Omega$  (typ.)
- High forward transfer admittance:  $|Y_{fs}| = 110 \text{ S}$
- Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = 100 \text{ V}$ )
- Enhancement mode:  $V_{th} = 1.1 \text{ to } 2.3 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 1 \text{ mA}$ )

### Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	100	V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )		$V_{DGR}$	100	V
Gate-source voltage		$V_{GSS}$	$\pm 20$	V
Drain current	DC (Note 1)	$I_D$	55	A
	Pulse (Note 1)	$I_{DP}$	210	
Drain power dissipation ( $T_c = 25^\circ\text{C}$ )		$P_D$	140	W
Single pulse avalanche energy (Note 2)		$E_{AS}$	382	mJ
Avalanche current		$I_{AR}$	55	A
Repetitive avalanche energy (Note 3)		$E_{AR}$	9.4	mJ
Channel temperature		$T_{ch}$	150	$^\circ\text{C}$
Storage temperature range		$T_{stg}$	-55 to 50	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

### Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	0.89	$^\circ\text{C/W}$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	83.3	$^\circ\text{C/W}$

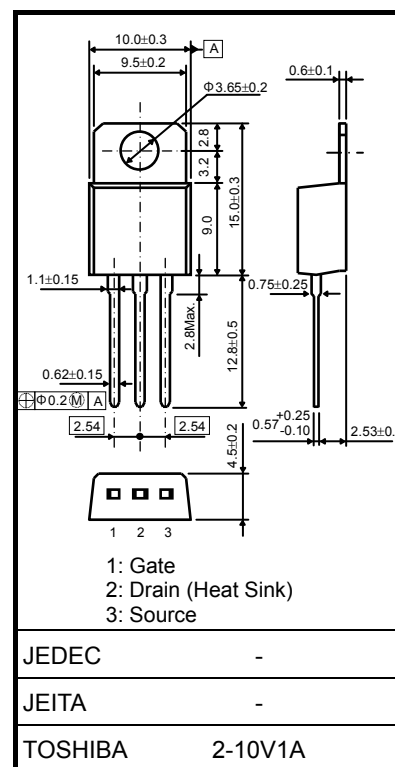
Note 1: Ensure that the channel and lead temperatures do not exceed  $150^\circ\text{C}$ .

Note 2:  $V_{DD} = 25 \text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$ ,  $L = 200 \text{ }\mu\text{H}$ ,  $I_{AR} = 55 \text{ A}$ ,  $R_G = 1 \text{ }\Omega$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

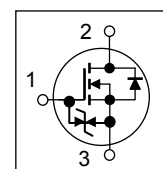
This transistor is an electrostatic-sensitive device. Handle with care.

Unit: mm

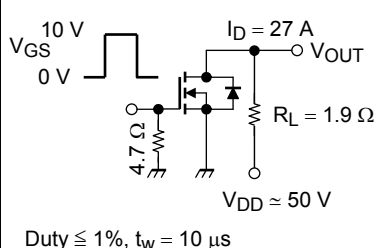


Weight: 1.35 g (typ.)

### Internal Connection



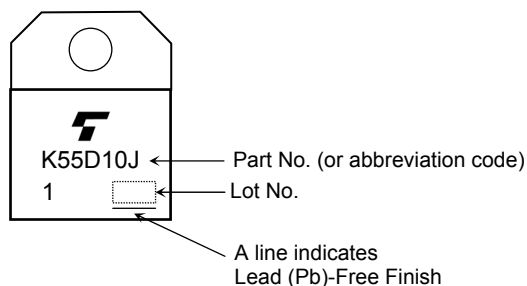
## Electrical Characteristics (Ta = 25°C)

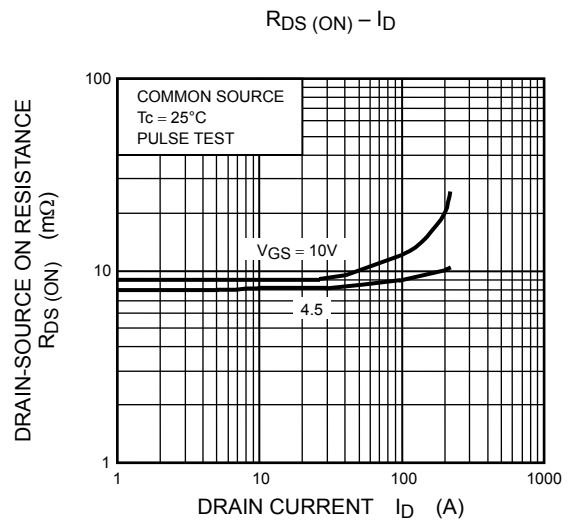
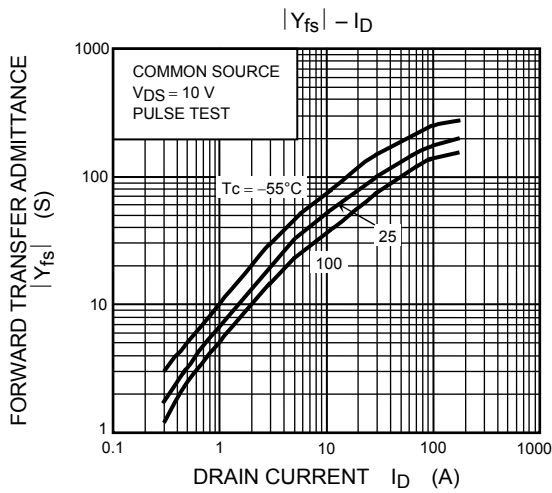
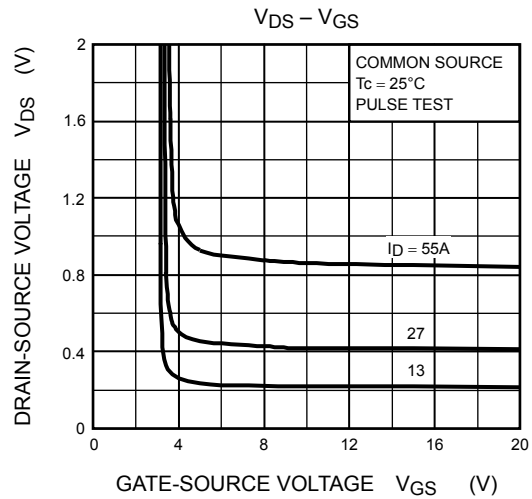
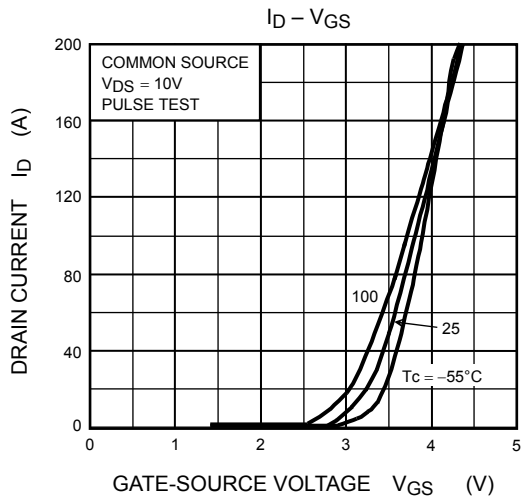
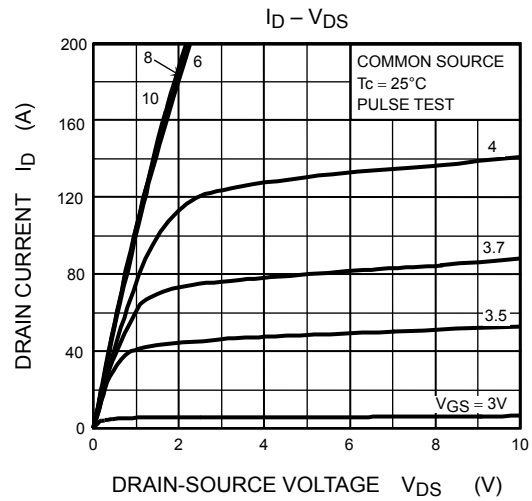
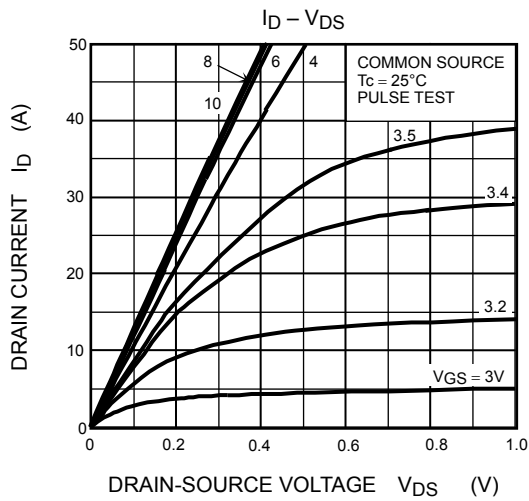
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V	—	—	±10	μA
Drain cut-OFF current		I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V	—	—	10	μA
Drain-source breakdown voltage		V (BR) DSS	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0 V	100	—	—	V
		V (BR) DSX	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = -20 V	55	—	—	
Gate threshold voltage		V <sub>th</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.1	—	2.3	V
Drain-source ON resistance		R <sub>DS (ON)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 27A	—	9.0	12.0	mΩ
			V <sub>GS</sub> = 10 V, I <sub>D</sub> = 27A	—	8.4	10.5	
Forward transfer admittance		Y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 27 A	55	110	—	S
Input capacitance		C <sub>iss</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0 V, f = 1 MHz	—	5700	—	pF
Reverse transfer capacitance		C <sub>rss</sub>		—	390	—	
Output capacitance		C <sub>oss</sub>		—	1000	—	
Switching time	Rise time	t <sub>r</sub>		—	7	—	ns
	Turn-ON time	t <sub>on</sub>		—	30	—	
	Fall time	t <sub>f</sub>		—	20	—	
	Turn-OFF time	t <sub>off</sub>		—	130	—	
Total gate charge (gate-source plus gate-drain)		Q <sub>g</sub>	V <sub>DD</sub> ≈ 80 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 55A	—	63	—	nC
			V <sub>DD</sub> ≈ 80 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 55A	—	110	—	
Gate-source charge 1		Q <sub>gs1</sub>	V <sub>DD</sub> ≈ 80 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 55A	—	17	—	
Gate-drain ("miller") charge		Q <sub>gd</sub>		—	32	—	
Gate switch charge		Q <sub>sw</sub>		—	38	—	

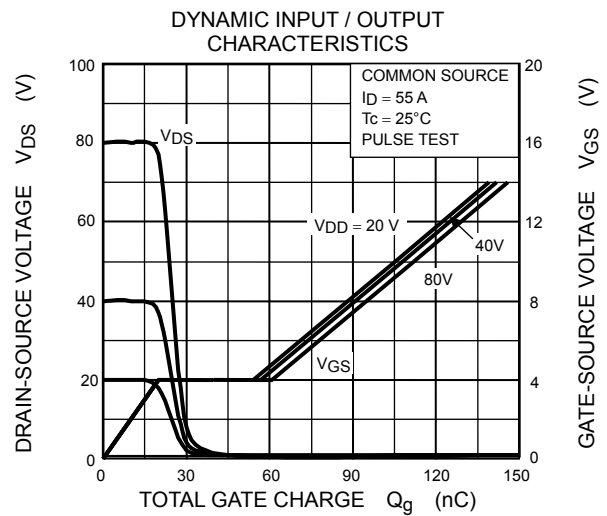
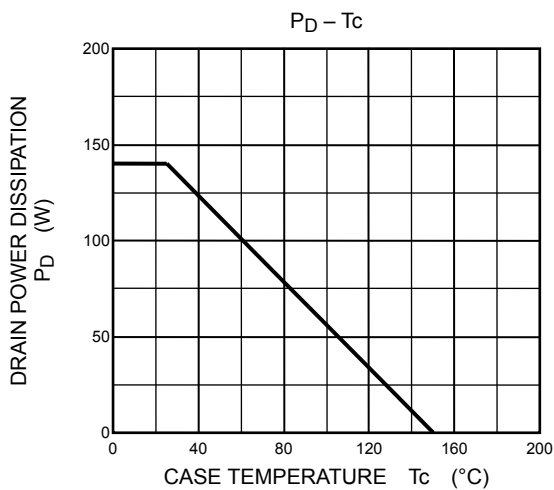
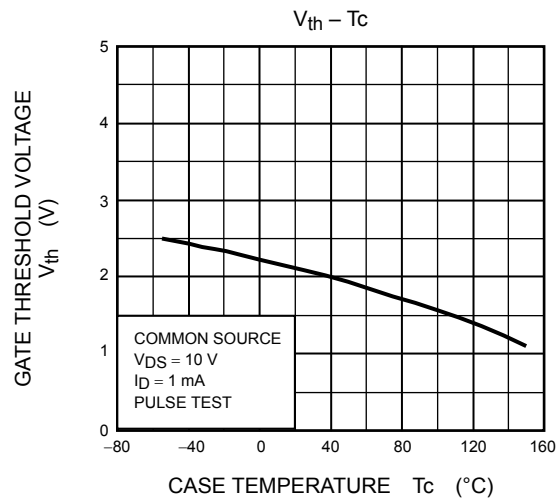
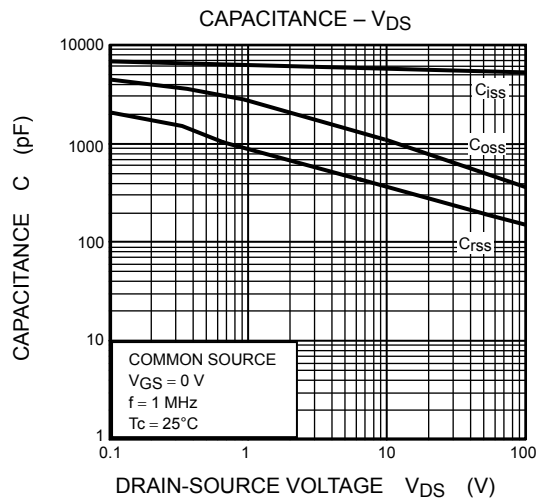
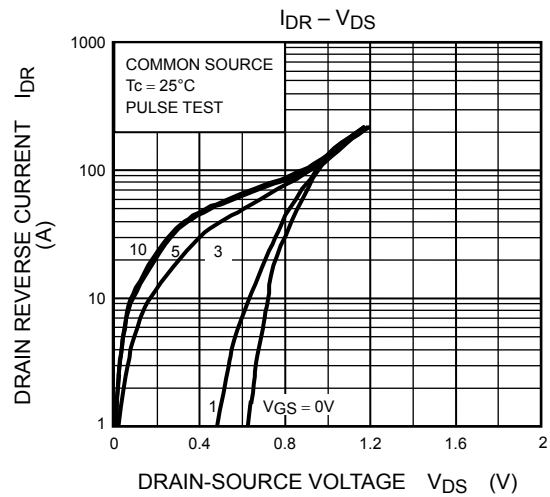
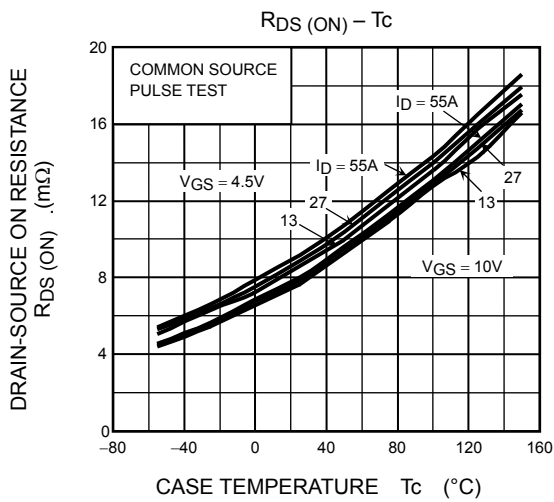
## Source-Drain Ratings and Characteristics (Ta = 25°C)

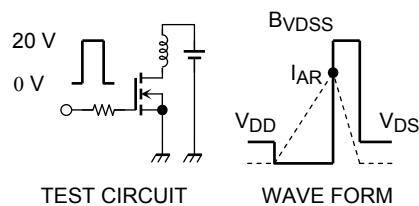
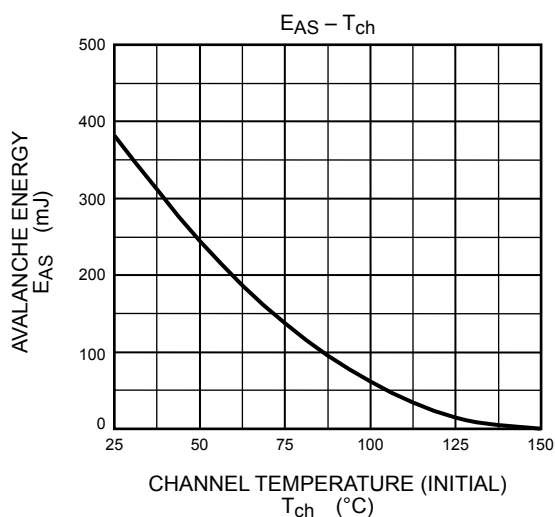
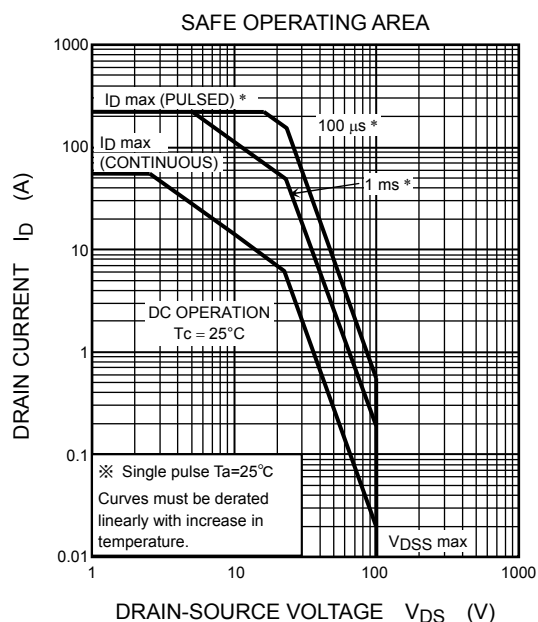
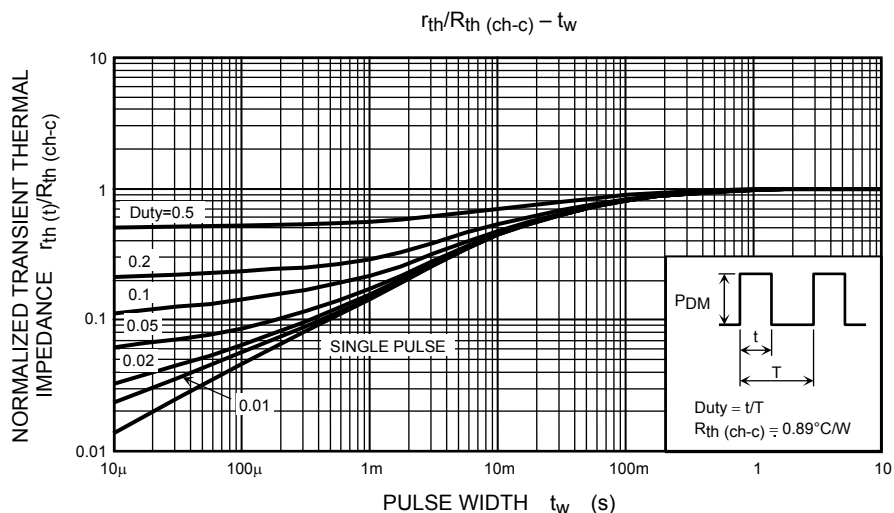
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	$I_{DR}$	—	—	—	55	A
Pulse drain reverse current (Note 1)	$I_{DRP}$	—	—	—	220	A
Forward voltage (diode)	$V_{DSF}$	$I_{DR} = 55 \text{ A}, V_{GS} = 0 \text{ V}$	—	-0.9	-1.2	V
Reverse recovery time	$t_{rr}$	$I_{DR} = 55 \text{ A}, V_{GS} = 0 \text{ V},$	—	67	—	ns
Reverse recovery charge	$Q_{rr}$	$dI_{DR}/dt = 50 \text{ A}/\mu\text{s}$	—	84	—	nC

## Marking









$$R_G = 1\Omega$$

$$V_{DD} = 25\text{ V}, L = 200\mu\text{H}$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left( \frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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