

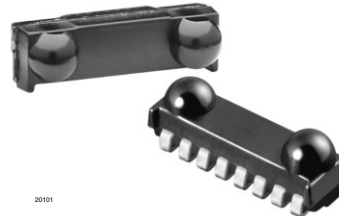
Infrared Transceiver Module (SIR, 115.2 kbit/s) for IrDA® Applications

Description

The TFDU4300 is a low profile (2.5 mm) infrared transceiver module with independent logic reference voltage (V_{logic}) for low voltage IO interfacing. It is compliant to the latest IrDA® physical layer standard for fast infrared data communication, supporting IrDA speeds up to 115.2 kbit/s (SIR) and carrier based remote control. The transceiver module consists of a PIN photodiode, an infrared emitter (IRED), and a low-power control IC to provide a total front-end solution in a single package.

This device covers an extended IrDA low power range of close to 1 m. With an external current control resistor the current can be adjusted for shorter ranges.

This Vishay SIR transceiver is built in a new smaller package using the experiences of the lead frame BabyFace technology.



The RXD output pulse width is independent of the optical input pulse width and stays always at a fixed pulse width thus making the device optimum for standard endecs. TFDU4300 has a tri-state output and is floating in shut-down mode with a weak pull-up.

Features

- Compliant to the latest IrDA physical layer specification (9.6 kbit/s to 115.2 kbit/s) and TV Remote Control, bi-directional operation included.
- Operates from 2.4 V to 5.5 V within specification over full temperature range from - 30 °C to + 85 °C
- Logic voltage 1.5 V to 5.5 V is independent of IRED driver and analog supply voltage
- Split power supply, transmitter and receiver can be operated from two power supplies with relaxed requirements saving costs, US patent no. 6.157.476
- Extended IrDA low power range to about 70 cm
- Typical remote control range 12 m
- Low power consumption (< 0.12 mA supply current)



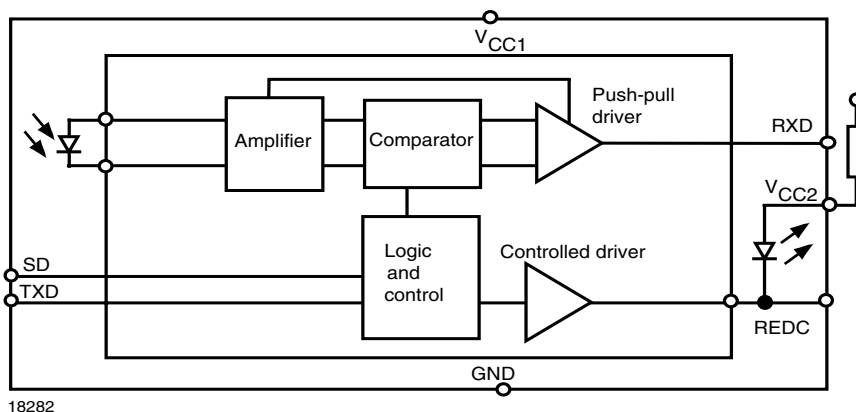
- Power shutdown mode (< 5 μ A shutdown current in full temperature range, up to 85 °C)
- Surface mount package, low profile (2.5 mm) - (L 8.5 mm \times H 2.5 mm \times W 2.9 mm)
- High efficiency emitter
- Low profile (universal) package capable of surface mount soldering to side and top view orientation
- Directly interfaces with various super I/O and controller devices as e.g. TOIM4232
- Tri-state-receiver output, floating in shut down with a weak pull-up
- Compliant with IrDA background light specification
- EMI immunity in GSM bands > 300 V/m verified
- Lead (Pb)-free device
- Qualified for lead (Pb)-free and Sn/Pb processing (MSL4)
- Device in accordance with RoHS 2002/95/EC and WEEE 2002/96EC

Applications

- Ideal for battery operated applications
- Telecommunication products (cellular phones, pagers)
- Digital still and video cameras
- Printers, fax machines, photocopiers, screen projectors
- Medical and industrial data collection
- Diagnostic systems
- Notebook computers, desktop PCs, palmtop computers (Win CE, Palm PC), PDAs
- Internet TV boxes, video conferencing systems
- External infrared adapters (dongles)
- Data loggers
- GPS
- Kiosks, POS, point and pay devices including IrFM - applications

Parts Table

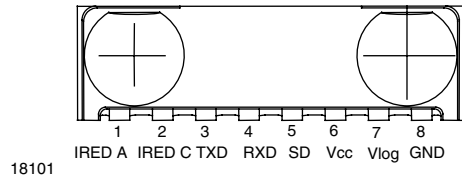
Part	Description	Qty/reel
TFDU4300-TR1	Oriented in carrier tape for side view surface mounting	750 pcs
TFDU4300-TR3	Oriented in carrier tape for side view surface mounting	2500 pcs
TFDU4300-TT1	Oriented in carrier tape for top view surface mounting	750 pcs
TFDU4300-TT3	Oriented in carrier tape for top view surface mounting	2500 pcs

Functional Block Diagram

Pin Description

Pin number	Function	Description	I/O	Active
1	V _{CC2} IRED anode	Connect IRED anode directly to the power supply (V _{CC2}). IRED current can be decreased by adding a resistor in series between the power supply and IRED anode. A separate unregulated power supply can be used at this pin.		Active
2	IRED cathode	IRED Cathode, internally connected to the driver transistor		
3	TXD	This Schmitt-Trigger input is used to transmit serial data when SD is low. An on-chip protection circuit disables the LED driver if the TXD pin is asserted for longer than 300 μ s. The input threshold voltage adapts to and follows the logic voltage swing defined by the applied V _{logic} voltage.	I	High
4	RXD	Received Data Output, push-pull CMOS driver output capable of driving standard CMOS or TTL loads. During transmission the RXD output is inactive. No external pull-up or pull-down resistor is required. Floating with a weak pull-up of 500 k Ω (typ.) in shutdown mode. The voltage swing is defined by the applied V _{logic} voltage	O	Low
5	SD	Shutdown. The input threshold voltage adapts to and follows the logic voltage swing defined by the applied V _{logic} voltage.	I	High
6	V _{CC1}	Supply voltage		
7	V _{logic}	V _{logic} defines the logic voltage level of the I/O ports to adapt the logic voltage swing to the IR controller. The RXD output range is from 0 V to V _{logic} , for optimum noise suppression the inputs- logic decision level is 0.5 x V _{logic}	I	
8	GND	Ground		

Pinout

TFDU4300
weight 75 mg



Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA® operating modes:

SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0

MIR: 576 kbit/s to 1152 kbit/s

FIR: 4 Mbit/s

VFIR: 16 Mbit/s

MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4. A new version of the standard in any case obsoletes the former version.

With introducing the updated versions the old versions are obsolete. Therefore the only valid IrDA® standard is the actual version IrPhy 1.4 (in Oct. 2002).

Absolute Maximum Ratings

Reference point ground (pin 8) unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range, transceiver	- 0.3 V < V _{CC2} < 6 V - 0.5 V < V _{logic} < 6 V	V _{CC1}	- 0.5		+ 6.0	V
Supply voltage range, transmitter	- 0.5 V < V _{CC1} < 6 V - 0.5 V < V _{logic} < 6 V	V _{CC2}	- 0.5		+ 6.0	V
Supply voltage range, V _{logic}	- 0.5 V < V _{CC1} < 6 V - 0.3 V < V _{CC2} < 6 V	V _{logic}	- 0.5		+ 6.0	V
RXD output voltage	- 0.5 V < V _{CC1} < 6 V - 0.3 V < V _{logic} < 6 V	V _{RXD}	- 0.5		V _{logic} + 0.5	V
Voltage at all inputs	Note: V _{in} ≥ V _{CC1} is allowed	V _{IN}	- 0.5		+ 6.0	V
Input current	for all pins, except IRED anode pin				10	mA
Output sinking current					25	mA
Power dissipation	see derating curve	P _D			250	mW
Junction temperature		T _J			125	°C
Ambient temperature range (operating)		T _{amb}	- 30		+ 85	°C
Storage temperature range		T _{stg}	- 40		+ 100	°C
Soldering temperature	see recommended solder profile				260	°C
Average output current, pin 1		I _{IRED(DC)}			125	mA
Repetitive pulsed output current, pin 1 to pin 2	t < 90 μs, t _{on} < 20 %	I _{IRED(RP)}			600	mA

Eye safety information

Parameter	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Virtual source size	Method: (1-1/e) encircled energy	d	1.3	1.8		mm
Maximum intensity for class 1	IEC60825-1 or EN60825-1, edition Jan. 2001, operating below the absolute maximum ratings	I _e			¹⁾ (500) ²⁾	mW/sr

Notes:

¹⁾ Due to the internal limitation measures the device is a "class 1" device under all conditions.

²⁾ IrDA specifies the max. intensity with 500 mW/sr.

Note: We apologize to use sometimes in our documentation the abbreviation LED and the word light emitting diode instead of Infrared Emitting Diode (IRED) for IR-emitters. That is by definition wrong; we are here following just a bad trend.

Typical values are for design aid only, not guaranteed nor subject to production testing and may vary with time.

Electrical Characteristics

Transceiver

Tested at $T_{amb} = 25^{\circ}\text{C}$, $V_{CC1} = V_{CC2} = 2.7\text{ V}$ to 5.5 V unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Remark: For $2.4\text{ V} < V_{CC1} < 2.6\text{ V}$ at $T_{amb} < -25^{\circ}\text{C}$ a minor reduction of the receiver sensitivity may occur	V_{CC1}	2.4		5.5	V
Idle supply current at V_{CC1} (receive mode, no signal)	SD = Low, $E_e = 1\text{ klx}^{(1)}$, $T_{amb} = -25^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC1} = V_{CC2} = 2.7\text{ V}$ to 5.5 V	I_{CC1}		90	130	μA
	SD = Low, $E_e = 1\text{ klx}^{(1)}$, $T_{amb} = 25^{\circ}\text{C}$, $V_{CC1} = V_{CC2} = 2.7\text{ V}$ to 5.5 V	I_{CC1}		75		μA
Idle supply current at V_{logic} (receive mode, no signal)	SD = Low, $E_e = 1\text{ klx}^{(1)}$, V_{log} , pin 7, no signal, no load at RXD	I_{log}			1	μA
Average dynamic supply current, transmitting	$I_{IRED} = 300\text{ mA}$, 20 % Duty Cycle	I_{CC1}			0.65	mA
Standby supply current	SD = High, $T = 25^{\circ}\text{C}$, $E_e = 0\text{ klx}$	I_{SD}			0.1	μA
	SD = High, $T = 70^{\circ}\text{C}$	I_{SD}			2	μA
	SD = High, $T = 85^{\circ}\text{C}$	I_{SD}			3	μA
Standby supply current, V_{logic}	no signal, no load	I_{log}			1	μA
Operating temperature range		T_A	- 30		+ 85	$^{\circ}\text{C}$
Output voltage low, RXD	$C_{Load} = 15\text{ pF}$	V_{OL}	- 0.5		$0.15 \times V_{logic}$	V
Output voltage high, RXD	$I_{OH} = -500\text{ }\mu\text{A}$	V_{OH}	$0.8 \times V_{logic}$		$V_{logic} + 0.5$	V
	$I_{OH} = -250\text{ }\mu\text{A}$, $C_{Load} = 15\text{ pF}$	V_{OH}	$0.9 \times V_{logic}$		$V_{logic} + 0.5$	V
RXD to V_{CC1} impedance		R_{RXD}	400	500	600	$\text{k}\Omega$
Input voltage low (TXD, SD)		V_{IL}	- 0.5		0.5	V
Input voltage high (TXD, SD)	CMOS level ²⁾ , $V_{logic} \geq 2.5\text{ V}$	V_{IH}	$V_{logic} - 0.5$		6	V
Input voltage high (TXD, SD)	CMOS level ²⁾ , $V_{logic} < 2.5\text{ V}$	V_{IH}	$0.8 \times V_{logic}$		6	V
Input leakage current (TXD, SD)	$V_{IN} = 0.9 \times V_{logic}$	I_{ICH}	- 2		+ 2	μA
Controlled pull down current	SD, TXD = "0" to "1", $V_{IN} < 0.15 V_{logic}$	I_{IRTx}			+ 150	μA
	SD, TXD = "0" to "1", $V_{IN} > 0.7 V_{logic}$	I_{IRTx}	- 1	0	1	μA
Input capacitance (TXD, SD)		C_{IN}			5	pF

Notes:

¹⁾ Standard illuminant A.

²⁾ To provide an improved immunity with increasing V_{logic} the typical threshold level is increasing with V_{logic} and set to $0.5 \times V_{logic}$. It is recommended to use the specified min/max values to avoid increased operating current.

Optoelectronic Characteristics

Receiver

Tested at $T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{CC1} = V_{CC2} = 2.7\text{ V}$ to 5.5 V unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Minimum irradiance E_e in angular range ²⁾	9.6 kbit/s to 115.2 kbit/s $\lambda = 850\text{ nm}$ to 900 nm ; $\alpha = 0^{\circ}, 15^{\circ}$	E_e		40 (4)	80 (8)	mW/m^2 ($\mu\text{W}/\text{cm}^2$)
Maximum Irradiance E_e In Angular Range ³⁾	$\lambda = 850\text{ nm}$ to 900 nm	E_e		5 (500)		kW/m^2 (mW/cm^2)
Maximum no detection irradiance ¹⁾	$\lambda = 850\text{ nm}$ to 900 nm $t_r, t_f < 40\text{ ns}$, $t_{po} = 1.6\text{ }\mu\text{s}$ at $f = 115\text{ kHz}$, no output signal allowed	E_e	4 (0.4)			mW/m^2 ($\mu\text{W}/\text{cm}^2$)
Rise time of output signal	10 % to 90 %, $C_L = 15\text{ pF}$	$t_{r(RXD)}$	20		100	ns
Fall time of output signal	90 % to 10 %, $C_L = 15\text{ pF}$	$t_{f(RXD)}$	20		100	ns
RXD pulse width of output signal	input pulse length $> 1.2\text{ }\mu\text{s}$	t_{PW}	1.65	2.0	3.0	μs
Stochastic jitter, leading edge	input irradiance = $100\text{ mW}/\text{m}^2$, $\leq 115.2\text{ kbit/s}$				250	ns
Standby/shutdown delay, receiver startup time	after shutdown active or power-on				150	μs
Latency		t_L		100	150	μs

Notes:

¹⁾ Equivalent to IrDA background light and electromagnetic field test: fluorescent lighting immunity.

²⁾ IrDA sensitivity definition: **minimum irradiance E_e in angular range**, power per unit area. The receiver must meet the BER specification while the source is operating at the minimum intensity in angular range into the minimum half-angular range at the maximum link length.

³⁾ **Maximum irradiance E_e in angular range**, power per unit area. The optical delivered to the detector by a source operating at the maximum intensity in angular range at minimum link length must not cause receiver overdrive distortion and possible related link errors. If placed at the active output interface reference plane of the transmitter, the receiver must meet its bit error ratio (BER). For more definitions see the document "Symbols and Terminology" on the Vishay website (<http://www.vishay.com/doc?82512>).

Transmitter

Tested at $T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{CC1} = V_{CC2} = 2.7\text{ V}$ to 5.5 V unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test conditions	Symbol	Min.	Typ.	Max.	Unit
IREDA operating current limitation	No external resistor for current limitation ¹⁾	I_D	250	300	350	mA
Forward voltage of built-in IRED	$I_f = 300\text{ mA}$	V_f	1.4	1.8	1.9	V
Output leakage IRED current	$\text{TXD} = 0\text{ V}$, $0 < V_{CC1} < 5.5\text{ V}$	I_{IRED}	- 1		1	μA
Output radiant intensity	$\alpha = 0^{\circ}, 15^{\circ}$ $\text{TXD} = \text{High}$, $\text{SD} = \text{Low}$	I_e	30	65		mW/sr
	$V_{CC1} = 5.0\text{ V}$, $\alpha = 0^{\circ}, 15^{\circ}$ $\text{TXD} = \text{Low}$ or $\text{SD} = \text{High}$ (Receiver is inactive as long as $\text{SD} = \text{High}$)	I_e			0.04	mW/sr
Output radiant intensity, angle of half intensity		α		± 24		$^{\circ}$
Peak - emission wavelength ²⁾		λ_p	880		900	nm
Spectral bandwidth		$\Delta\lambda$		45		nm
Optical rise time, fall time		t_{ropt}, t_{fopt}			100	ns
Optical output pulse duration	input pulse width $1.6 < t_{\text{TXD}} < 20\text{ }\mu\text{s}$	t_{opt}	$t_{\text{TXD}} - 0.15$		$t_{\text{TXD}} + 0.15$	μs
	input pulse width $t_{\text{TXD}} \geq 20\text{ }\mu\text{s}$	t_{opt}		20	300	μs
Optical overshoot					25	%

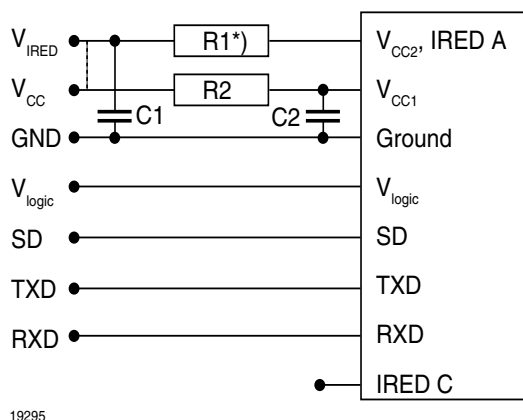
Notes:

¹⁾ Using an external current limiting resistor is allowed and recommended to reduce IRED intensity and operating current when current reduction is intended to operate at the IrDA low power conditions. E.g. for $V_{CC2} = 3.3\text{ V}$ a current limiting resistor of $R_S = 56\text{ }\Omega$ will allow a power minimized operation at IrDA low power conditions.

²⁾ Note: Due to this wavelength restriction compared to the IrDA spec of 850 nm to 900 nm the transmitter is able to operate as source for the standard remote control applications with codes as e.g. Phillips RC5/RC6[®] or RECS 80.

Recommended Circuit Diagram

Operated with a clean low impedance power supply the TFDU4300 needs no additional external components. However, depending on the entire system design and board layout, additional components may be required (see figure 1).



19295

Figure 1. Recommended Application Circuit

*) R1 is optional when reduced intensity is used

The capacitor C1 is buffering the supply voltage and eliminates the inductance of the power supply line. This one should be a Tantalum or other fast capacitor to guarantee the fast rise time of the IRED current. The resistor R1 is the current limiting resistor, which may be used to reduce the operating current to levels below the specified controlled values for saving battery power.

Vishay's transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring should be avoided. The shutdown input must be grounded for normal operation, also when the shutdown function is not used.

Table 1.

Recommended Application Circuit Components

Component	Recommended value	Vishay part number
C1	4.7 μ F, 16 V	293D 475X9 016B
C2	0.1 μ F, Ceramic	VJ 1206 Y 104 J XXMT
R1	depends on current to be adjusted	
R2	47 Ω , 0.125 W	CRCW-1206-47R0-F-RT1

The inputs (TXD, SD) and the output RXD should be directly connected (DC - coupled) to the I/O circuit. The capacitor C2 combined with the resistor R2 is the low pass filter for smoothing the supply voltage. R2, C1 and C2 are optional and dependent on the quality of the supply voltages VCC1 and injected noise. An unstable power supply with dropping voltage during transmission may reduce the sensitivity (and transmission range) of the transceiver.

The placement of these parts is critical. It is strongly recommended to position C2 as close as possible to the transceiver pins.

When extended wiring is used as in bench tests the inductance of the power supply can cause dynamically a voltage drop at VCC2. Often some power supplies are not able to follow the fast current rise time. In that case another 4.7 μ F (type, see table under C1) at VCC2 will be helpful.

Under extreme EMI conditions as placing an RF-transmitter antenna on top of the transceiver, we recommend to protect all inputs by a low-pass filter, as a minimum a 12 pF capacitor, especially at the RXD port. The transceiver itself withstands EMI at a GSM frequencies above 500 V/m. When interference is observed, the wiring to the inputs picks it up. It is verified by DPI measurements that as long as the interfering RF - voltage is below the logic threshold levels of the inputs and equivalent levels at the outputs no interferences are expected.

One should keep in mind that basic RF - design rules for circuits design should be taken into account. Especially longer signal lines should not be used without termination. See e.g. "The Art of Electronics" Paul Horowitz, Winfield Hill, 1989, Cambridge University Press, ISBN: 0521370957.

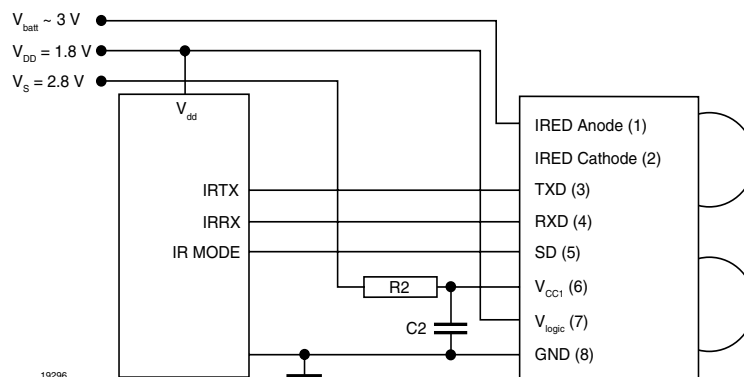


Figure 2. Typical application circuit

Figure 2 shows an example of a typical application for to work with low voltage logic (connected to V_{DD}), a separate supply voltage V_S and using the transceiver with the IRED Anode connected to the unregulated battery V_{batt} . This method reduces the peak load of the regulated power supply and saves therefore costs. Alternatively all supplies can also be tied to only one voltage source. R1 and C1 are not used in this case and are depending on the circuit design in most cases not necessary.

I/O and Software

In the description, already different I/Os are mentioned. Different combinations are tested and the function verified with the special drivers available from the I/O suppliers. In special cases refer to the I/O manual, the Vishay application notes, or contact directly Vishay Sales, Marketing or Application. For operating at RS232 ports the ENDEC TOIM4232 is recommended.

Current Derating Diagram

Figure 3 shows the maximum operating temperature when the device is operated without external current limiting resistor.

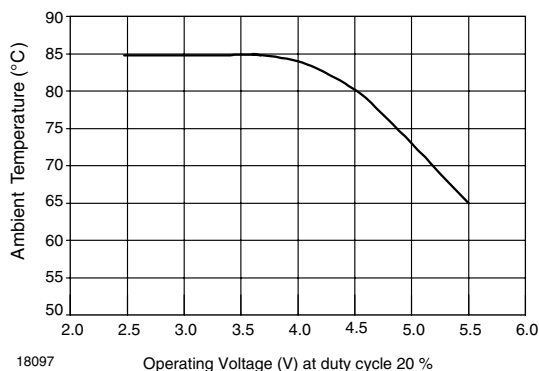


Figure 3. Current Derating Diagram

Table 2. Truth table

Inputs			Outputs		Remark
SD	TXD	Optical input irradiance mW/m ²	RXD	Transmitter	Operation
high > 1 ms	x	x	weakly pulled (500 kΩ) to V_{CC1}	0	Shutdown
low	high	x	high inactive	I_e	Transmitting
low	high > 50 μs	x	high inactive	0	Protection is active
low	low	< 4	high inactive	0	Ignoring low signals below the IrDA [®] defined threshold for noise immunity
low	low	> Min. irradiance E_e < Max. irradiance E_e	low (active)	0	Response to an IrDA [®] compliant optical input signal
low	low	> Max. Irradiance E_e	undefined	0	Overload conditions can cause unexpected outputs

Recommended Solder Profiles

Solder Profile for Sn/Pb Soldering

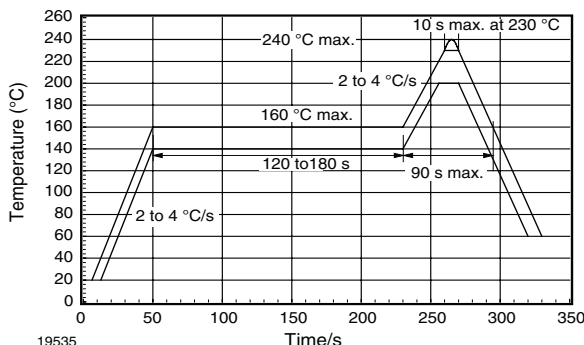


Figure 4. Recommended Solder Profile for Sn/Pb soldering

Lead (Pb)-free, Recommended Solder Profile

The TFDU4300 is a lead (Pb)-free transceiver and qualified for lead (Pb)-free processing. For lead (Pb)-free solder paste like Sn (3.0 - 4.0) Ag (0.5 - 0.9) Cu, there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown below in figure 5 and 6 are VISHAY's recommended profiles for use with the TFDU4300 transceivers. For more details please refer to the application note "SMD Assembly Instructions" (<http://www.vishay.com/doc?82602>).

A ramp-up rate less than 0.9 °C/s is not recommended. Ramp-up rates faster than 1.3 °C/s could damage an optical part because the thermal conductivity is less than compared to a standard IC.

Wave Soldering

For TFDUxxxx and TFBSxxxx transceiver devices wave soldering is not recommended.

Manual Soldering

Manual soldering is the standard method for lab use. However, for a production process it cannot be recommended because the risk of damage is highly dependent on the experience of the operator. Nevertheless, we added a chapter to the above mentioned application note, describing manual soldering and desoldering.

Storage

The storage and drying processes for all VISHAY transceivers (TFDUxxxx and TFBSxxx) are equivalent to MSL4.

The data for the drying procedure is given on labels on the packing and also in the application note "Taping, Labeling, Storage and Packing" (<http://www.vishay.com/doc?82601>).

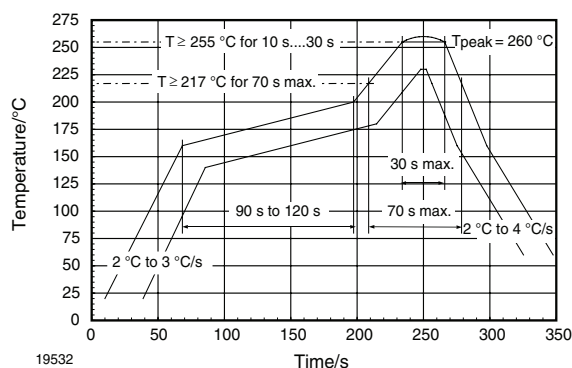


Figure 5. Solder Profile, RSS Recommendation

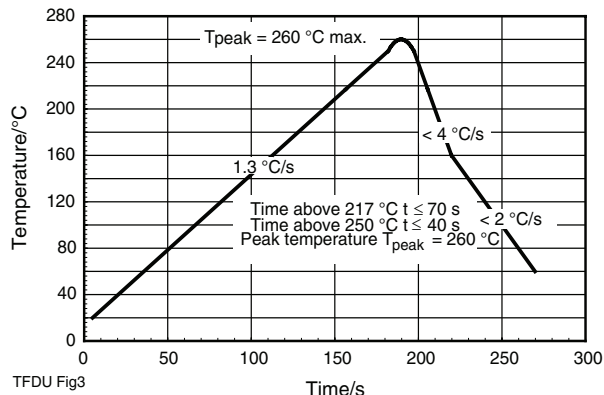
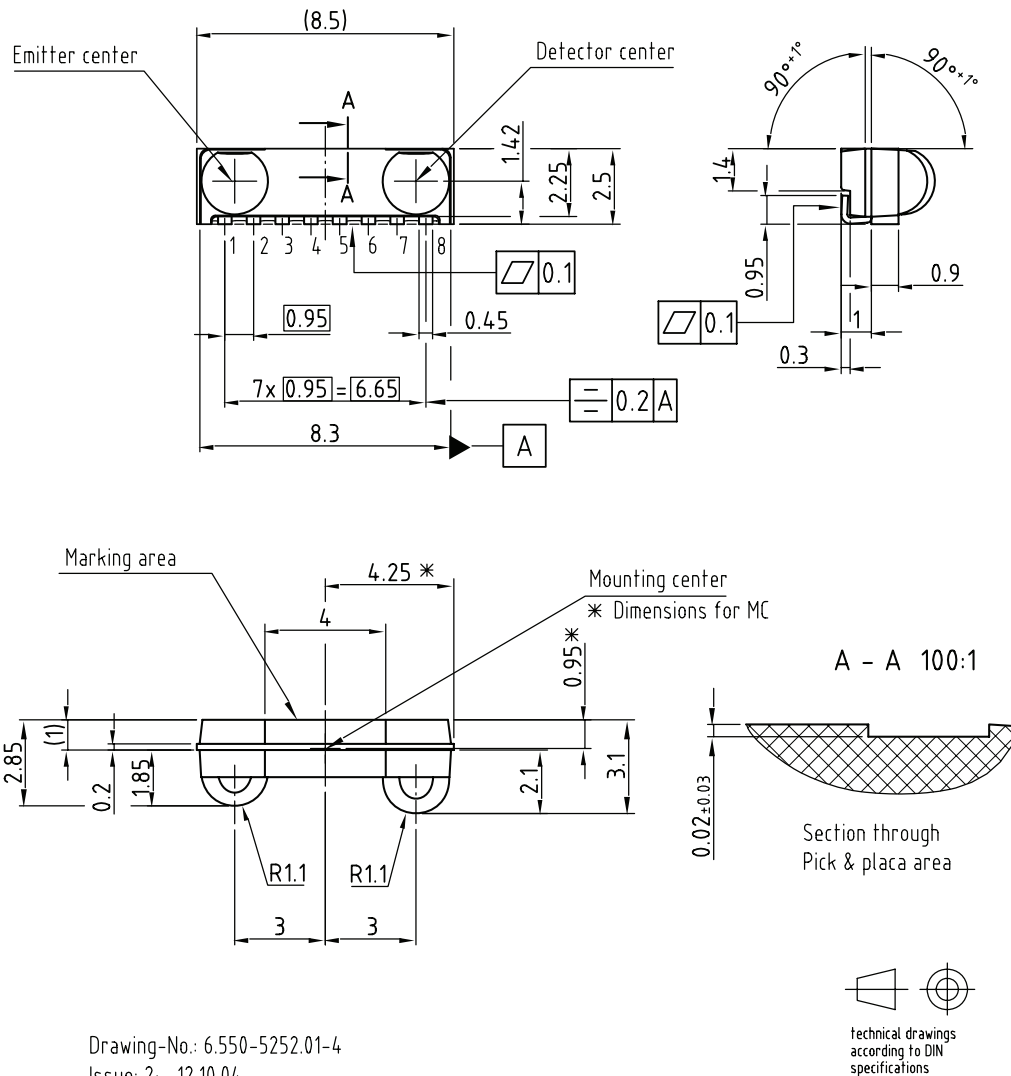


Figure 6. RTS Recommendation

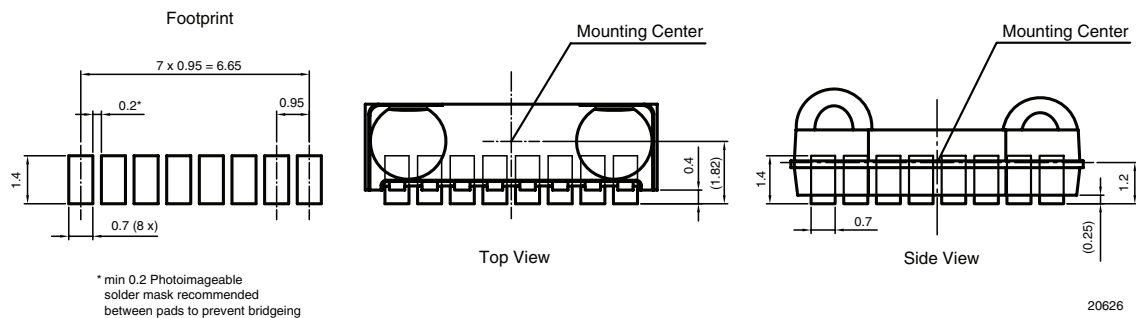
Package Dimensions in mm



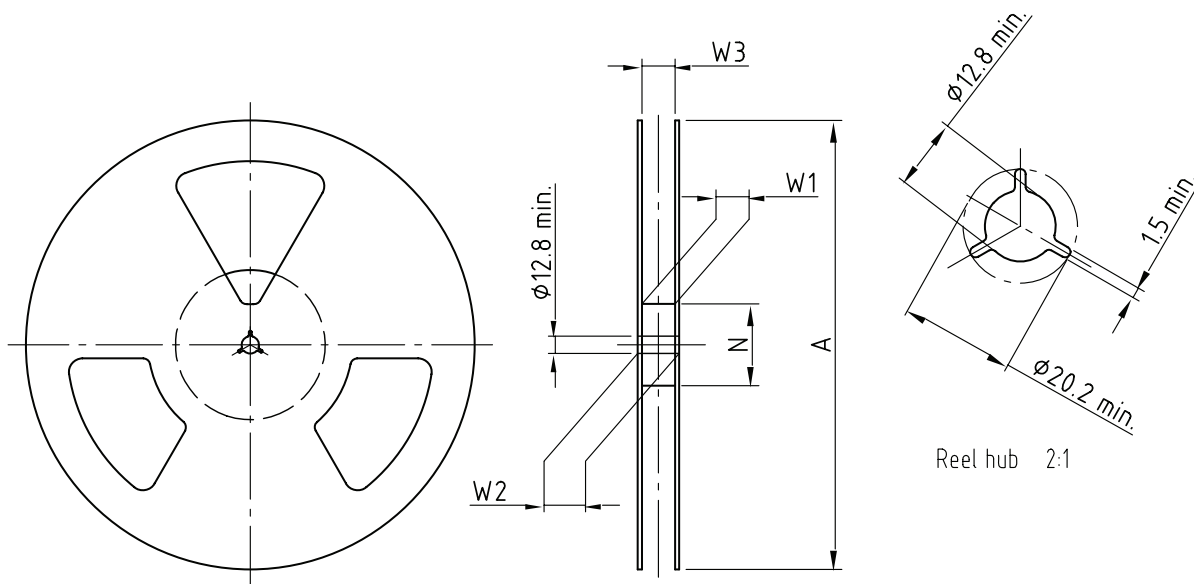
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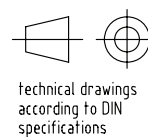
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Reel Dimensions in mm


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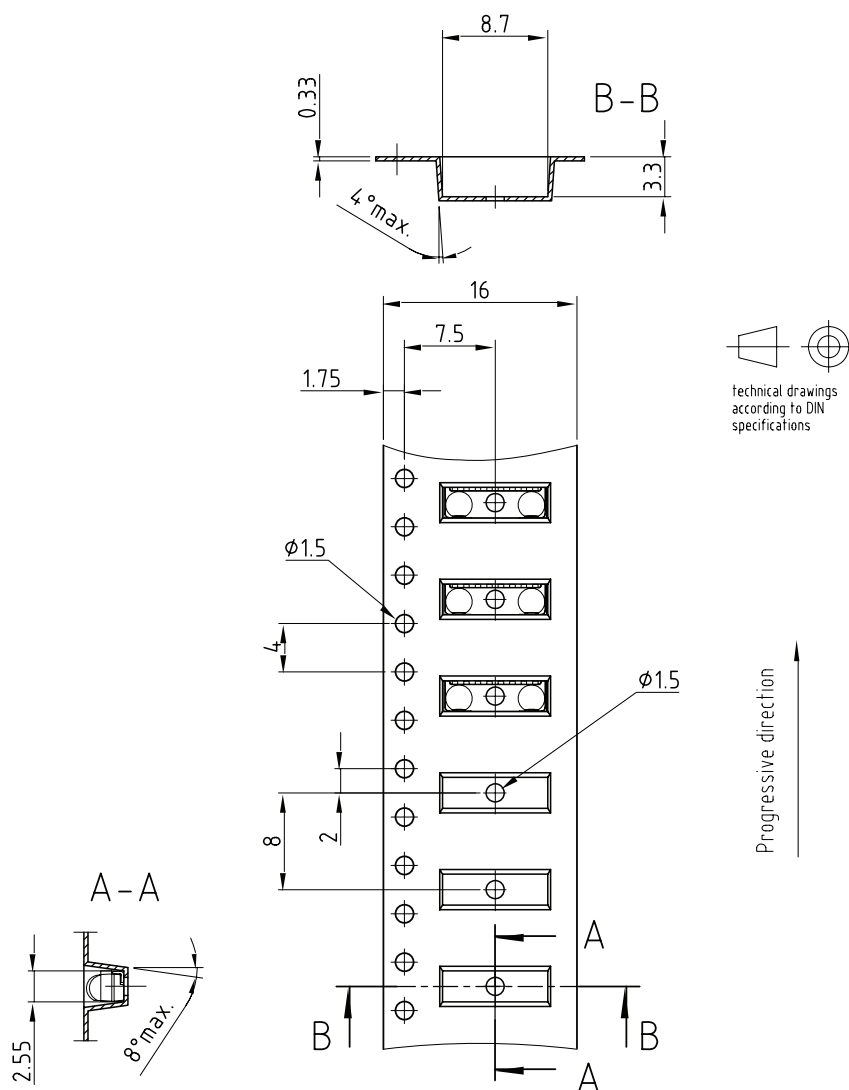
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of the wheel is supplier specific.

Dimension acc. to IEC EN 60 286-3



Tape width	A max.	N	W_1 min.	W_2 max.	W_3 min.	W_3 max.
mm	mm	mm	mm	mm	mm	mm
16	180	60	16.4	22.4	15.9	19.4
16	330	50	16.4	22.4	15.9	19.4

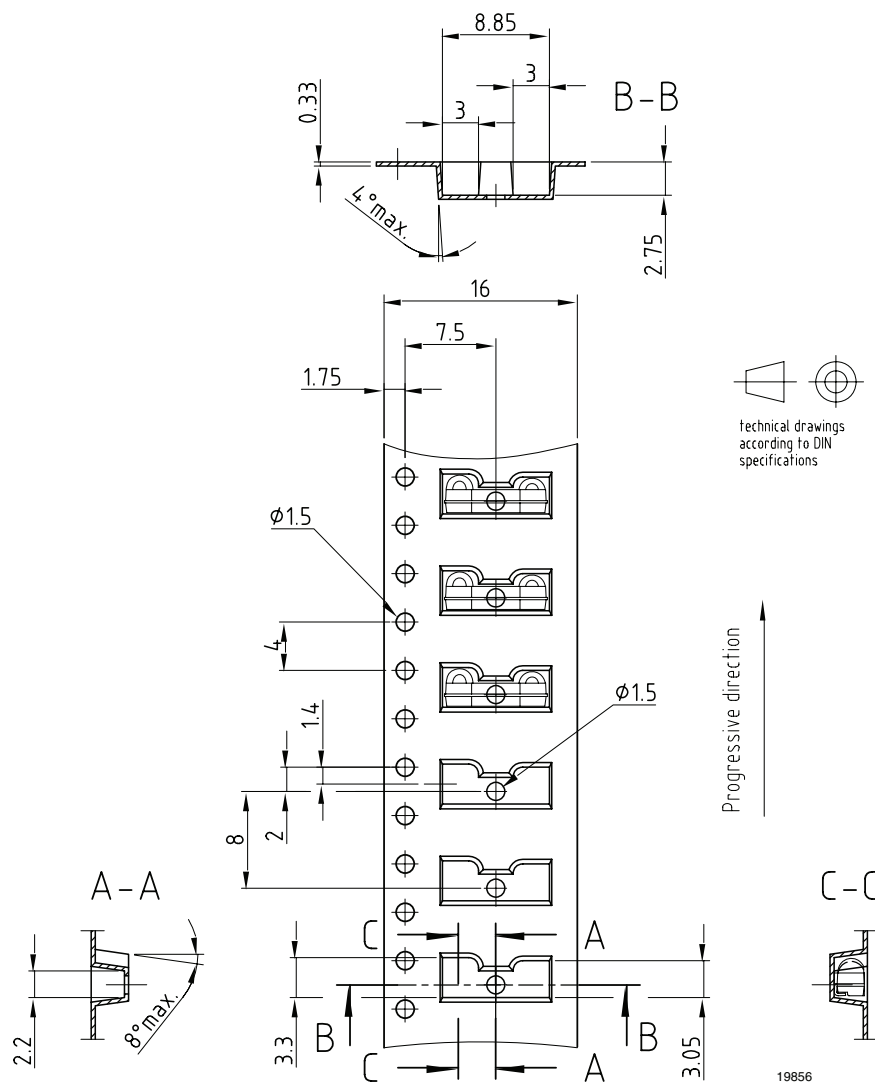
Tape Dimensions in mm



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Figure 7. Tape drawing, TFDU4300 for top view mounting



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Figure 8. Tape drawing, TFDU4300 for side view mounting



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