TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7WT74FU

D-Type Flip-Flop with Preset and Clear

The TC7WT74FU is high speed CMOS D-TYPE FLIP-FLOP fabricated with silicon gate CMOS technology.

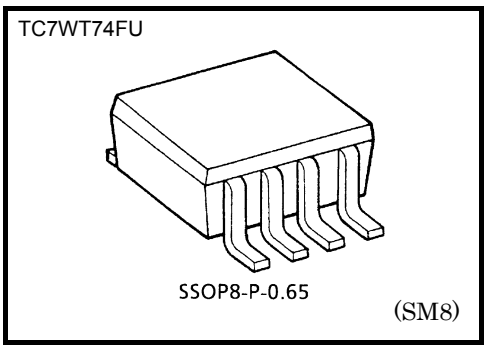
It achieves the high speed operation similar to equivalent Bipolar schottky TTL while maintaining the CMOS low power dissipation.

The input threshold levels are compatible with TTL output voltage.

The signal level applied to the D-INPUT is tranceferred to Q-OUTPUT during the positive going trasition of the CK pulse.

CLEAR and PRESET are independent of the CK and are accompished by setting the appropriate input low.

All inputs are equipped with protection circuits against static dichage or transient excess voltage.



Weight
SSOP8-P-0.65: 0.02 g (typ.)

Features

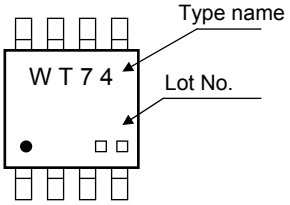
- High speed: f_{MAX} = 53 MHz(typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 2 μA (max) at Ta = 25°C
- Compatible with TTL inputs: V_{IL} = 0.8 V(max) at Ta=25°C
- Output drive capability: 10 LSTTL Loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)

Absolute Maximum Ratings (Ta = 25°C)

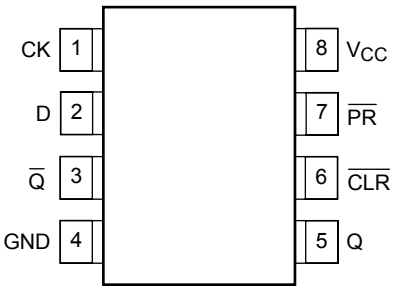
Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±25	mA
Power dissipation	P_D	300	mW
Storage temperature	T_{stg}	−65 to 150	°C
Lead temperature (10s)	T_L	260	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Marking



Pin Assignment (top view)

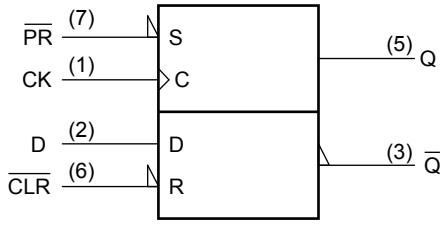


Truth Table

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Qn	$\overline{Q}$n	No Change

X: Don't care

Logic Diagram



Operating Ranges

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 500	ns

DC Electrical Characteristics

Characteristics		Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
				V_{CC} (V)	Min	Typ.	Max	Min	Max	
Input voltage	High level	V_{IH}	—	4.5 to 5.5	2.0	—	—	2.0	—	V
	Low level	V_{IL}	—	4.5 to 5.5	—	—	0.8	—	0.8	
Output voltage	High level	V_{OH}	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −20 μA	4.5	4.4	4.5	—	4.4	—	V
			V_{IN} = V_{IL} or V_{IH}, I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
	Low level	V_{OL}	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 20 μA	4.5	—	0.0	0.10	—	0.10	V
			V_{IN} = V_{IL} or V_{IH}, I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
Input leakage current		I_{IN}	V_{IN} = V_{CC} or GND	5.5	—	—	±0.1	—	±1	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND	5.5	—	—	2.0	—	20.0	μA
		I_{CCT}	PER INPUT: V_{IN} = 0.5 V or 2.4V; OTHER INPUT: V_{CC} or GND	5.5	—	—	2.0	—	2.9	mA

Timing Requirements (Input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ	LIMIT	LIMIT	
Minimum pulse width (CLOCK)	$t_W(L)$	—	4.5	—	25	29	ns
	$t_W(H)$		5.5	—	20	23	
Minimum pulse width ($\overline{CLR}$, $\overline{PR}$)	$t_W(L)$	—	4.5	—	30	34	ns
			5.5	—	25	28	
Minimum set-up time	t_S	—	4.5	—	25	29	ns
			5.5	—	20	23	
Minimum hold time	t_h	—	4.5	—	10	10	ns
			5.5	—	8	8	
Minimum removal time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}	—	4.5	—	10	10	ns
			5.5	—	10	10	
Clock frequency	f	—	4.5	—	22	16	MHz
			5.5	—	25	19	

AC Electrical Characteristics (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH}	—	—	6	12	ns
	t_{THL}					
Propagation delay time (CLOCK – Q, $\overline{Q}$)	t_{PLH}	—	—	17	28	ns
	t_{PHL}					
Propagation delay time ($\overline{CLR}$, $\overline{PR}$ – Q, $\overline{Q}$)	t_{PLH}	—	—	20	30	ns
	t_{PHL}					
Maximum clock frequency	f_{MAX}	—	24	53	—	MHz

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH}	—	4.5	—	8	15	—	19	ns
	t_{THL}		5.5	—	7	13	—	16	
Propagation delay time (CLOCK – Q, $\overline{Q}$)	t_{PLH}	—	4.5	—	21	33	—	41	ns
	t_{PHL}		5.5	—	19	30	—	37	
Propagation delay time ($\overline{CLR}$, $\overline{PR}$ – Q, $\overline{Q}$)	t_{PLH}	—	4.5	—	23	35	—	43	ns
	t_{PHL}		5.5	—	20	32	—	40	
Maximum clock frequency	f_{MAX}	—	4.5	22	48	—	16	—	MHz
			5.5	25	53	—	19	—	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD}	(Note)		—	34	—	—	—	pF

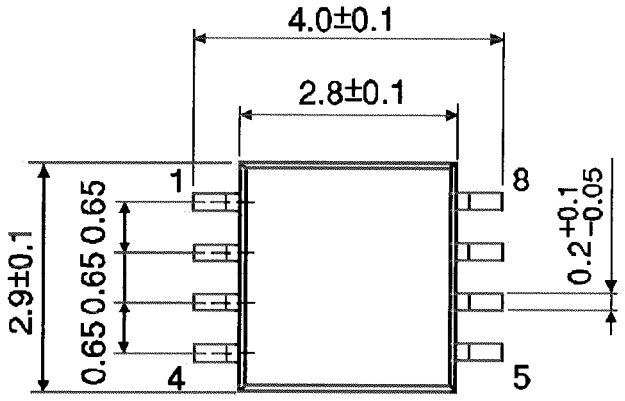
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

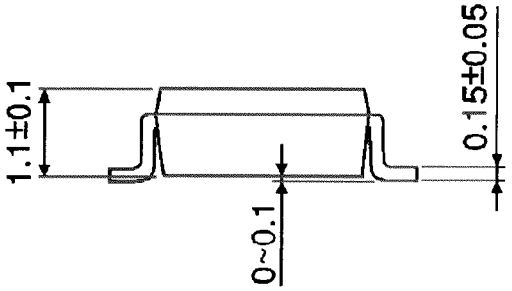
Average operating current can be obtained by the equation:

$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

SSOP8-P-0.65 Unit : mm





Weight: 0.02 g (typ.)

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20070701-EN GENERAL

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