TOSHIBA CMOS Digital Integrated Circuit   Silicon Monolithic

TC74VCX162373FT

Low-Voltage 16-Bit D-Type Latch with 3.6-V Tolerant Inputs and Outputs

The TC74VCX162373FT is a high-performance CMOS 16-bit D-type latch. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is also designed with overvoltage tolerant inputs and outputs up to 3.6 V.

This 16-bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$) which are common to each byte. It can be used as two 8-bit latches or one 16-bit latch. When the $\overline{OE}$ input is high, the outputs are in a high-impedance state.

The 26-Ω series resistor helps reducing output overshoot and undershoot without external resistor.

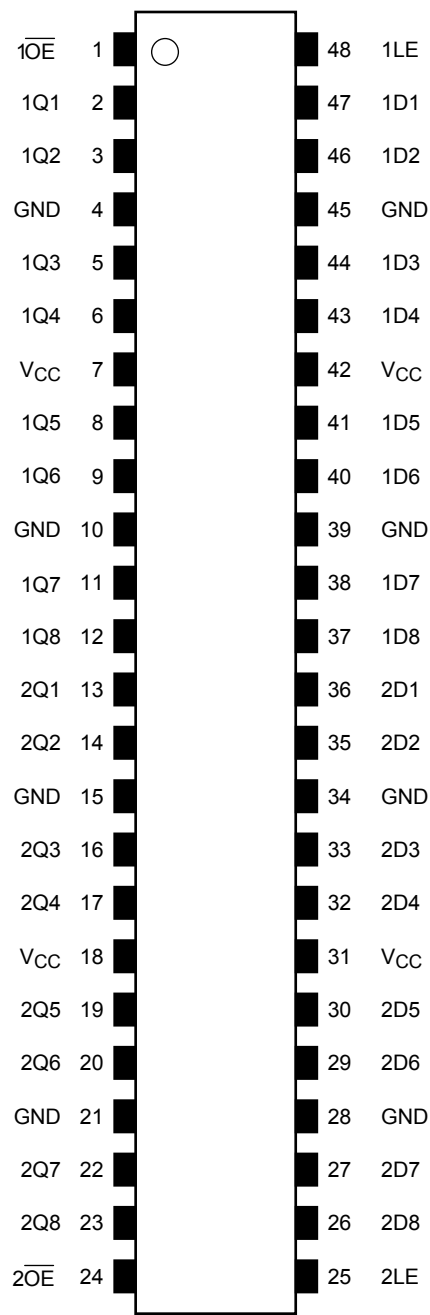All inputs are equipped with protection circuits against static discharge.
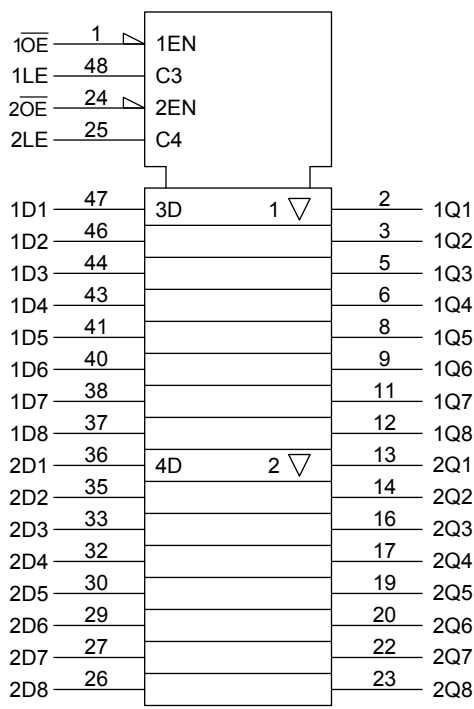
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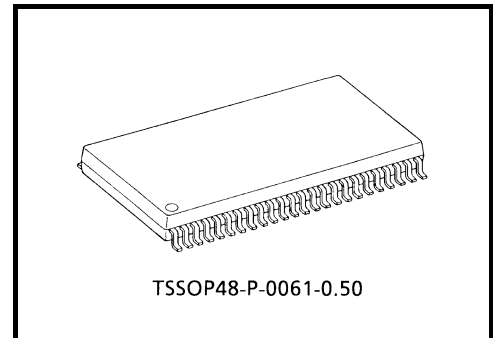
Weight: 0.25 g (typ.)

Features

- 26-Ω series resistors on outputs
- Low-voltage operation: V_{CC} = 1.8 to 3.6 V
- High-speed operation: t_{pd} = 3.3 ns (max) (V_{CC} = 3.0 to 3.6 V)
    - : t_{pd} = 4.5 ns (max) (V_{CC} = 2.3 to 2.7 V)
    - : t_{pd} = 5.8 ns (max) (V_{CC} = 1.8 V)
- Output current: I_{OH}/I_{OL} = ±12 mA (min) (V_{CC} = 3.0 V)
    - : I_{OH}/I_{OL} = ±8 mA (min) (V_{CC} = 2.3 V)
    - : I_{OH}/I_{OL} = ±4 mA (min) (V_{CC} = 1.8 V)
- Latch-up performance: ±300 mA
- ESD performance：Machine model > ±200 V
    - ：Human body model > ±2000 V
- Package: TSSOP (thin shrink small outline package)
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs

Pin Assignment (top view)

1$\overline{\text{OE}}$	1		48	1LE
1Q1	2		47	1D1
1Q2	3		46	1D2
GND	4		45	GND
1Q3	5		44	1D3
1Q4	6		43	1D4
V_{CC}	7		42	V_{CC}
1Q5	8		41	1D5
1Q6	9		40	1D6
GND	10		39	GND
1Q7	11		38	1D7
1Q8	12		37	1D8
2Q1	13		36	2D1
2Q2	14		35	2D2
GND	15		34	GND
2Q3	16		33	2D3
2Q4	17		32	2D4
V_{CC}	18		31	V_{CC}
2Q5	19		30	2D5
2Q6	20		29	2D6
GND	21		28	GND
2Q7	22		27	2D7
2Q8	23		26	2D8
2$\overline{\text{OE}}$	24		25	2LE

IEC Logic Symbol

Input	Pin	Label
1$\overline{\text{OE}}$	1	1EN
1LE	48	C3
2$\overline{\text{OE}}$	24	2EN
2LE	25	C4

Input	Pin		Output	Pin
1D1	47	3D	1Q1	2
1D2	46		1Q2	3
1D3	44		1Q3	5
1D4	43		1Q4	6
1D5	41		1Q5	8
1D6	40		1Q6	9
1D7	38		1Q7	11
1D8	37		1Q8	12
2D1	36	4D	2Q1	13
2D2	35		2Q2	14
2D3	33		2Q3	16
2D4	32		2Q4	17
2D5	30		2Q5	19
2D6	29		2Q6	20
2D7	27		2Q7	22
2D8	26		2Q8	23

Truth Table

Inputs			Outputs
1$\overline{OE}$	1LE	1D1-1D8	1Q1-1Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

Inputs			Outputs
2$\overline{OE}$	2LE	2D1-2D8	2Q1-2Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram
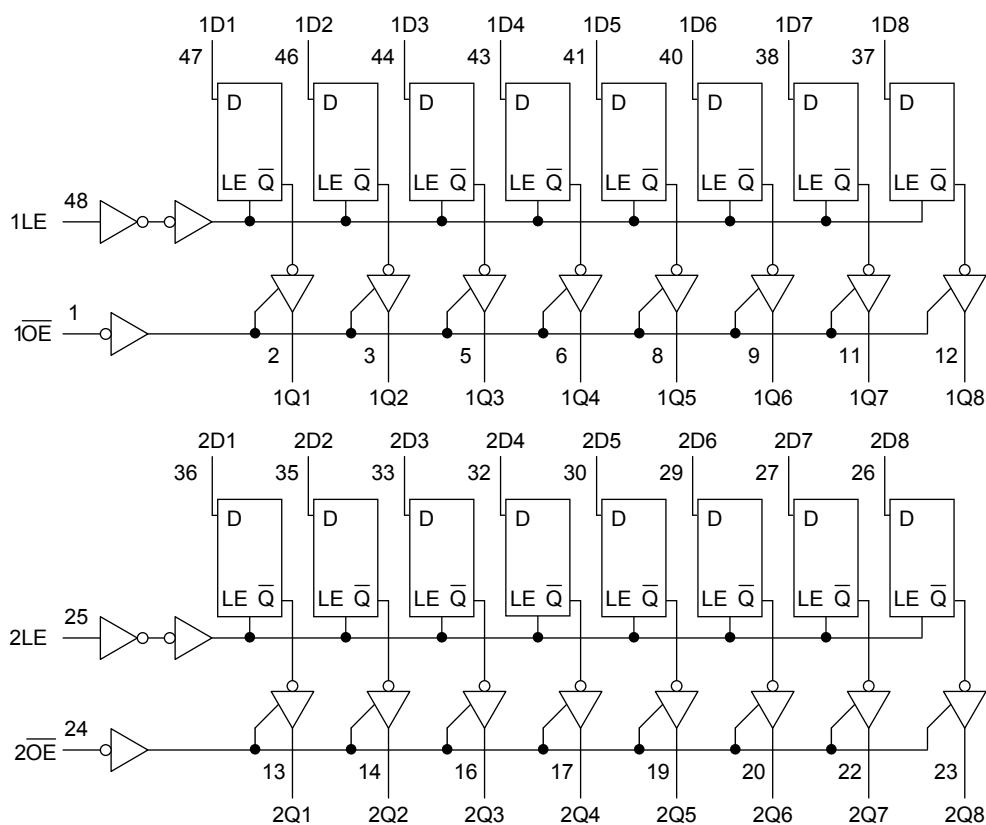
Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 4.6	V
DC input voltage	V_{IN}	−0.5 to 4.6	V
DC output voltage	V_{OUT}	−0.5 to 4.6 (Note 2) −0.5 to V_{CC} + 0.5 (Note 3)	V
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	±50 (Note 4)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	400	mW
DC V_{CC}/ground current per supply pin	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: OFF state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: V_{OUT} < GND, V_{OUT} > V_{CC}

Recommended Operating Range (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.8 to 3.6 1.2 to 3.6 (Note 2)	V
Input voltage	V_{IN}	−0.3 to 3.6	V
Output voltage	V_{OUT}	0 to 3.6 (Note 3) 0 to V_{CC} (Note 4)	V
Output current	I_{OH}/I_{OL}	±12 (Note 5) ±8 (Note 6) ±4 (Note 7)	mA
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 8)	ns/V

Note 1: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Note 2: Data retention only

Note 3: OFF state

Note 4: High or low state

Note 5: V_{CC} = 3.0 to 3.6 V

Note 6: V_{CC} = 2.3 to 2.7 V

Note 7: V_{CC} = 1.8 V

Note 8: V_{IN} = 0.8 to 2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = −40 to 85°C, 2.7 V < V_{CC} ≦ 3.6 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		2.7 to 3.6	2.0	—	V
	L-level	V_{IL}	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.7 to 3.6	V_{CC} − 0.2	—	V
				I_{OH} = −6 mA	2.7	2.2	—	
				I_{OH} = −8 mA	3.0	2.4	—	
				I_{OH} = −12 mA	3.0	2.2	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7 to 3.6	—	0.2	
				I_{OL} = 6 mA	2.7	—	0.4	
				I_{OL} = 8 mA	3.0	—	0.55	
				I_{OL} = 12 mA	3.0	—	0.8	
Input leakage current		I_{IN}	V_{IN} = 0 to 3.6 V		2.7 to 3.6	—	±5.0	μA
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		2.7 to 3.6	—	±10.0	μA
Power-off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.7 to 3.6	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.7 to 3.6	—	±20.0	
Increase in I_{CC} per input		ΔI_{CC}	V_{IH} = V_{CC} − 0.6 V		2.7 to 3.6	—	750	

DC Characteristics (Ta = −40 to 85°C, 2.3 V ≦ V_{CC} ≦ 2.7 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		2.3 to 2.7	1.6	—	V
	L-level	V_{IL}	—		2.3 to 2.7	—	0.7	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.3 to 2.7	V_{CC} − 0.2	—	V
				I_{OH} = −4 mA	2.3	2.0	—	
				I_{OH} = −6 mA	2.3	1.8	—	
				I_{OH} = −8 mA	2.3	1.7	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.3 to 2.7	—	0.2	
				I_{OL} = 6 mA	2.3	—	0.4	
				I_{OL} = 8 mA	2.3	—	0.6	
Input leakage current		I_{IN}	V_{IN} = 0 to 3.6 V		2.3 to 2.7	—	±5.0	μA
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		2.3 to 2.7	—	±10.0	μA
Power-off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.3 to 2.7	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.3 to 2.7	—	±20.0	

DC Characteristics (Ta = −40 to 85°C, 1.8 V ≦ V_{CC} < 2.3 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		1.8 to 2.3	0.7 × V_{CC}	—	V
	L-level	V_{IL}	—		1.8 to 2.3	—	0.2 × V_{CC}	
Output voltage	H-level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100$ μA	1.8	V_{CC} − 0.2	—	V
				$I_{OH} = -4$ mA	1.8	1.4	—	
	L-level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100$ μA	1.8	—	0.2	
				$I_{OL} = 4$ mA	1.8	—	0.3	
Input leakage current		I_{IN}	$V_{IN} = 0$ to 3.6 V		1.8	—	±5.0	μA
3-state output OFF state current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to 3.6 V		1.8	—	±10.0	μA
Power-off leakage current		I_{OFF}	V_{IN}, $V_{OUT} = 0$ to 3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	$V_{IN} = V_{CC}$ or GND		1.8	—	20.0	μA
			$V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6$ V		1.8	—	±20.0	

AC Characteristics (Ta = −40 to 85°C, input: $t_r = t_f$ = 2.0 ns, C_L = 30 pF, R_L = 500 Ω) (Note 1)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Propagation delay time (D-Q)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.8	1.5	5.8	ns
			2.5 ± 0.2	1.0	4.5	
			3.3 ± 0.3	0.8	3.3	
Propagation delay time (LE-Q)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.8	1.5	6.2	ns
			2.5 ± 0.2	1.0	4.9	
			3.3 ± 0.3	0.8	3.6	
3-state output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.8	1.5	7.6	ns
			2.5 ± 0.2	1.0	5.4	
			3.3 ± 0.3	0.8	3.9	
3-state output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.8	1.5	5.3	ns
			2.5 ± 0.2	1.0	4.4	
			3.3 ± 0.3	0.8	4.0	
Minimum pulse width (LE)	$t_{w (H)}$	Figure 1, Figure 2	1.8	3.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum setup time	t_s	Figure 1, Figure 2	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time	t_h	Figure 1, Figure 2	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 2)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 2: Parameter guaranteed by design.
$(t_{osLH} = |t_{pLHm} − t_{pLHn}|, t_{osHL} = |t_{pHLm} − t_{pHLn}|)$

Dynamic Switching Characteristics (Ta = 25°C, input: t_r = t_f = 2.0 ns, C_L = 30 pF)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	V_{IH} = 1.8 V, V_{IL} = 0 V	(Note)	1.8	0.15	V
		V_{IH} = 2.5 V, V_{IL} = 0 V	(Note)	2.5	0.25	
		V_{IH} = 3.3 V, V_{IL} = 0 V	(Note)	3.3	0.35	
Quiet output minimum dynamic V_{OL}	V_{OLV}	V_{IH} = 1.8 V, V_{IL} = 0 V	(Note)	1.8	−0.15	V
		V_{IH} = 2.5 V, V_{IL} = 0 V	(Note)	2.5	−0.25	
		V_{IH} = 3.3 V, V_{IL} = 0 V	(Note)	3.3	−0.35	
Quiet output minimum dynamic V_{OH}	V_{OHV}	V_{IH} = 1.8 V, V_{IL} = 0 V	(Note)	1.8	1.55	V
		V_{IH} = 2.5 V, V_{IL} = 0 V	(Note)	2.5	2.05	
		V_{IH} = 3.3 V, V_{IL} = 0 V	(Note)	3.3	2.65	

Note: Parameter guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	1.8, 2.5, 3.3	6	pF
Output capacitance	C_O	—	1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz (Note)	1.8, 2.5, 3.3	20	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$I_{CC \, (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16$ (per bit)

AC Test Circuit

Parameter	Switch	
t_{pLH}, t_{pHL}	Open	
t_{pLZ}, t_{pZL}	6.0 V $V_{CC} \times 2$	@V_{CC} = 3.3 ± 0.3 V @V_{CC} = 2.5 ± 0.2 V @V_{CC} = 1.8 V
t_{pHZ}, t_{pZH}	GND	
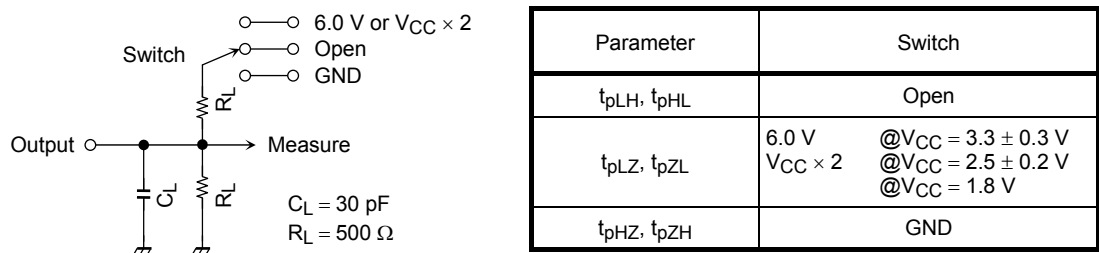
Figure 1

AC Waveform
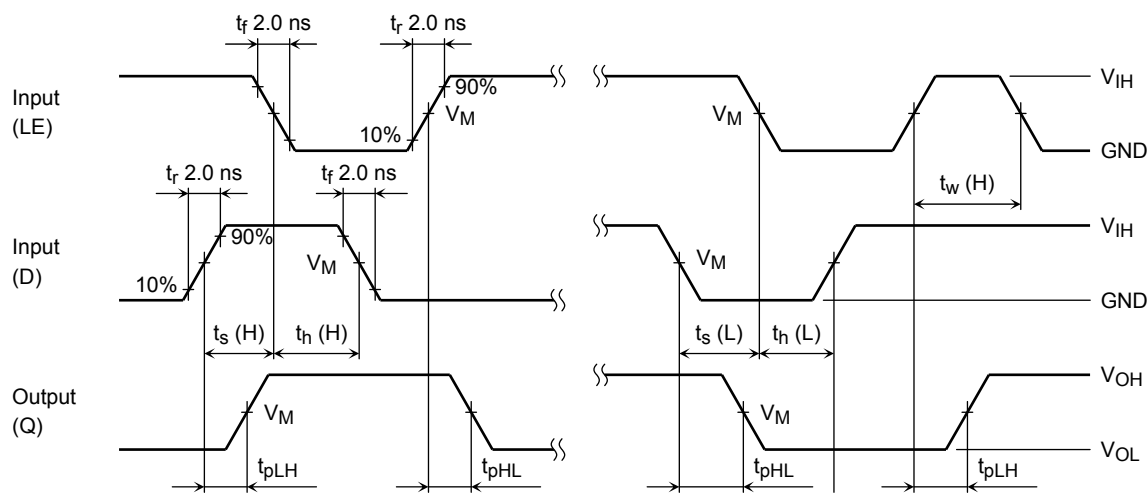
Figure 2 t_{pLH}, t_{pHL}, t_w, t_s, t_h
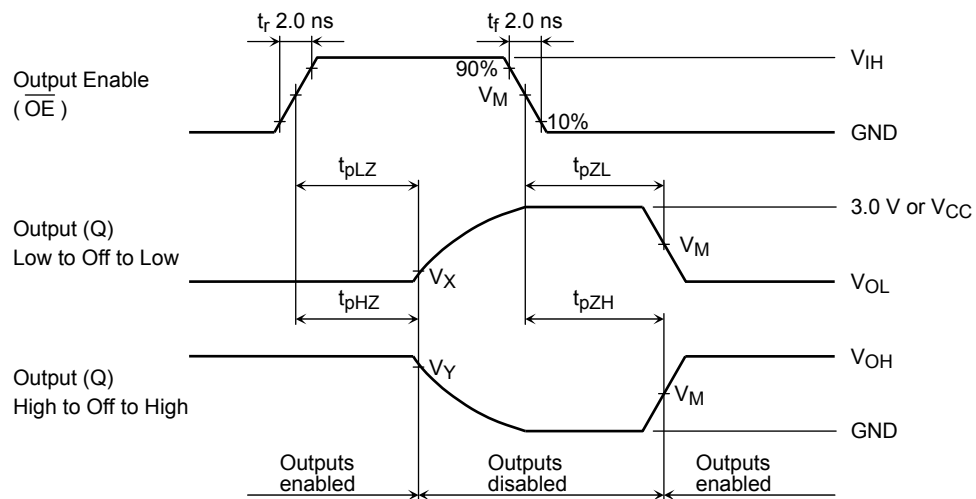
Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Symbol	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3$ V	$V_{OL} + 0.15$ V	$V_{OL} + 0.15$ V
V_Y	$V_{OH} - 0.3$ V	$V_{OH} - 0.15$ V	$V_{OH} - 0.15$ V

Package Dimensions

TSSOP48-P-0061-0.50

Unit : mm

12.8MAX
12.5±0.1
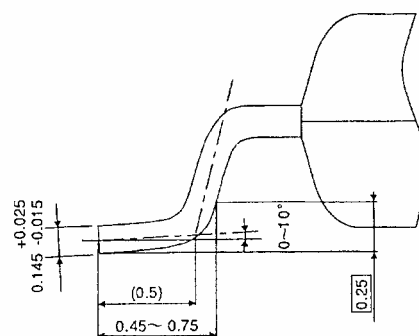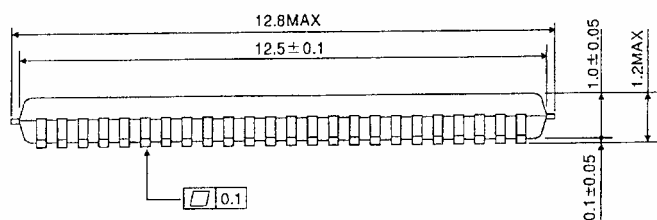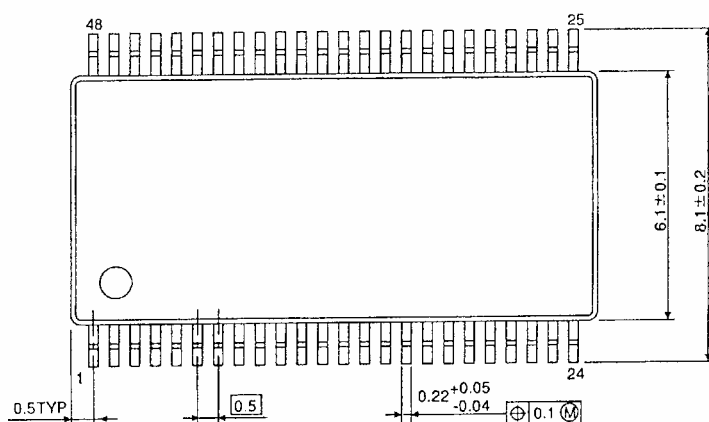
Weight: 0.25 g (typ.)

Note: Lead (Pb)-Free Packages

TSSOP48-P-0061-0.50

RESTRICTIONS ON PRODUCT USE