TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# **TC74LCX16373AFT**

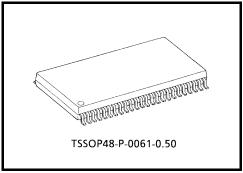
#### Low-Voltage 16-Bit D-Type Latch with 5-V Tolerant Inputs and Outputs

The TC74LCX16373AFT is a high-performance CMOS 16-bit D-type latch. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage  $(3.3\ V)\ VCC$  applications, but it could be used to interface to 5-V supply environment for both inputs and outputs.

This 16-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ( $\overline{OE}$ ) which are common to each byte. It can be used as two 8-bit latches or one 16-bit latch. When the  $\overline{OE}$  input is high, the outputs are in a high-impedance state.

All inputs are equipped with protection circuits against static discharge.

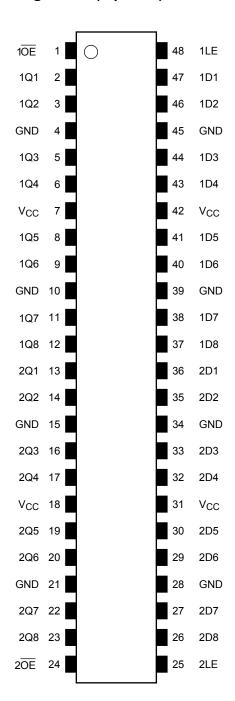


Weight: 0.25 g (typ.)

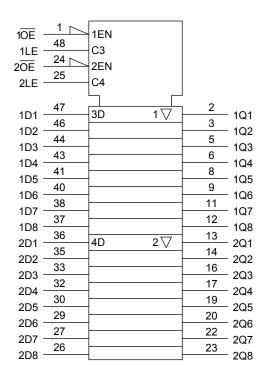
#### **Features**

- Low-voltage operation: V<sub>CC</sub> = 2.0 to 3.6 V
- High-speed operation:  $t_{pd} = 7.0 \text{ ns (max) (V}_{CC} = 3.0 \text{ to } 3.6 \text{ V)}$
- Ouput current:  $|I_{OH}|/I_{OL} = 24 \text{ mA (min)} (V_{CC} = 3.0 \text{ V})$
- Latch-up performance: ±500 mA
- · Package: TSSOP (thin shrink small outline package)
- · Power-down protection provided on all inputs and outputs

### Pin Assignment (top view)



### **IEC Logic Symbol**



#### **Truth Table**

	Outputs		
1OE	1LE	1D1-1D8	1Q1-1Q8
Н	Х	Х	Z
L	L	Х	Qn
L	Н	L	L
L	Н	Н	Н

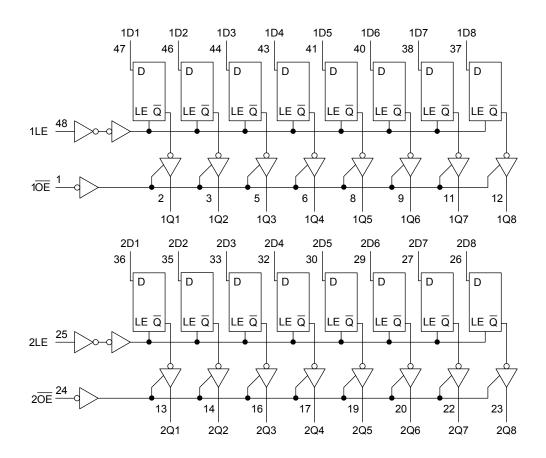
	Outputs		
2OE	2LE	2D1-2D8	2Q1-2Q8
Н	X	Х	Z
L	L	Х	Qn
L	Н	L	L
L	Н	Н	Н

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level

### **System Diagram**



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### **Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	−0.5 to 7.0	V
Input voltage	V <sub>IN</sub>	-0.5 to 7.0	V
		-0.5 to 7.0 (Note 2)	
Output voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
		(Note 3)	
Input diode current	I <sub>IK</sub>	-50	mA
Output diode current	lok	±50 (Note 4)	mA
DC output current	lout	±50	mA
Power dissipation	P <sub>D</sub>	400	mW
DC V <sub>CC</sub> /ground current per supply pin	I <sub>CC</sub> /I <sub>GND</sub>	±100	mA
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: Output in OFF state

Note 3: High or low state. IOUT absolute maximum rating must be observed.

Note 4:  $V_{OUT} < GND, V_{OUT} > V_{CC}$ 

### **Recommended Operating Conditions (Note 1)**

Characteristics	Symbol	Rating	Unit		
Power supply voltage	V <sub>CC</sub>	2.0 to 3.6	V		
Tower supply voltage	VCC	1.5 to 3.6 (Note 2)	V		
Input voltage	V <sub>IN</sub>	0 to 5.5	V		
Output voltage	V	0 to 5.5 (Note 3)	٧		
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub> (Note 4)	V		
Output current	la/la.	±24 (Note 5)	mA		
Output current	I <sub>OH</sub> /I <sub>OL</sub>	±12 (Note 6)	ША		
Operating temperature	T <sub>opr</sub>	-40 to 85	°C		
Input rise and fall time	dt/dv	0 to 10 (Note 7)	ns/V		

Note 1: The recommended operating conditions are required to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.

Note 2: Data retention only

Note 3: Output in OFF state

Note 4: High or low state

Note 5:  $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$ 

Note 6:  $V_{CC} = 2.7 \text{ to } 3.0 \text{ V}$ 

Note 7:  $V_{IN} = 0.8$  to 2.0 V,  $V_{CC} = 3.0$  V



### **Electrical Characteristics**

# DC Characteristics ( $Ta = -40 \text{ to } 85^{\circ}\text{C}$ )

Characteris	tics	Symbol	Test Condition			Min	Max	Unit	
	1				V <sub>CC</sub> (V)				
Input voltage	H-level	$V_{IH}$	-	_	2.7 to 3.6	2.0	_	V	
mpat voltage	L-level	V <sub>IL</sub>	-	_	2.7 to 3.6	_	0.8	V	
				$I_{OH} = -100 \mu A$	2.7 to 3.6	V <sub>CC</sub> - 0.2	l		
	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$I_{OH} = -12 \text{ mA}$	2.7	2.2	_		
				$I_{OH} = -18 \text{ mA}$	3.0	2.4			
Output voltage				$I_{OH} = -24 \text{ mA}$	3.0	2.2	_	V	
	V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$I_{OL} = 100 \mu A$	2.7 to 3.6	_	0.2			
			$I_{OL} = 12 \text{ mA}$	2.7	_	0.4			
	L-level	V <sub>OL</sub>	AIM = AIH OL AIT	AOF AIM = AIH OLAIF	$I_{OL} = 16 \text{ mA}$	3.0	_	0.4	
				I <sub>OL</sub> = 24 mA	3.0	_	0.55		
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 0 to 5.5 V		2.7 to 3.6	_	±5.0	μА	
2 state output OFF at			V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		2.7 to 3.6		15.0	^	
3-state output OFF state current		IOZ	$I_{OZ}$ $V_{OUT} = 0$ to 5.5 V		2.7 10 3.6	_	±5.0	μА	
Power-off leakage cur	rent	loff	$V_{IN}/V_{OUT} = 5.5 \text{ V}$		0	_	10.0	μΑ	
Quiescent supply curr	pply current $I_{CC} = \frac{V_{IN} = V_{CC} \text{ or GND}}{V_{IN}/V_{OUT} = 3.6 \text{ to } 5.5 \text{ V}}$		2.7 to 3.6	_	20.0				
Quiescent Supply Curi			2.7 to 3.6	_	±20.0	μΑ			
Increase in Icc per inp	out	Δl <sub>CC</sub>	$V_{IH} = V_{CC} - 0.6 V$		2.7 to 3.6	_	500		

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# AC Characteristics ( $Ta = -40 \text{ to } 85^{\circ}\text{C}$ )

Characteristics	Characteristics Symbol Test Condition			Min	Max	Unit
Characteristics	Symbol Took condition	V <sub>CC</sub> (V)	IVIIII	IVIAX	Offic	
Propagation delay time	t <sub>pLH</sub>	Figure 1, Figure 2	2.7	_	8.0	ns
(D-Q)	$t_{pHL}$	rigure 1, rigure 2	$3.3 \pm 0.3$	1.5	7.0	115
Propagation delay time	$t_{pLH}$	Figure 1, Figure 2	2.7	_	8.0	ns
(LE-Q)	$t_{pHL}$	rigure 1, rigure 2	$3.3 \pm 0.3$	1.5	7.0	110
3-state output enable time	$t_{pZL}$	Figure 1 Figure 3	2.7	_	8.2	ns
3-state output enable time	t <sub>pZH</sub>	t <sub>pZH</sub> Figure 1, Figure 3	$3.3 \pm 0.3$	1.5	7.2	110
3-state output disable time	t <sub>pLZ</sub>	pLZ Figure 4 Figure 2	2.7	_	8.2	ns
3-state output disable time	t <sub>pHZ</sub>	Figure 1, Figure 3	$3.3 \pm 0.3$	1.5	7.2	115
Minimum pulse width	+ (山)	Figure 1, Figure 2	2.7	4.0		ns
(LE)	t <sub>w</sub> (H)	rigure 1, rigure 2	$3.3 \pm 0.3$	3.0		110
Minimum setup time	ts	Figure 1, Figure 2	2.7	2.5		ns
willimum setup time	ıs		$3.3 \pm 0.3$	2.5		110
Minimum hold time	+.	Figure 1, Figure 2	2.7	1.5		ns
Willimani noid time	t <sub>h</sub>	rigure 1, rigure 2	$3.3 \pm 0.3$	1.5		115
Output to output skow	t <sub>osLH</sub>	(Noto)	2.7	_		ns
Output to output skew	t <sub>osHL</sub>	(Note)	$3.3 \pm 0.3$	_	1.0	115

Note: Parameter guaranteed by design.

 $(t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|)$ 

### **Dynamic Switching Characteristics**

(Ta = 25°C, input:  $t_r = t_f = 2.5$  ns,  $C_L = 50$  pF,  $R_L = 500$  Ω)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	8.0	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V

### **Capacitive Characteristics (Ta = 25°C)**

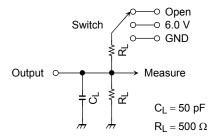
Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Input capacitance	C <sub>IN</sub>	_	3.3	7	pF
Output capacitance	C <sub>OUT</sub>	_	3.3	8	pF
Power dissipation capacitance	C <sub>PD</sub>	$f_{IN} = 10 \text{ MHz}$ (No	te) 3.3	25	pF

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16 \text{ (per bit)}$ 

#### **AC Test Circuit**



Parameter	Switch
t <sub>pLH</sub> , t <sub>pHL</sub>	Open
$t_{pLZ}$ , $t_{pZL}$	6.0 V
t <sub>pHZ</sub> , t <sub>pZH</sub>	GND
$t_W$ , $t_S$ , $t_h$ ,	Open

Figure 1

#### **AC Waveform**

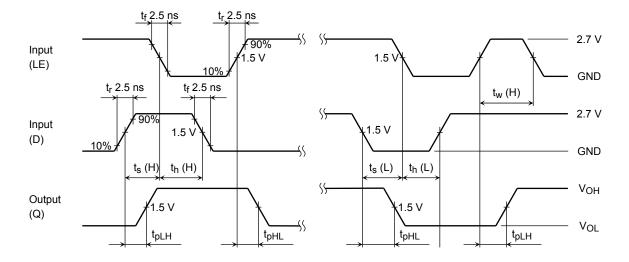


Figure 2 t<sub>pLH</sub>, t<sub>pHL</sub>, t<sub>w</sub>, t<sub>s</sub>, t<sub>h</sub>

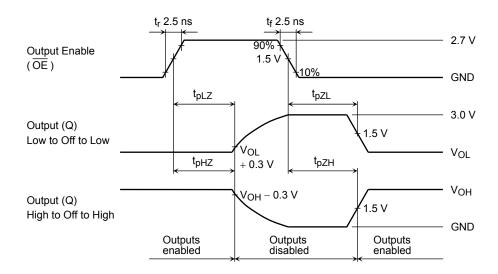
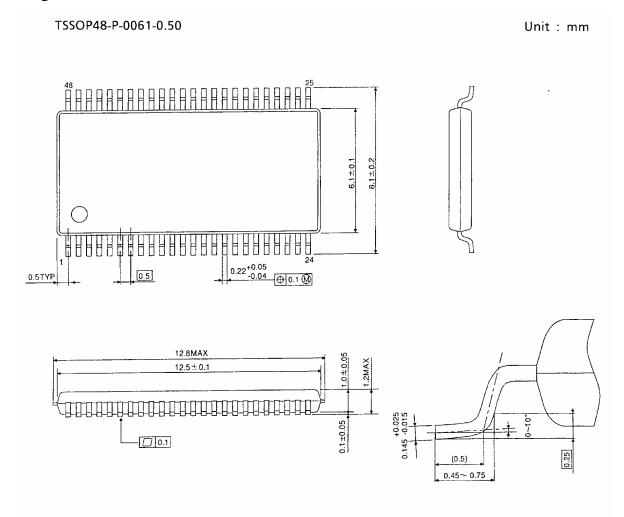


Figure 3  $t_{\text{pLZ}},\,t_{\text{pHZ}},\,t_{\text{pZL}},\,t_{\text{pZH}}$ 

# **Package Dimensions**



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Weight: 0.25 g (typ.)

Note: Lead (Pb)-Free Packages

TSSOP48-P-0061-0.50

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