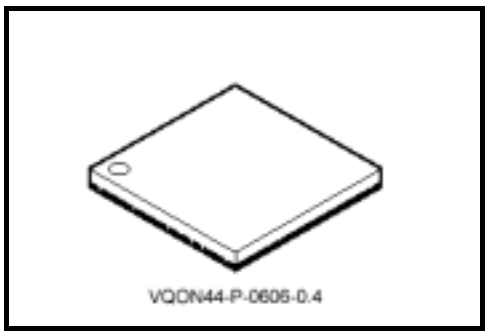
TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TENTATIVE

TB6613FTG

DC Motor Driver, Stepping Motor Driver

TB6613FTG is a driver IC for DC motors, with low on-resistance LDMOS as output drive transistors.
The TB6613FTG incorporates five constant current-controlled H-bridge with PWM system. Four H-bridges are also available for μ-Step stepping motor controllong among them.
(Two stepping motors in maximum case.)
The TB6613FTG makes it ideal for controlling actuators of lenses in DSC or other applications.
The TB6613FTG supports three-wire serial data comunication thus reducing the number of lines for interfacing the IC.



Weight: 0.05 g (Typ.)

Features

- Motor power supply Voltage: V_M ≤ 6V (max)
- Control power supply Voltage: V_{CC} = 3V to 6V
- Output Current I_{out} ≤ 0.8 A (Max)
- Pch/Nch LDMOS complementally output transistors
- Output on-resistance: Ron (upper and lower) = (1.5) Ω (@VM=Vcc=5V, Typ.)

【 ch. A, B, C, D 】

・Four H-bridges with PWM constant current control system,
for controlling two bipolar type stepping motor(STM) or four actuator maximum.
・H-sw mode or STM mode is selectable with setting of serial data.
・In STM mode, two resolution mode are selectable,
6bit (256steps/360deg electrical angle) or 1bit (8steps/360deg electrical angle)

【 ch. E 】

・One H-bridge with PWM constant current control system.
・Constant current reference voltage (Vref) is set with internal 6bit DAC.

【 Others 】

・Constant current reference voltage setting DAC for each channel is included.
・Independent stand-by (power save) circuit is included.
・Thermal shutdown circuit is included.(TSD: Shutdown the output bias on detecting the internal junction at 170deg Celsius)
・Low voltage malfunction prevention circuit is included. (Shutdown circuit UVLO: Vcc≤ (2.2V: Typ.))
・Small package VQON44(Pitch=0.4mm)
・For lead-free reflow mounting

Note: This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

Block Diagram

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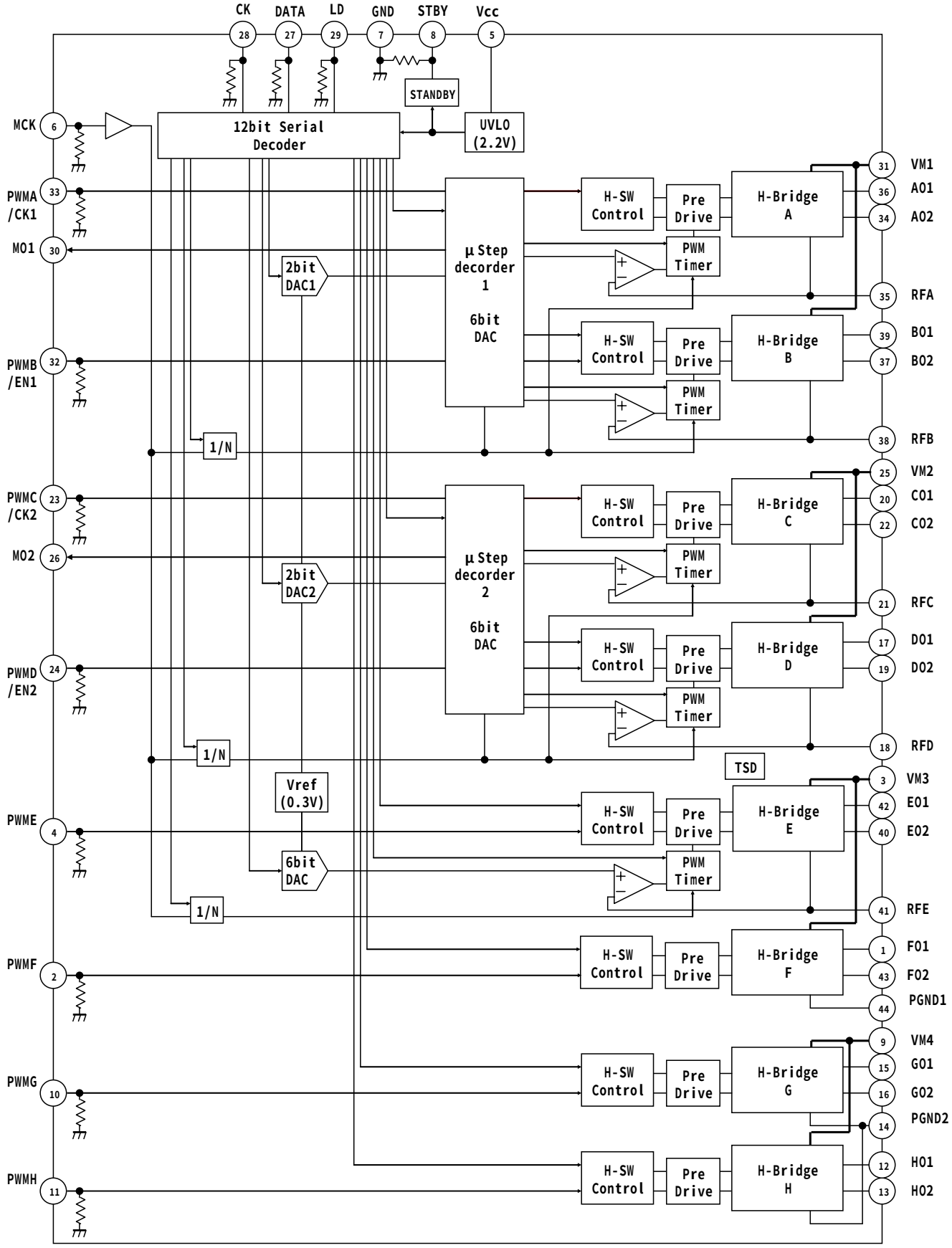

Pin Function

No.	Pin name	I/O	Function	No.	Pin name	I/O	Function
1	FO1	O	F ch output pin 1	23	PWMC /CK2	I	PWM signal input pin(C ch) / Clock for μStep input pin 2
2	PWMF	I	PWM signal input pin (F ch)	24	PWMD /EN2	I	PWM signal input pin(D ch) / STM enable signal input pin 2
3	VM3	-	Motor Power Supply Voltage pin 3(E,Fch)	25	VM2	-	Motor Power Supply Voltage pin 2(C,Dch)
4	PWME	I	PWM signal input pin(E ch)	26	MO2	O	STM electrical angle monitor output pin 2
5	Vcc	-	Power Supply Voltage pin	27	DATA	I	Serial Data input pin
6	MCK	I	Clock for constant current control input pin	28	CK	I	Serial Clock input pin
7	GND	-	Ground pin	29	LD	I	Serial Data Load Signal input pin
8	STBY	I	Standby (Power Save) Control Signal input pin	30	MO1	O	STM electrical angle monitor output pin 1
9	VM4	-	Motor Power Supply Voltage pin 4 (G,Hch)	31	VM1	-	Motor Power Supply Voltage pin 1
10	PWMG	I	PWM signal input pin(G ch)	32	PWMB /EN1	I	PWM signal input pin(B ch) / STM enable signal input pin 1
11	PWMH	I	PWM signal input pin(H ch)	33	PWMA /CK1	I	PWM signal input pin(A ch) / Clock for μStep input pin 1
12	HO1	O	H ch output pin 1	34	AO2	O	A ch output pin 2
13	HO2	O	H ch output pin 2	35	RFA	-	Current detect resistor connection pin (A ch)
14	PGND2	-	Motor Ground pin 2 (G,Hch)	36	AO1	O	A ch output pin 1
15	GO1	O	G ch output pin 1	37	BO2	O	B ch output pin 2
16	GO2	O	G ch output pin 2	38	RFB	-	Current detect resistor connection pin (B ch)
17	DO1	O	D ch output pin 1	39	BO1	O	B ch output pin 1
18	RFD	-	Current detect resistor connection pin (D ch)	40	EO2	O	E ch output pin 1
19	DO2	O	D ch output pin 2	41	RFE	-	Current detect resistor connection pin (E ch)
20	CO1	O	C ch output pin 1	42	EO1	O	E ch output pin 1
21	RFC	-	Current detect resistor connection pin (C ch)	43	FO2	O	F ch output pin 2
22	CO2	O	C ch output pin 2	44	PGND1	-	Motor Ground pin 1 (Fch)

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Absolute Maximum Ratings (Ta = 25deg Celsius)

Characteristics	Symbol	Rating	Unit	Remarks
Supply Voltage	V_{CC}	6	V	V_{CC}
Motor Supply Voltage	V_M	6	V	V_M
Output Pin Voltage	V_{OUT}	-0.2 to 6	V	Ch.A to G
Output Current	I_{OUT}	0.8	A	
Input Voltage	V_{IN}	−0.2 to 6	V	Each control input pin
Power Dissipation	P_D	TBD	W	IC only
		TBD		Note.
Operationg Temprature	T_{opr}	−20 to 85	°C	
Strage Templature	T_{stg}	−55 to 150	°C	

Note: When one side is mounted on 50mm×50mm×1.6mm, Cu 40% glass epoxy board.

Recommended Operating Conditions 1 (Ta= -20deg to 85deg Celsius)

Characteristics	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Small Signal Supply Voltage	V_{CC}	3	3.3	5.5	V	
Motor Supply Voltage	V_M	2.5	—	5.5	V	
Output Current	I_{OUT}	—	—	600	mA	VM≧3V
		—	—	250		2.5V≦VM＜3V
PWM Frequency	f_{PWM}	—	—	100	kHz	
Mastor Clock Frequency	fMCK	—	ı	5	MHz	

Recommended Operating Conditions 2: Serial Data Controller (Ta= -20deg to 85deg Celsius)

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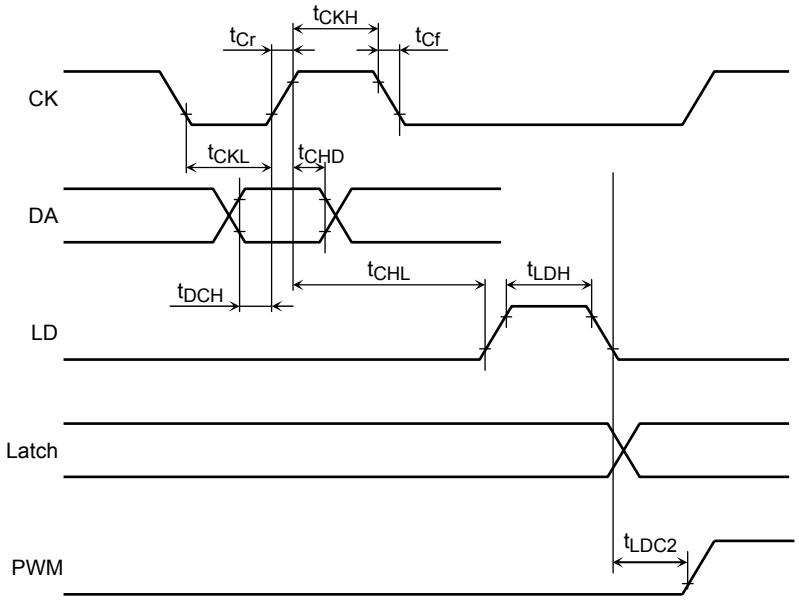
Characteristics	Symbol	Rating		Unit
		Min	Max	
Low-level Clock Pulse Width	t_{CKL}	200	—	ns
High-level Clock Pulse Width	t_{CKH}	200	—	
Clock Rise Time	t_{Cr}	—	50	
Clock Fall Time	t_{Cf}	—	50	
Data Setup Time	t_{DCH}	30	—	
Data Hold Time	t_{CHD}	60	—	
Load Setup Time	t_{CHL}	200	—	
Load Hold Time	t_{LDC}	200	—	
PWM Synchronization Time	tLDC2	100	—	
High-level Load Pulse Width	t_{LDH}	2	—	μs
CK (clock pulse) Frequency	f_{CLK}	—	2.5	MHz



Specifications and Operation of Each Circuit Block:

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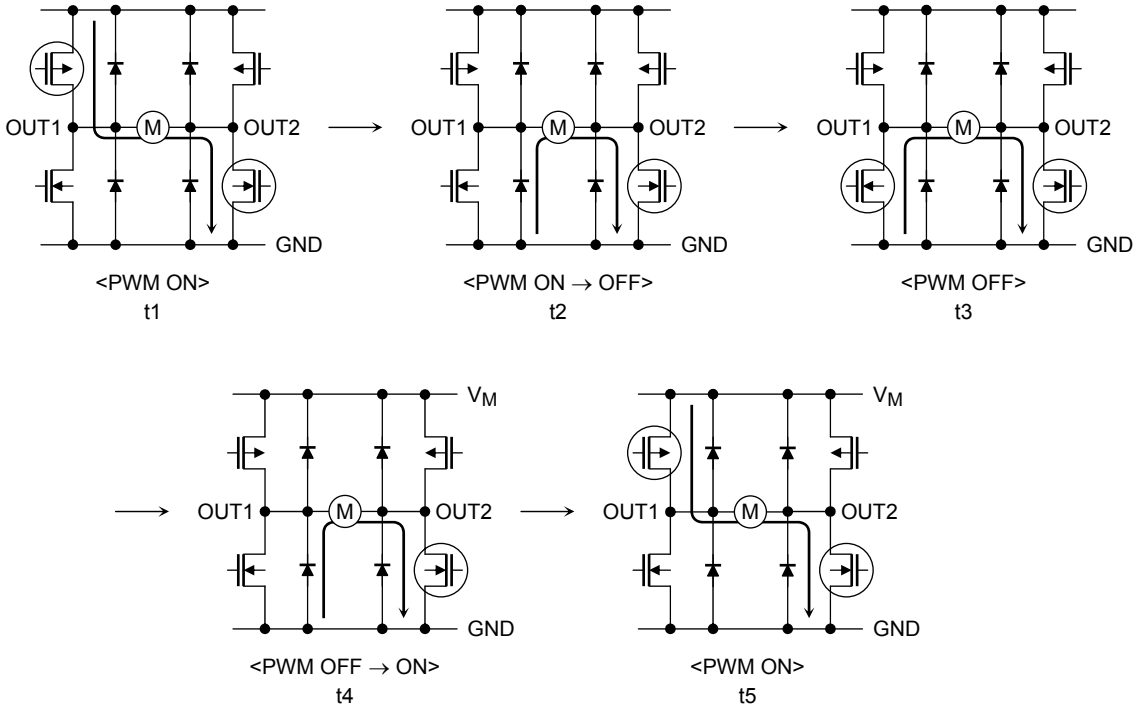
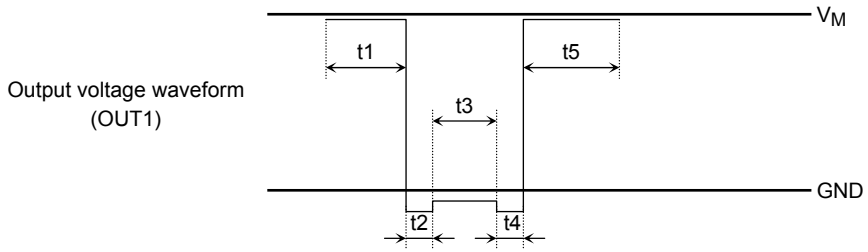
- Bridge output block: ch.A to ch.H

PWM control feature

While PWM control is applied, normal operation t1, t5, and short brake t3 are repeated.
(Dead time t2 and t4 are inserted to prevent pass-through current.)





Constant Current Bridge Block: Off Time Fixed Type PWM Constant Current Chopping

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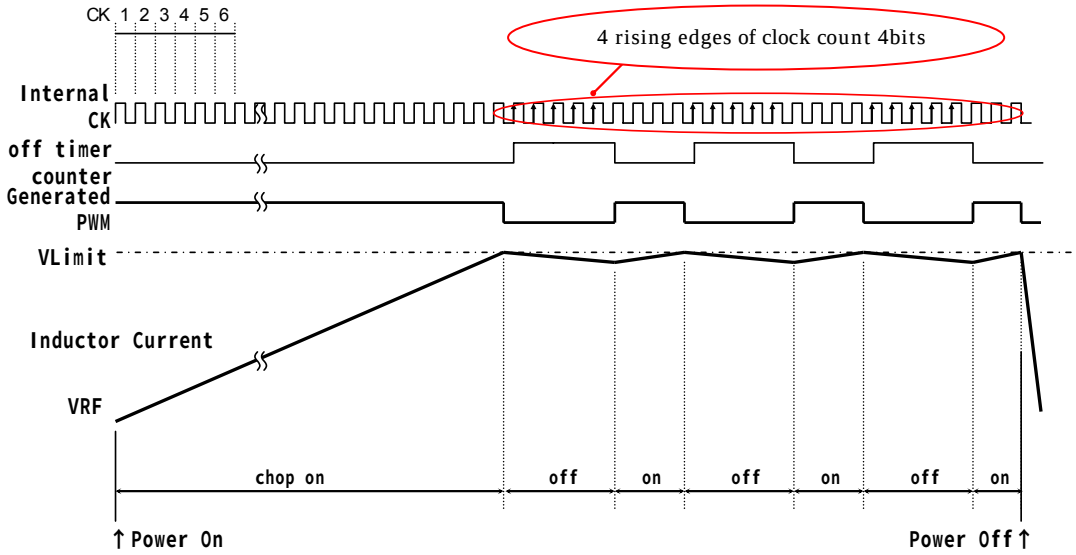
The TB6613FTG has PWM circuit of chop off time fixed type.
Chop off time is determined with internal counting of external input clock signal.
To change the chop off time is change the clock signal or change the internal count setting, 2,4,6,8 counts.

Example：Clock 4bit count setting

First, chopping on starts and current occurs to the load inductor.
Next, when voltage level of external current detect resister reaches to comparator reference voltage Vlimit, the comparator operates and move to chop off.
The chop off period is determined with internal clock counting.
The counting is started at up-edge timing of internal clock just after output hi-side transistor turns off, and ends after four bit count (reset at fifth up-edge timing).
This chop-off time control function produce PWM signal to tern on or off the output transistor.

Conceptual diagram for PWM chopping operation (example of 4 clock count)



(The inductor current (Io peak) is limited at the value obtained from the equation I_O = Vlimt/RNF)

μ-Step Control mode: Ch A, B, C, D

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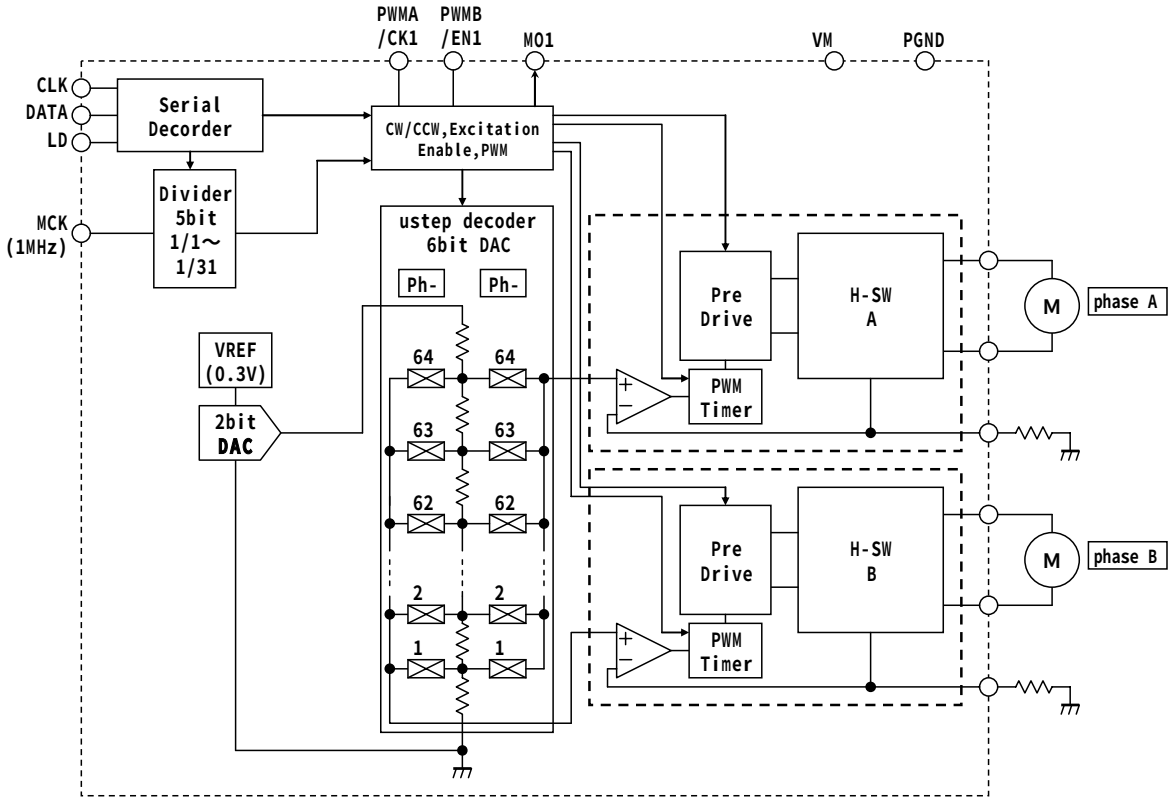
・Constant current control is using chop-off time fixed method counting internal clock(MCLK frequency division) with PWM timer.



・Pulse clock in control : Step-up is done on up-edge timing of CK input signal into PWMA/CK1(Ch A,B) or PWMC/CK2(Ch C,D)
Actual timing is synchronized to internal clock made with MCK.

・Excitation mode : 2 mode selectable
1bit mode: resolution=8/360deg or 6bit: mode: resolution =256/360deg mode

・Enable control : Excitation ON/OFF is controlled with input signal into PWMB/EN1(Ch A,B) or PWMD/EN2(Ch C,D)
Enable ON : ENn = 1 ／ Enable OFF : ENn = 0

・Current decay mode : 4 mode of decay on Vref changing timing around step down period is selectable

・Electrical angle monitor : Negative pulse on each electrical angle timing (93deg or 360deg) is outputted to MO1 or MO2.

・PWM chopping Frequency : PWM Frequency is generated through divider from external MCK signal.
5bit:Max=1/31

・Chop off count : 4 mode selectable (2,4,6,8 counts of internal clock from MCK signal with divider.)

・Constant current setting : 100% level is from internal Vref=0.3V and set 4 level with 2bit DAC.
(0.3V, 0.225V, 0.15V, 0.075V)
Constant current reference level is determined by μstep decoder (6bit) from this 100% level.

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Current decay mode : Only for step down slope during μstep control.

During step down slope during μstep control, in some case big distortion could be occurring.

It depends on time constant of motor coil.

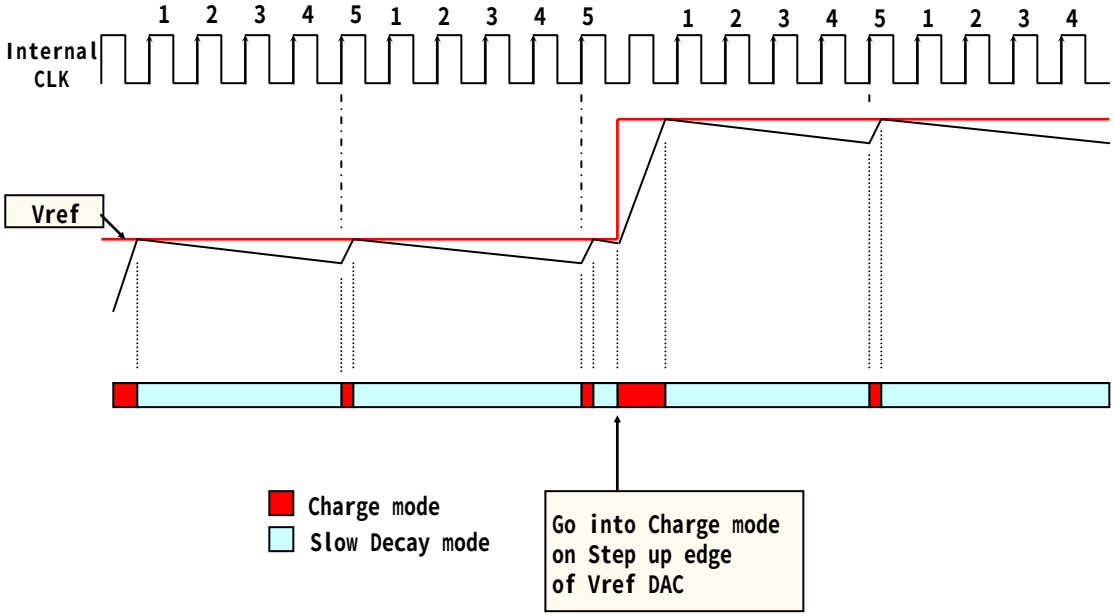
The TB6613FTG has Fast mode to reduce the distortion with enough trackability during step down slope.

Selectable 4 Fast mode

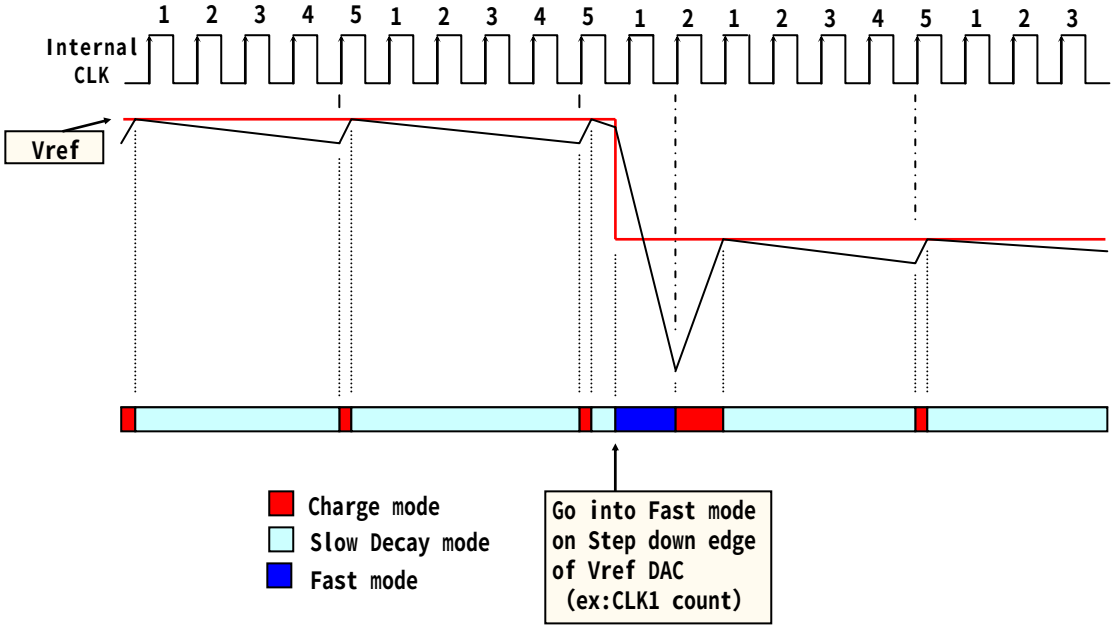
Fast mode time is generated from internal clock count.

Fast mode	Internal CLK count	Effect of decay
Fast0	0	No
Fast1	1	Small
Fast2	2	Middle
Fast3	3	Big

Step Up Slope



Step Down Slope (Ex. Fast1 mode)



Conceptual diagram of 1bit mode (1bit: 8step/360deg)

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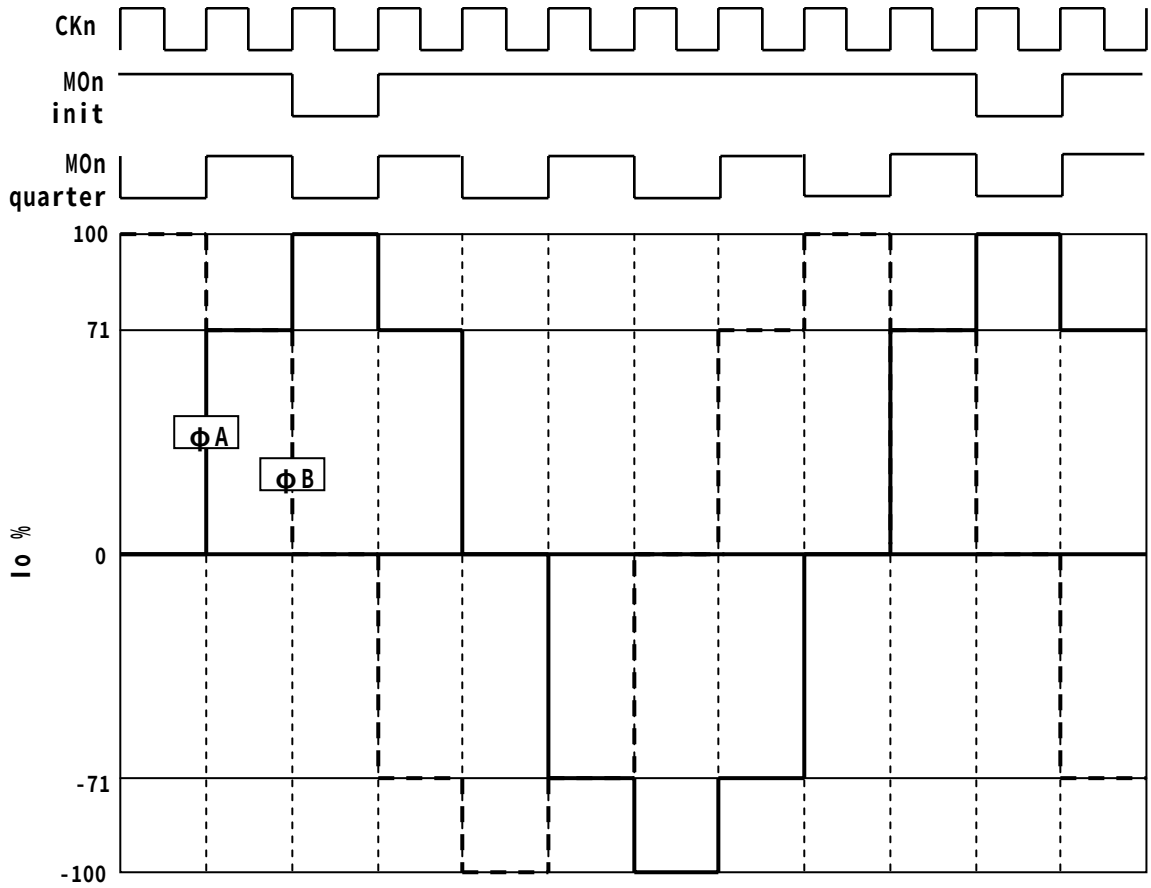
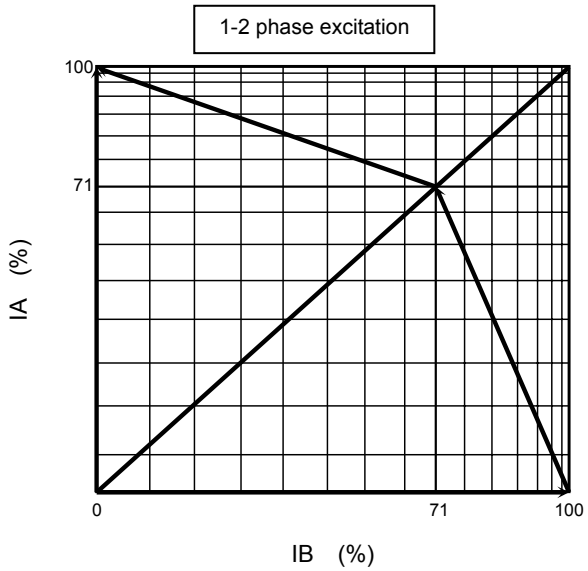


Output Current Vector



Conceptual diagram of 6bit mode (6bit: 256step/360deg)

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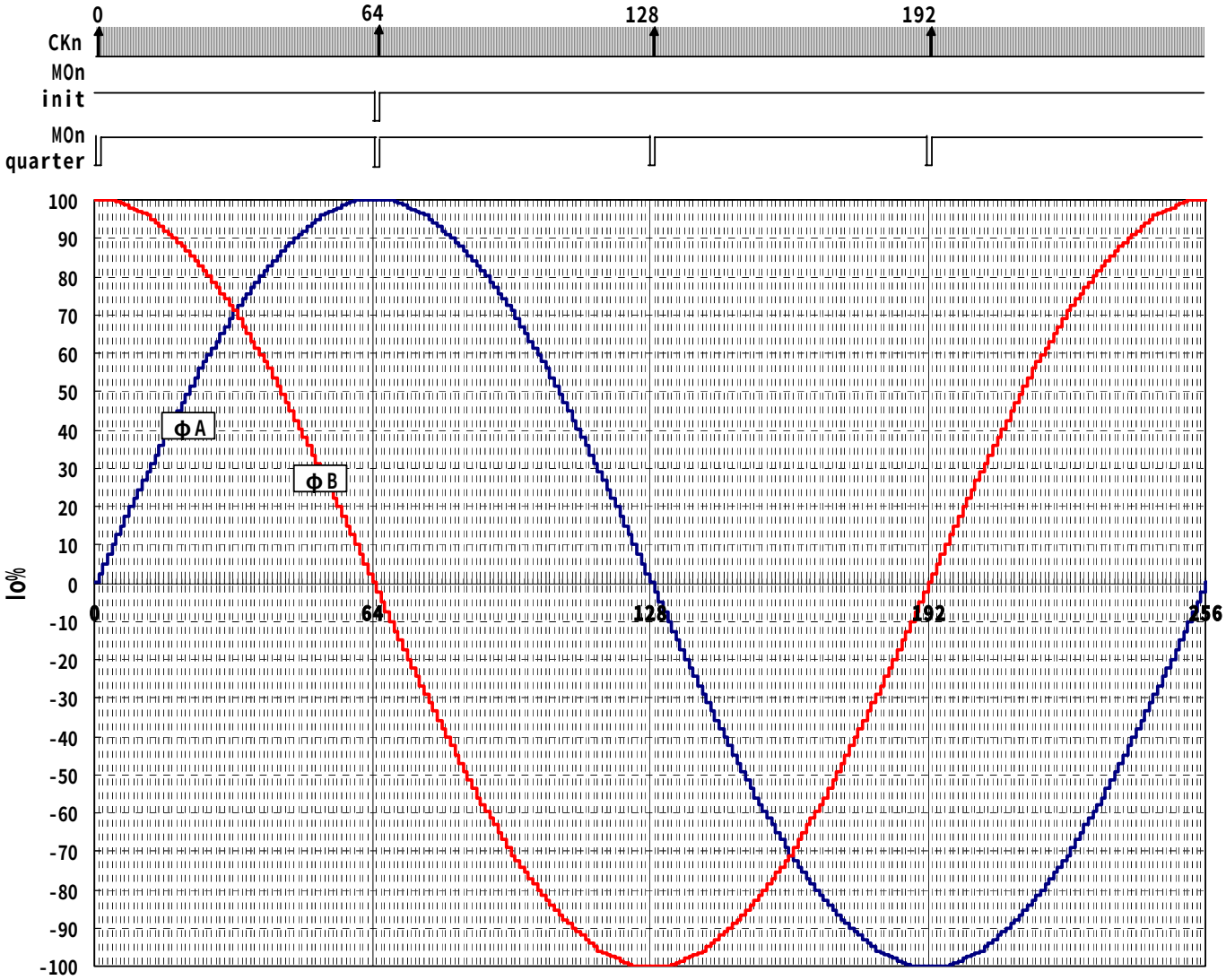

Enable and Count Reset signal

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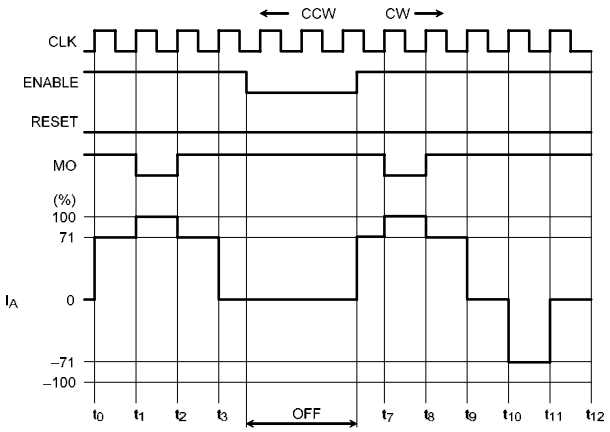
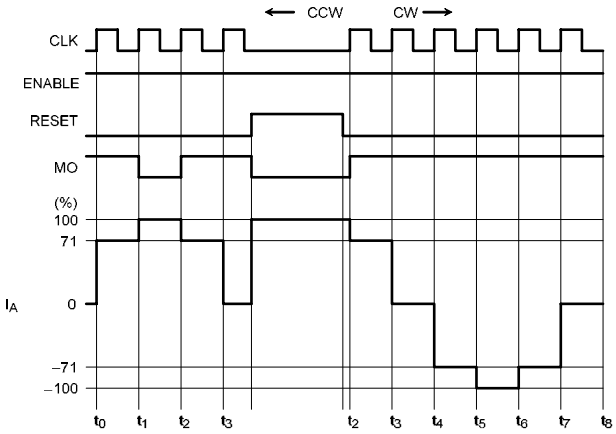
Enable(ENn pin) Function of ON/OFF



Output turns off when ENn changes to L.
But internal circuit except output stage keeps going with Input CKn Signal.
Output level becomes the one on the time after CKn going when ENn changes to H.

If ENn=L, output is absolutely off not on Reset signal.

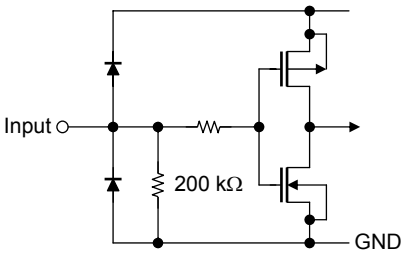
RESET(Serial command) Function of ON/OFF



Output turns to initial state when Reset changes to H and Mon outputs L level.
After that when Reset goes back to L,
Output starts on timing of next CKn up edge from the next step of initial state.

Input terminal

Each input pin (CK, DATA, LD, PWMA/CK1,PWMB/EN1,PWMC/CK2,PWMD/EN2,PWME/CK3,PWMF/EN3, PWMF/EN3, STBY,MCK) includes pulldown resister (about 200 kΩ).



Serial Data Specifications

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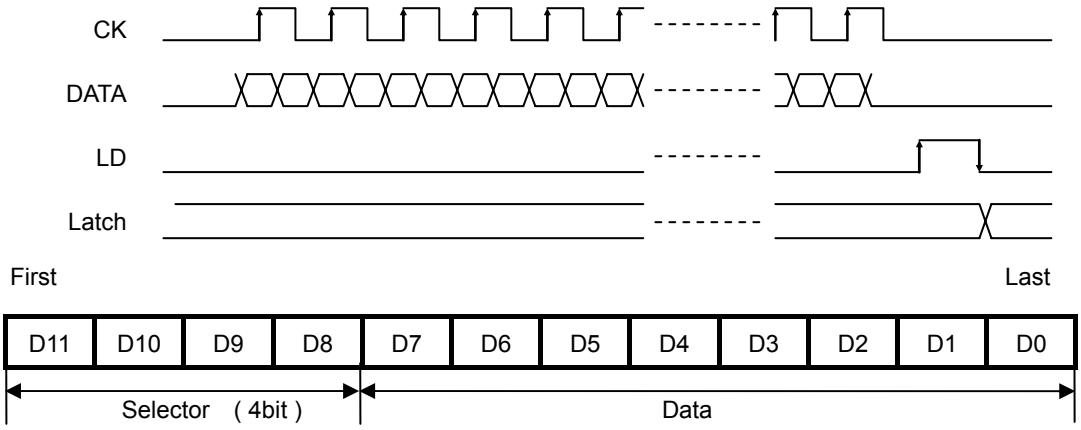
12 bit serial data format



Each register mode

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	ｱﾄﾞﾚｽ
0	0	0	0	mod1	stm1	if1	ick1:5bit					0
0	0	0	1	2bit DAC1		mdr1	rst1	mo1	off1		---	1
0	0	1	0	p1a	p1b	sdfst1		scw1	---	---	---	2
0	0	1	1	mod2	p2a	p2b	if2	off2		---	---	3
0	1	0	0	mod3	stm3	if3	ick3:5bit					4
0	1	0	1	2bit DAC2		mdr3	rst3	mo3	off3		---	5
0	1	1	0	p3a	p3b	Sdfst3		scw3	---	---	---	6
0	1	1	1	mod4	p4a	p4b	if4	off4		---	---	7
1	0	0	0	mod5	if5	6bit DAC						8
1	0	0	1	off5		---	ick5:5bit					9
1	0	1	0	p5a	p5b	---	---	---	---	---	---	10
1	0	1	1	mod6	p6a	p6b	---	---	---	---	---	11
1	1	0	0	mod7	p7a	p7b	---	---	---	---	---	12
1	1	0	1	mod8	p8a	p8b	---	---	---	---	---	13
1	1	1	0	Don't care								14
1	1	1	1									15

modx	:	H-SW control	0=Direct PWM(table1) mode / 1=table2 control mode
stmx	:	STM mode	0=H-SW independent mode / 1=micro-step mode
ifx	:	Constant current select	0=Not with CC control / 1=with CC control * Available only in H-SW independent mode (stmx=0), absolutely with CC control in micro-step mode.
2bit DACx	:	2bit DACsetting	0.075V,0.15V,0.225V,0.3V 0.075V step 4levels
ickx	:	Internal CLK division ratio	Ext MCK division ratio 5bit(×1/1(set to 1)～1/31(set to 31))
mdrx	:	STM excitation mode	0=6bit micro-step mode / 1=1-2phase excitation mode
sdfstx	:	step down Fast mode	0=Without / 1=1CLK / 2=2CLK / 3=3CLK
scwx	:	STM CCW/CW	0=CCW / 1=CW
rstx	:	STM step count initialize	0= count mode / 1=reset(initialize)
mox	:	Monitor signal select	0=360deg timing / 1=90deg timing
offx	:	PWM off count number	0=2CLK / 1=4CLK / 2=6CLK / 3=8CLK
pxa	:	H-SW control a	See table1 or table2
pxb	:	H-SW control b	See table1 or table2
6bit DAC	:	Ch.E 6bit DAC	

Note. Address=3,7 is available only in H-SW independent mode (stmx=0), (not available when stmx=1)

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＜Register supplement explanation＞

1. The address is separately prepared for every channel or μ step pair.

Address	Object for setting
0,1,2,3	Ch-A, Ch-B (stm1=1：μstep pair(A&B))
4,5,6,7	Ch-C, Ch-D (stm3=1：μstep pair(C&D))
8,9,10	Ch-E
11	Ch-F
12	Ch-G
13	Ch-H

※Address 3(Ch-B setting) and 7(Ch-D setting) are available only in the H-SW independent mode (stmx=0). (It is invalid in the μstep mode. It is common setting for every pair.)

2. The x (number) part of each setting name corresponds to each channel.

x	Object for setting
x=1	Ch-A (stmx, ickx, 2bit DACx, mdrx, rstx, mox, sdfstx, scwx : Common setting for Ch-A and B.)
x=2	Ch-B
x=3	Ch-C (stmx, ickx, 2bit DACx, mdrx, rstx, mox, sdfstx, scwx : Common setting for Ch-C and D.)
x=4	Ch-D
x=5	Ch-E
x=6	Ch-F
x=7	Ch-G
x=8	Ch-H

3. Setting the ickx internal clock dividing ratio

Internal clock dividing ratio for each channel(μstep pair) can be set by D4, D3, D2, D1, and D0 of the address 0 (Ch-A,B), address 4(Ch-C,D), and address 8(Ch-E).

Dec	Bin	Add 0 or 4 or 8 setting					Int-clock
		D4	D3	D2	D1	D0	div. ratio
1	00001	0	0	0	0	1	1/1
2	00010	0	0	0	1	0	1/2
3	00011	0	0	0	1	1	1/3
4	00100	0	0	1	0	0	1/4
5	00101	0	0	1	0	1	1/5
6	00110	0	0	1	1	0	1/6
7	00111	0	0	1	1	1	1/7
8	01000	0	1	0	0	0	1/8
9	01001	0	1	0	0	1	1/9
10	01010	0	1	0	1	0	1/10
11	01011	0	1	0	1	1	1/11
12	01100	0	1	1	0	0	1/12
13	01101	0	1	1	0	1	1/13
14	01110	0	1	1	1	0	1/14
15	01111	0	1	1	1	1	1/15
16	10000	1	0	0	0	0	1/16
17	10001	1	0	0	0	1	1/17
18	10010	1	0	0	1	0	1/18
19	10011	1	0	0	1	1	1/19
20	10100	1	0	1	0	0	1/20
21	10101	1	0	1	0	1	1/21
22	10110	1	0	1	1	0	1/22
23	10111	1	0	1	1	1	1/23
24	11000	1	1	0	0	0	1/24
25	11001	1	1	0	0	1	1/25
26	11010	1	1	0	1	0	1/26
27	11011	1	1	0	1	1	1/27
28	11100	1	1	1	0	0	1/28
29	11101	1	1	1	0	1	1/29
30	11110	1	1	1	1	0	1/30
31	11111	1	1	1	1	1	1/31

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4. Setting 6bit DAC Ch-E 6bit DAC

Voltage level which determines the target current for controlling Ch-E constant current can be set by D5, D4, D3, D2, D1, and D0 of the address 8.

The target current is determined by this voltage level and the external detect resistance.

※ Setting voltage in the table below is typical value.

Dec	Bin	Add 8 setting						Set Voltage
		D5	D4	D3	D2	D1	D0	[mV]
0	000000	0	0	0	0	0	0	0.0
1	000001	0	0	0	0	0	1	4.8
2	000010	0	0	0	0	1	0	9.5
3	000011	0	0	0	0	1	1	14.3
4	000100	0	0	0	1	0	0	19.0
5	000101	0	0	0	1	0	1	23.8
6	000110	0	0	0	1	1	0	28.6
7	000111	0	0	0	1	1	1	33.3
8	001000	0	0	1	0	0	0	38.1
9	001001	0	0	1	0	0	1	42.9
10	001010	0	0	1	0	1	0	47.6
11	001011	0	0	1	0	1	1	52.4
12	001100	0	0	1	1	0	0	57.1
13	001101	0	0	1	1	0	1	61.9
14	001110	0	0	1	1	1	0	66.7
15	001111	0	0	1	1	1	1	71.4
16	010000	0	1	0	0	0	0	76.2
17	010001	0	1	0	0	0	1	81.0
18	010010	0	1	0	0	1	0	85.7
19	010011	0	1	0	0	1	1	90.5
20	010100	0	1	0	1	0	0	95.2
21	010101	0	1	0	1	0	1	100.0
22	010110	0	1	0	1	1	0	104.8
23	010111	0	1	0	1	1	1	109.5
24	011000	0	1	1	0	0	0	114.3
25	011001	0	1	1	0	0	1	119.0
26	011010	0	1	1	0	1	0	123.8
27	011011	0	1	1	0	1	1	128.6
28	011100	0	1	1	1	0	0	133.3
29	011101	0	1	1	1	0	1	138.1
30	011110	0	1	1	1	1	0	142.9
31	011111	0	1	1	1	1	1	147.6
32	100000	1	0	0	0	0	0	152.4
33	100001	1	0	0	0	0	1	157.1
34	100010	1	0	0	0	1	0	161.9
35	100011	1	0	0	0	1	1	166.7
36	100100	1	0	0	1	0	0	171.4
37	100101	1	0	0	1	0	1	176.2
38	100110	1	0	0	1	1	0	181.0
39	100111	1	0	0	1	1	1	185.7
40	101000	1	0	1	0	0	0	190.5
41	101001	1	0	1	0	0	1	195.2
42	101010	1	0	1	0	1	0	200.0
43	101011	1	0	1	0	1	1	204.8
44	101100	1	0	1	1	0	0	209.5
45	101101	1	0	1	1	0	1	214.3
46	101110	1	0	1	1	1	0	219.0
47	101111	1	0	1	1	1	1	223.8
48	110000	1	1	0	0	0	0	228.6
49	110001	1	1	0	0	0	1	233.3
50	110010	1	1	0	0	1	0	238.1
51	110011	1	1	0	0	1	1	242.9
52	110100	1	1	0	1	0	0	247.6
53	110101	1	1	0	1	0	1	252.4
54	110110	1	1	0	1	1	0	257.1
55	110111	1	1	0	1	1	1	261.9
56	111000	1	1	1	0	0	0	266.7
57	111001	1	1	1	0	0	1	271.4
58	111010	1	1	1	0	1	0	276.2
59	111011	1	1	1	0	1	1	281.0
60	111100	1	1	1	1	0	0	285.7
61	111101	1	1	1	1	0	1	290.5
62	111110	1	1	1	1	1	0	295.2
63	111111	1	1	1	1	1	1	300.0

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Function table

Function in H-SW independent mode (stmx=0) is selectable by modx.

(As for Ch-E, F, G, and H, they are always in the independent mode without stmx setting.)

table1

modx=0 stmx=0

pxa	pxb	PWMx	OUTxA	OUTxB	Driving mode
0	0	X	Z	Z	STOP
0	1	L	L	L	Short brake
0	1	H	L	H	CCW
1	0	L	L	L	Short brake
1	0	H	H	L	CW
1	1	X	L	L	Short brake

table2

modx=1 stmx=0

pxa	pxb	PWMx	OUTxA	OUTxB	Driving mode
0	X	X	Z	Z	STOP
1	0	L	H	L	CW
1	0	H	L	H	CCW
1	1	X	L	L	Short brake

Function of STBY,UVLO,TSD and rstx(internal register)

Function	STBY *1)	UVLO	TSD	rstx
Register clear	Clear	Clear	Holding	Holding
Driver off	Off	Off	Off	On (control with EN pin)

*1)STBY : L=Standby(Power save) mode, H=Normal operation mode

*2) Resistance clear: All addresses are zero.

Electric Characteristics(V_{CC} = 3.3 V, V_M = 5 V, Ta = 25°C unless otherwise specified)

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Characteristics		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current		I_{CC}	All 8ch in CW mode	—	2	(4)	mA
		$I_{CC\ (STB)}$	Standby mode(STBY=0V)	—	0.1	10	μA
		$I_{M\ (STB)}$		—	0	1	
Serial/ Standby/ PWM,CLK input	Input voltage	V_{INH}		Vcc×0.7	—	Vcc+0.2	V
		V_{INL}		−0.2	—	Vcc×0.3	
	Input current	I_{INH}	V_{IH} = 3 V	5	15	25	μA
		I_{INL}	V_{IL} = 0 V	—	—	1	
Output saturation voltage(Ch.A to H)		$V_{sat\ (U+L)}$	I_O = 0.2 A,Vcc=5V	—	(0.3)	(0.4)	V
			I_O = 0.6 A,Vcc=5V	—	(0.9)	(1.2)	
Output leakage current(Ch.A to H)		$I_{L\ (U)}$	V_M = 6V	—	—	1	μA
		$I_{L\ (L)}$		—	—	1	
Output diode forword voltage		$V_{F\ (U)}$	I_F = 0.6 A(Design value)	—	1	—	V
		$V_{F\ (L)}$		—	1	—	
6bit DAC	Nonlinerity error	LB	Ch.E	−3	—	3	LSB
	Differential linearity error	DLB		−2	—	2	
μstep reference level	6bit mode	θ	See next page.	—	—	—	%
	1bit mode	Half step	(Design value)	—	71	—	
Vcc low voltage control	low voltage detect level	UVLD	(Design value)	—	2.0	—	V
	Recovery level	UVLC		—	2.2	—	
Thermal shut down temprature		TSD	(Design value)	—	170	—	°C
Thermal shut down histeresis		ΔTSD		—	20	—	

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Table） μstep level on 6bit mode(Design Value)

θ	Min.	Typ.	Max.	Unit	θ	Min.	Typ.	Max.	Unit
θ63	—	100	—		θ31	—	71	—	
θ62	—	100	—		θ30	—	69	—	
θ61	—	100	—		θ29	—	67	—	
θ60	—	100	—		θ28	—	65	—	
θ59	—	100	—		θ27	—	63	—	
θ58	—	99.5	—		θ26	—	61.25	—	
θ57	—	99	—		θ25	—	59.5	—	
θ56	—	98.5	—		θ24	—	57.75	—	
θ55	—	98	—		θ23	—	56	—	
θ54	—	97.5	—		θ22	—	53.75	—	
θ53	—	97	—		θ21	—	51.5	—	
θ52	—	96.5	—		θ20	—	49.25	—	
θ51	—	96	—		θ19	—	47	—	
θ50	—	95	—		θ18	—	44.75	—	
θ49	—	94	—		θ17	—	42.5	—	
θ48	—	93	—		θ16	—	40.25	—	
θ47	—	92	—	%	θ15	—	38	—	%
θ46	—	91	—		θ14	—	35.75	—	
θ45	—	90	—		θ13	—	33.5	—	
θ44	—	89	—		θ12	—	31.25	—	
θ43	—	88	—		θ11	—	29	—	
θ42	—	86.75	—		θ10	—	26.75	—	
θ41	—	85.5	—		θ9	—	24.5	—	
θ40	—	84.25	—		θ8	—	22.25	—	
θ39	—	83	—		θ7	—	20	—	
θ38	—	81.5	—		θ6	—	17.5	—	
θ37	—	80	—		θ5	—	15	—	
θ36	—	78.5	—		θ4	—	12.5	—	
θ35	—	77	—		θ3	—	10	—	
θ34	—	75.5	—		θ2	—	7.5	—	
θ33	—	74	—		θ1	—	5	—	
θ32	—	72.5	—		θ0	—	2.5	—	

Application Circuit Example

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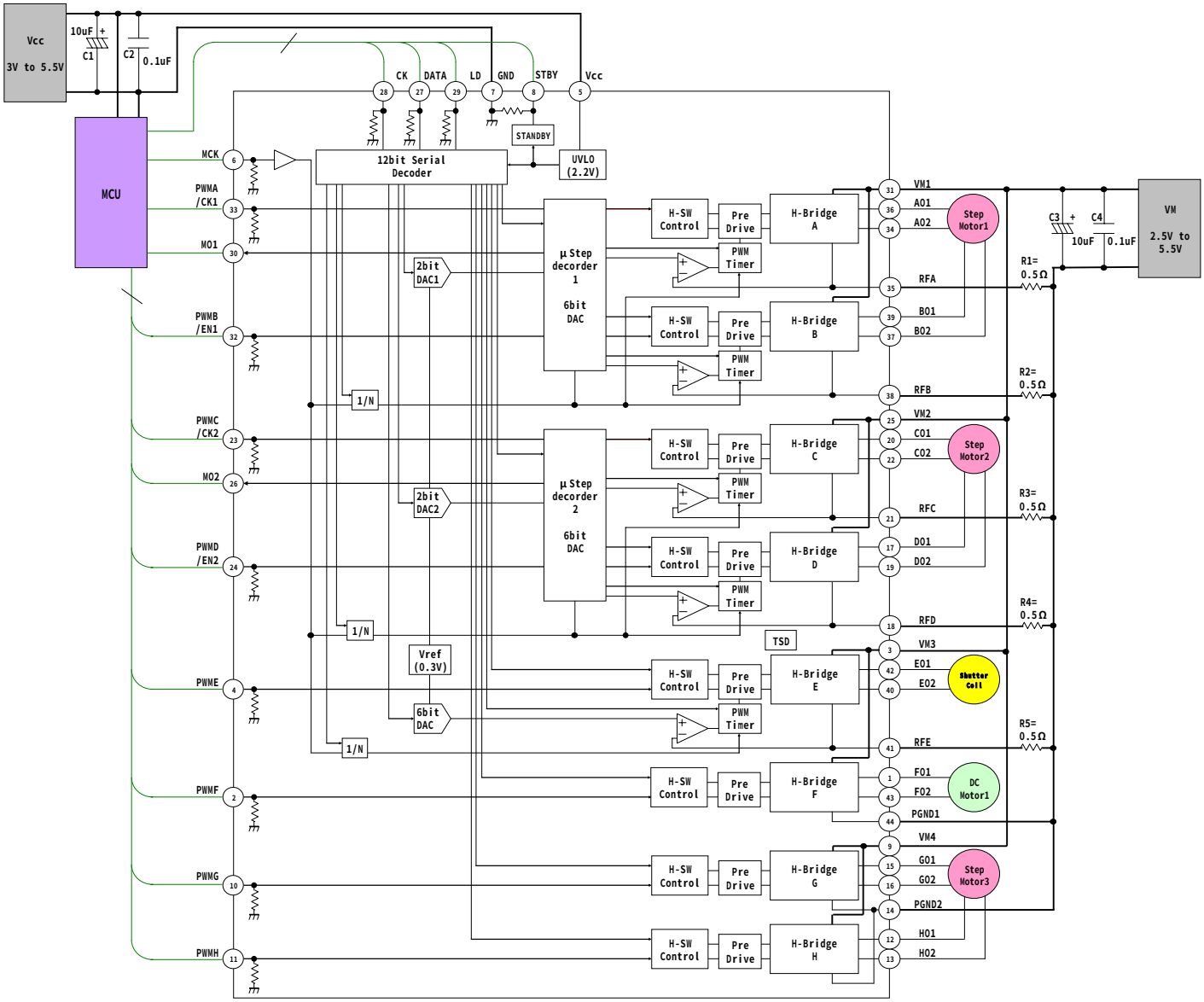
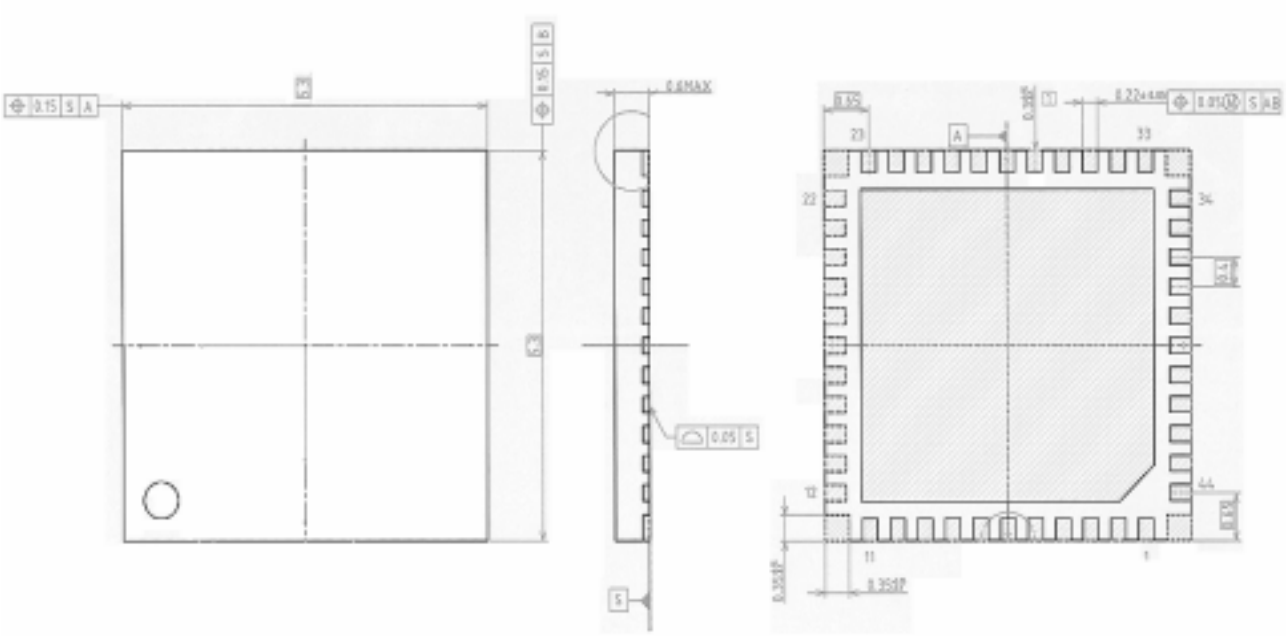


Package outline drawing

TENTATIVE

VQON44-P-0606-0.40

Unit:mm



Weight: 0.05 g (Typ.)

TB6613FTG is a Pb-free product.
The following conditions apply to solderability:
*Solderability
1. Use of Sn-37Pb solder bath
   *solder bath temperature = 230°C
   *dipping time = 5 seconds
   *number of times = once
   *use of R-type flux
2. Use of Sn-3.0Ag-0.5Cu solder bath
   *solder bath temperature = 245°C
   *dipping time = 5 seconds
   *number of times = once
   *use of R-type flux

Notes on Contents

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1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

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(1) Over current Protection Circuit and thermal Shutdown Circuit

Over current protection circuits (referred to as current limiter circuits) and thermal shutdown circuits do not necessarily protect ICs under all circumstances. After they have operated, clear the over current status and the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit and thermal shutdown circuit to not operate properly or IC breakdown before operation.

(2) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(3) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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