SY89852U

Precision Low Power Differential 2:1 LVPECL MUX with Internal Termination

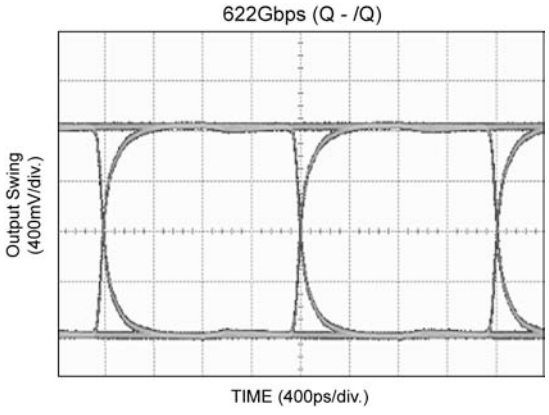
General Description

The SY89852U is a 2.5V/3.3V precision, high-speed, 2:1 differential MUX capable of handling clocks up to 2.5GHz and data streams up to 2.5Gbps.

The differential input includes Micrel's unique, patent pending 3-pin input termination architecture that allows users to interface to any differential signal (AC- or DC-coupled) as small as 100mV ($200mV_{pp}$) without any level shifting or termination resistor networks in the signal path. The unique, patent input isolation design minimizes crosstalk minimizing crosstalk induced jitter. The outputs are 800mV LVPECL, with extremely fast rise/fall time guaranteed to be less than 180ps.

The SY89852U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY89852U is part of Micrel's high-speed, Precision Edge® product line. All support documentation can be found on Micrel's web site at: www.micrel.com.

Typical Applications



Precision Edge®

Features

- Provides a low jitter copy of the selected input
- Superior alternative to the EP58 2:1 MUX
- Low power: 58mW (2.5V nominal, no load)
- Guaranteed AC performance over temperature and supply voltage:
  - DC- to > 2.5Gbps data rate throughput
  - DC- to > 2.5GHz clock f_{MAX}
  - < 340ps In-to-Out t_{pd}
  - < 180ps t_r/t_f time
- Ultra-low Jitter Design:
  - $<1ps_{(rms)}$ random jitter
  - $<10ps_{(pp)}$ deterministic jitter
  - $<10ps_{(pp)}$ total jitter (clock)
  - $<0.7ps_{(rms)}$ crosstalk induced jitter
- Unique, patent-pending input isolation design minimizes crosstalk
- Unique, patent pending input termination and VT pin accepts DC-coupled and AC-coupled inputs (CML, PECL, LVDS)
- Typical 800mV (100k) LVPECL output swing
- Power supply 2.5V ±5% or 3.3V ±10%
- Industrial temperature range –40°C to +85°C
- Available in ultra-small (3mm x 3mm) 16-pin MLF® package

Applications

- Redundant clock distribution
- SONET/SDH clock/data distribution
- Loopback
- Fibre Channel distribution

Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

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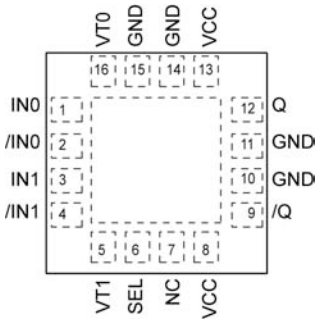
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89852UMG	MLF-16	Industrial	852U with bar-line designator	NiPdAu Pb-Free
SY89852UMGTR[2]	MLF-16	Industrial	852U with bar-line designator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electrical Only.
2. Tape and Reel.

Pin Configuration



16-Pin MLF® (MLF-16)

Pin Description

Pin Number	Pin Name	Pin Function
1,2, 3,4	IN, /IN	Differential Input: This input pair is the signal to be buffered. These inputs accept AC- or DC-coupled signals as small as 100mV (200mV$_{PP}$). Each pin of this pair internally terminates to a VT pin through 50Ω. Note that this input will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details.
16,5	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to this pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
8,13	VCC	Positive Power Supply. Bypass with 0.1µF||0.01µF low ESR capacitors as close to the V_{CC} pin as possible.
12,9	Q, /Q	Differential 100K LVPECL Output: This LVPECL output is the output of the device. Terminate through 50Ω to V_{CC} –2V. PECL output requires DC path to ground. Thus, AC-coupled applications require pull-down resistors. See "Output Interface Applications" section.
10,11,14,15	GND, Exposed Pad	Ground. Ground pin and exposed pad must be connected to the same ground plane.
6	SEL	This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25KΩ pull-up resistor and will default to logic HIGH state if left open.
7	NC	No connect.

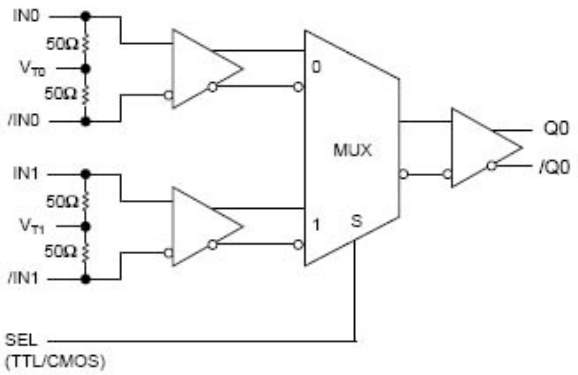
Truth Table

IN0	IN1	SEL[1]	Q
0	X	0	0
1	X	0	1
X	0	1	0
X	1	1	1

Note:

1. SEL is connected to a 25kΩ pull-up resistor and will default to logic high if left open.

Functional Block Diagram



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Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Termination Current[3]
  Source or sink current on V_T ..... ±50mA
Lead Temperature (soldering, 20sec.)..... +260°C
Storage Temperature (T_s) ..... –65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[4]
MLF® (θ_{JA})
  Still-Air ..... 60°C/W
MLF® (ψ_{JB})
  Junction-to-Board ..... 38°C/W

DC Electrical Characteristics[5]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
			3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		23	35	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
R_{IN}	Input Resistance (IN-to-V_T)		40	50	60	Ω
V_{IH}	Input High Voltage (IN-to-/IN)	Note 6	V_{CC} –1.6		V_{CC}	V
V_{IL}	Input Low Voltage (IN-to-/IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN-/IN|	See Figure 1b.	0.2			V
V_{T_IN}	IN-to-V_T (IN-to-/IN)				1.28	V

Notes:

1. Permanent device damage may occur if the “Absolute Maximum Ratings” are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} use a 4-layer board in still air, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IH} (min) not lower than 1.2V.

LVPECL Outputs DC Electrical Characteristics[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to + 85°C; R_L = 50Ω to V_{CC} –2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage Q, /Q		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	550	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q, /Q	See Figure 1b.	1100	1600		mV

LVTTL/CMOS DC Electrical Characteristics[7]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		-125		30	µA
I_{IL}	Input LOW Current		-300			µA

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to + 85°C, R_L = 50Ω to V_{CC} –2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	2.5	3.2		Gbps
		Clock, V_{OUT} ≥ 400mV	2.5	3.5		GHz
t_{PD}	Propagation Delay IN-to-Q, /IN-to-Q SEL-to-Q	V_{IN} ≥ 100mV	 140 100	 230 250	 340 400	 ps ps
t_{PD} Tempco	Differential Propagation Delay Temperature Coefficient			100		fs/°C
t_{Jitter}	Data Random Jitter (RJ)	Note 9			1	ps_{RMS}
	Deterministic Jitter (DJ)	Note 10			10	ps_{RMS}
	Clock Cycle-to-Cycle Jitter	Note 11			1	ps_{PP}
	Total Jitter	Note 12			10	ps_{RMS}
	Crosstalk-induced Jitter	Note 13			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	50	100	180	ps

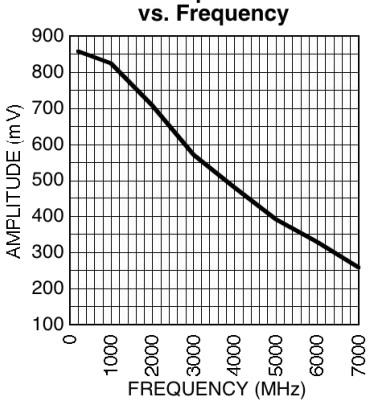
Notes:

8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Random jitter is measured with a K28.7 character pattern, measured at 2.5Gbps.
10. DJ is measured at 2.5Gbps, with both K28.5 and 2^{23} – 1 PRBS pattern.
11. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, T_n – T_{n-1} where T is the time between rising edges of the output signal.
12. Total jitter definition: With an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
13. Crosstalk induced jitter is defined as the added jitter that results from signals applied to two adjacent channels. It is measured at the output while applying two similar, differential clock frequencies that are asynchronous with respect to each other at the inputs.

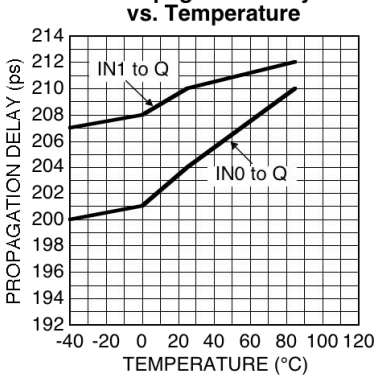
Operating Characteristics

V_{CC} = 2.5V, V_{IN} = 100mV, T_A = 25°C; unless otherwise stated.

Amplitude vs. Frequency

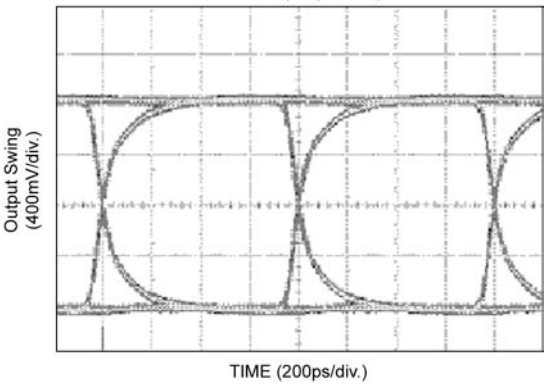


Propagation Delay vs. Temperature

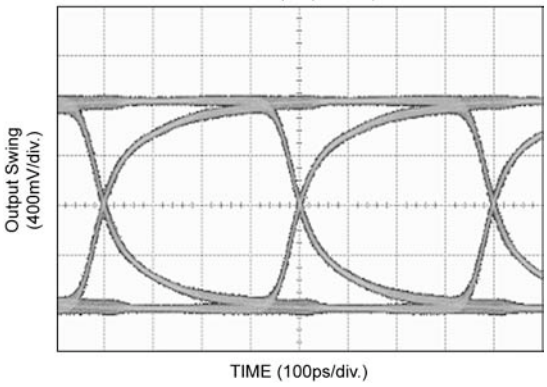


Operating Characteristics

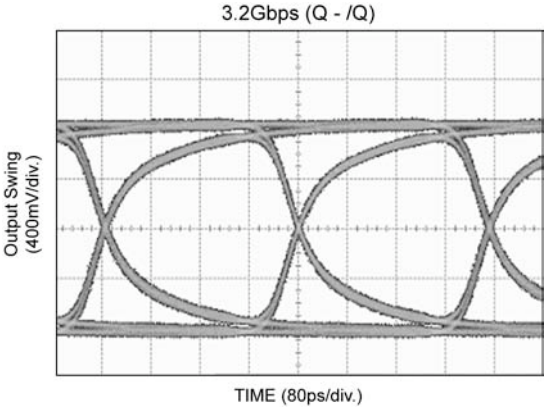
1.25Gbps (Q - /Q)



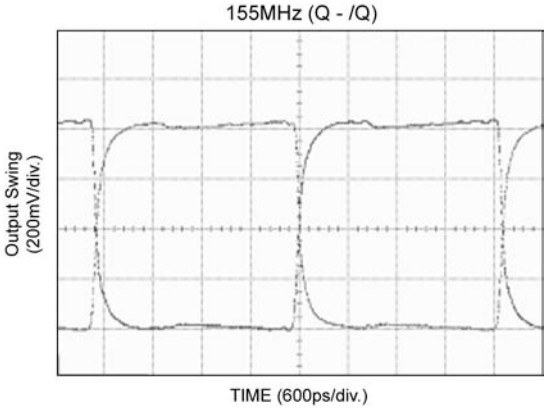
2.5Gbps (Q - /Q)



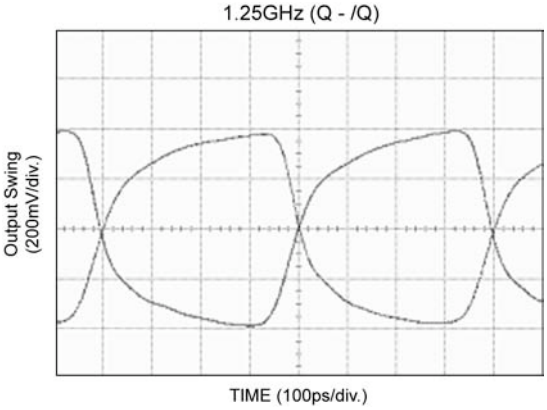
3.2Gbps (Q - /Q)



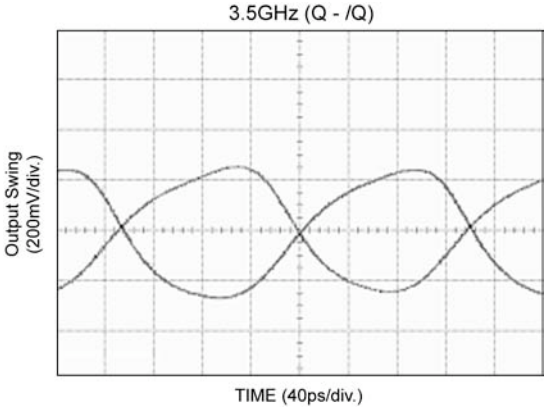
155MHz (Q - /Q)



1.25GHz (Q - /Q)



3.5GHz (Q - /Q)



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Singled-Ended and Differential Swings

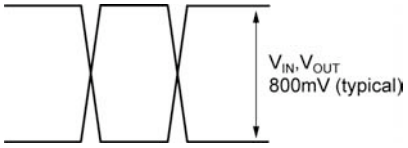

Figure 1a. Single-Ended Voltage Swing

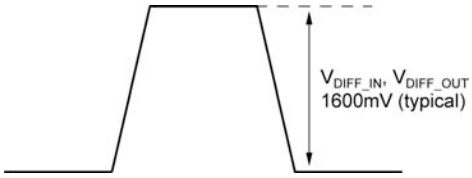

Figure 1b. Differential Voltage Swing

Timing Diagrams

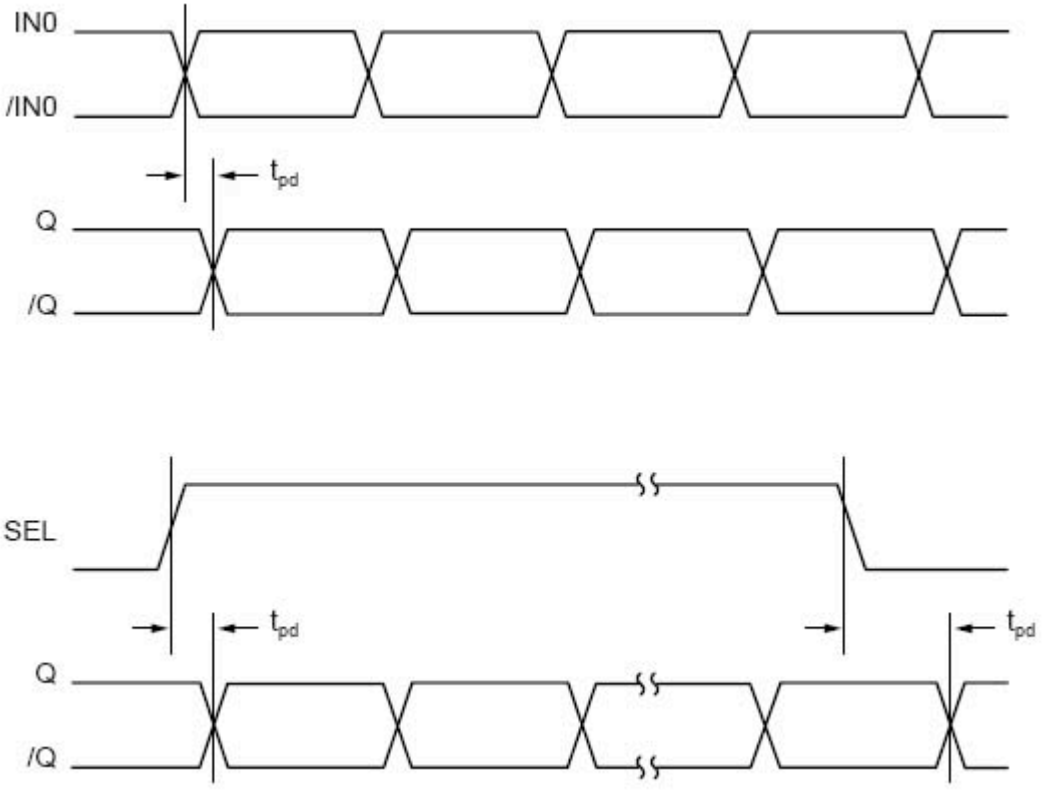

Figure 2. Timing Diagram

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Input and Output Stages

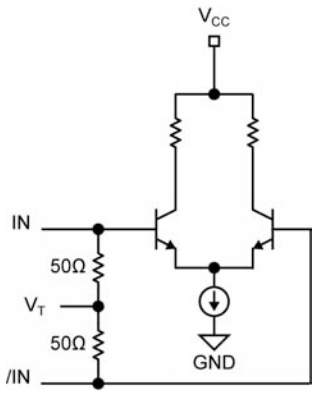


Figure 3a. Simplified Differential Input Stage

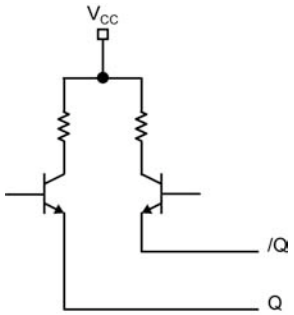


Figure 3b. Simplified LVPECL Output Stage

Input Interface Applications

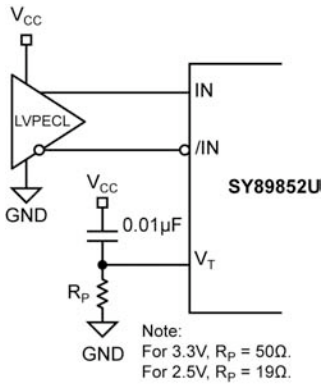


Figure 4a. LVPECL Interface (DC-Coupled)

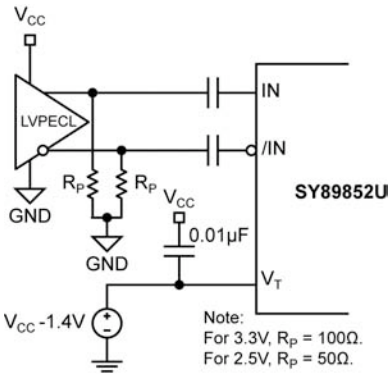
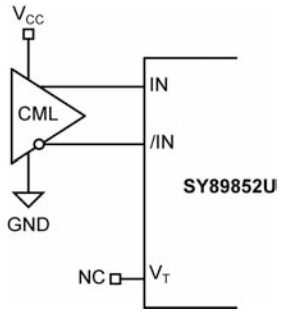


Figure 4b. LVPECL Interface (AC-Coupled)



Option: may connect V_T to V_{CC}

Figure 4c. CML Interface (DC-Coupled)

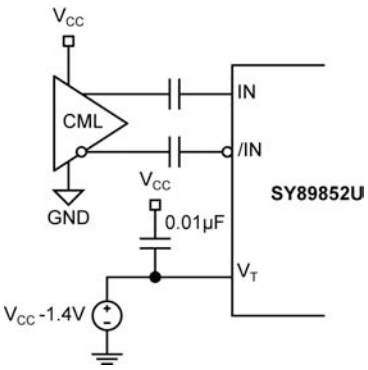


Figure 4d. CML Interface (AC-Coupled)

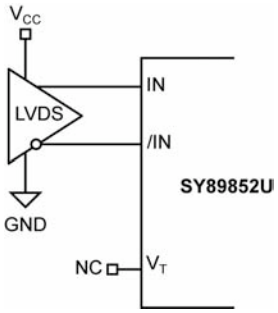


Figure 4e. LVDS Interface

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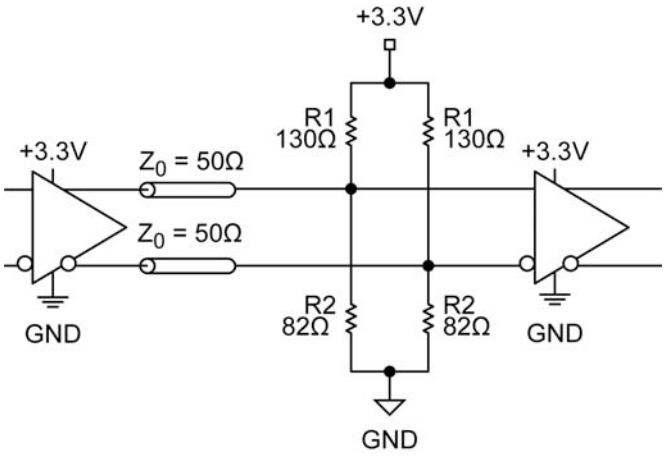
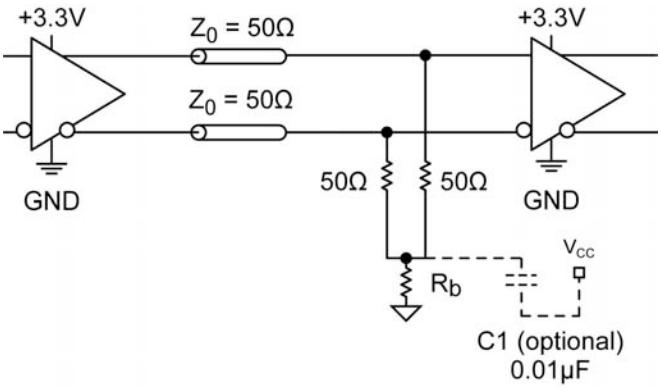
Output Interface Applications



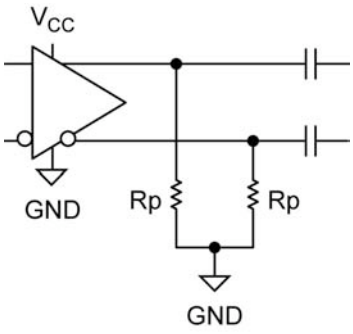
Note:
For +2.5V systems
R1 = 250Ω, R2 = 82.5Ω

Figure 5a. Parallel Thevenin-Equivalent Termination



Note:
For +2.5V systems: Rb = 19Ω
For 3.3V systems Rb = 50Ω

Figure 5b. Parallel Termination (3-Resistor)



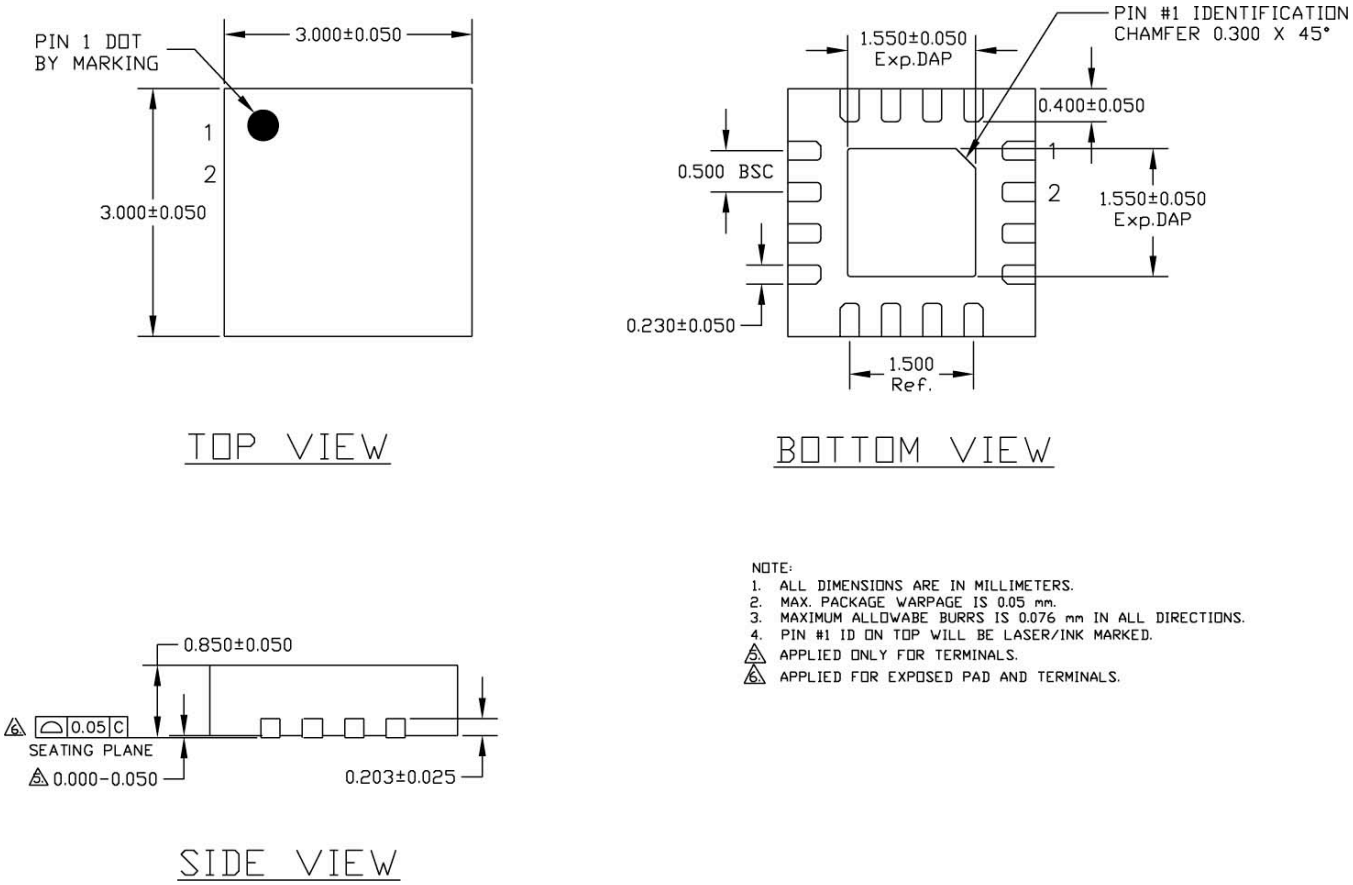
Note:
For +2.5V systems: Rb = 50Ω
For 3.3V systems Rb = 100Ω
The output pair requires a DC-current path to GND.

Figure 5c. AC-Coupled Output Pull-down Resistors

Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY89852U	Precision Low Power Differential 2:1 LVPECL MUX w/Internal Termination	www.micrel.com/product-info/products/sy89852u.shtml
	MLF® Application Note	www.amkor.com/products/notes_papers/MLF_AppNote.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Package Information



16-Pin (3mm x 3mm) MLF® (MLF-16)

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