

### **FEATURES**

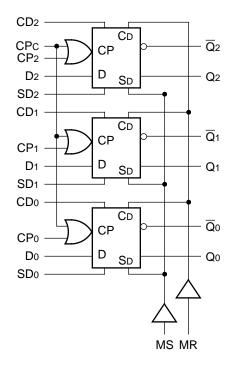
- Max. toggle frequency of 800MHz
- **■** Differential outputs
- IEE min. of -80mA
- Industry standard 100K ECL levels
- Extended supply voltage option: VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75k $\Omega$  input pull-down resistors
- 150% faster than Fairchild
- 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

## **DESCRIPTION**

The SY100S331 offers three D-type, edge-triggered master/slave flip-flops with true and complement outputs, designed for use in high-performance ECL systems. Each flip-flop is controlled by a common clock (CPc), as well as its own clock pulse (CPn). The resultant clock signal controlling the flip-flop is the logical OR operation of these two clock signals. Data enters the master when both CPc and CPn are LOW and enters the slave on the rising edge of either CPc or CPn (or both).

Additional control signals include Master Set (MS) and Master Reset (MR) inputs. Each flip-flop also has its own Direct Set (SDn) and Direct Clear (CDn) signals. The MR, MS, SDn and DCn signals override the clock signals. The inputs on this device have  $75k\Omega$  pull-down resistors.

### **BLOCK DIAGRAM**

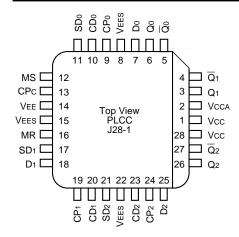


## **PIN NAMES**

Pin	Function
CP0 - CP2	Individual Clock Inputs
CPc	Common Clock Input
D0 - D2	Data Inputs
CD0 - CD2	Individual Direct Clear Inputs
SDn	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q0 – Q2	Data Outputs
$\overline{Q}_0 - \overline{Q}_2$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

Micrel, Inc. SY100S331

# PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

# **Ordering Information**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S331JC	J28-1	Commercial	SY100S331JC	Sn-Pb
SY100S331JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S331JC	Sn-Pb
SY100S331JZ <sup>(2)</sup>	J28-1	Commercial	SY100S331JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S331JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S331JZ with Pb-Free bar-line indicator	Matte-Sn

#### Notes:

- 1. Tape and Reel.
- 2. Pb-Free package is recommended for new designs.

### **TRUTH TABLES**

	Asynchronous Operation <sup>(1)</sup>								
	Outputs								
Dn	CPn	СРс	MS SDn	MR DCn	Qn (t+1)				
Х	Х	Х	Н	L	Н				
Х	Х	Х	L	Н	L				
Х	Х	Х	Н	Н	U				

#### NOTE:

 H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

Synchronous Operation <sup>(1)</sup>								
	Outputs							
Dn	CPn	Qn						
L	u	L	L	L	L			
Н	u	L	L	L	Н			
L	L	u	L	L	L			
Н	L	u	L	L	Н			
Х	L	L	L	L	Qn (t)			
Х	Н	Х	L	Ĺ	Qn (t)			
Х	Х	Н	L	L	Qn (t)			

#### NOTE:

 H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

# DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

Symbol	Parameter	Min.	Тур.	Max.	Unit	Condition		
lін	Input HIGH Current, All Inputs	1	_	200	μΑ	VIN = VIH (Max.)		
IEE	Power Supply Current	-80	-65	-35	mA	Inputs Open		

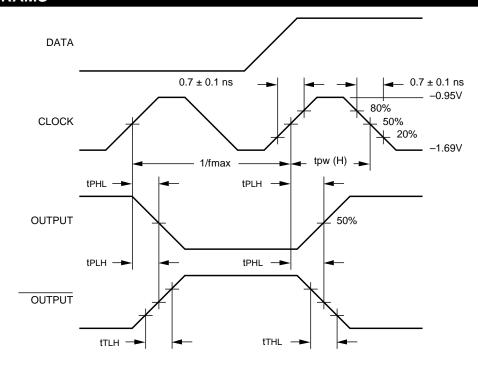
# **AC ELECTRICAL CHARACTERISTICS**

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

		TA = 0°C TA = +25°C		TA = +85°C					
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
fmax	Toggle Frequency	800	_	800	_	800	_	MHz	
tPLH tPHL	Propagation Delay CPc to Output	300	700	300	700	300	700	ps	
tPLH tPHL	Propagation Delay CPn to Output	300	700	300	700	300	700	ps	
tPLH tPHL	Propagation Delay CDn, SDn to Output	300	800	300	800	300	800	ps	
tPLH tPHL	Propagation Delay MS, MR to Output	300	900	300	900	300	900	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts	Set-up Time Dn CDn, SDn (Release Time) MS, MR (Release Time)	400 500 800	_ _ _	400 500 800	_ _ _	400 500 800		ps	
tH	Hold Time Dn	300	_	300		300	_	ps	
tpw (H)	Pulse Width HIGH CPn, CPc, DCn SDn, MR, MS	800	_	800	_	800	_	ps	

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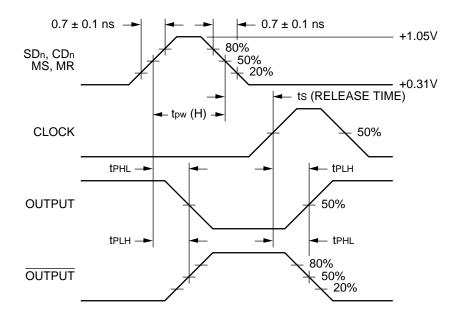
## **TIMING DIAGRAMS**



**Propagation Delay (Clock) and Transition Times** 

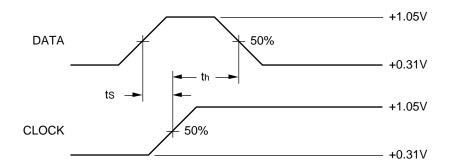
#### Note:

Vee = -4.2V to -5.5V unless otherwise specified, Vcc = VccA = GND



**Propagation Delay (Sets and Resets)** 

# **TIMING DIAGRAMS**



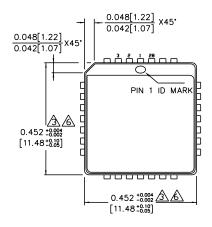
**Data Setup and Hold Time** 

#### Notes:

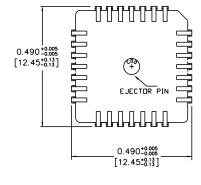
ts is the minimum time before the transition of the clock that information must be present at the data input. th is the minimum time after the transition of the clock that information must remain unchanged at the data input.

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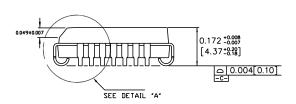
## 28-PIN PLCC (J28-1)



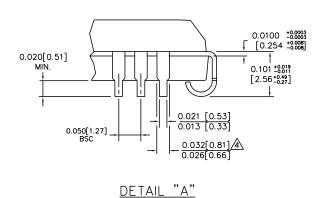
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Rev. A

### NOTES:

- DITES:
  DIMENSIONS ARE IN INCHES [MM].
  CONTROLLING DIMENSION: INCHES.
  DIMENSION DOES NOT INCLUDE MOLD FLASH
  OR PROTRUSIONS, EITHER OF WHICH SHALL NOT
  EXCEED 0.008 [0.203].
  LEAD DIMENSION DOES NOT INCLUDE DAMBAR
  PROTRUSION.
  MAXIMUM AND MINIMUM SPECIFICATIONS ARE
  INDICATED AS FOLLOWS: MAX/MIN
  ANCHAGE TOP DIMENSION MAY BE SLIGHTLY
- - PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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