



STSJ50NH3LL

N-channel 30 V - 0.008 Ω - 12 A - PowerSO-8™
ultra low gate charge STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} (max)	I _D
STSJ50NH3LL	30V	< 0.0105 Ω	12A ⁽¹⁾

- Optimal R_{DS(on)} x Q_g trade-off @ 4.5V
- Reduced switching losses
- Reduced conduction losses
- Improved junction-case thermal resistance

Applications

- Switching application

Description

This series utilizes the latest advanced design rules of ST's proprietary STripFET™ technology, and a proprietary process for integrating a monolithic Scottky diode. The new Power MOSFET is optimized for the most demanding synchronous switch function in DC-DC converter for computer and telecom.

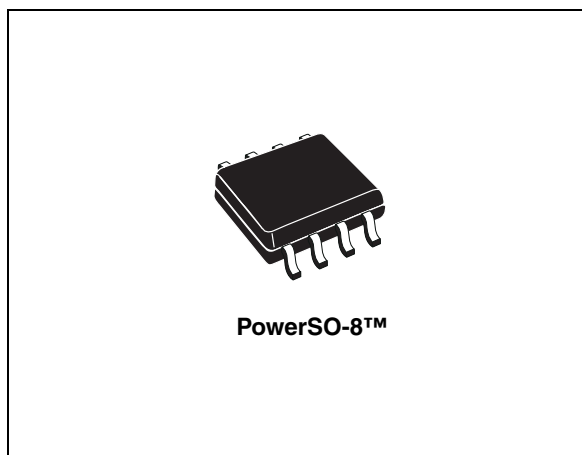


Figure 1. Internal schematic diagram

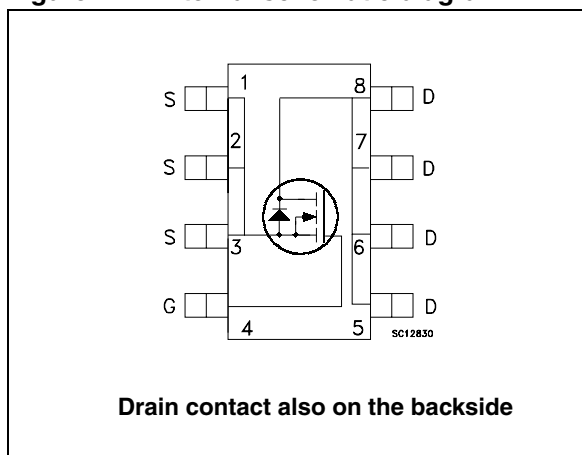


Table 1. Device summary

Order code	Marking	Package	Packaging
STSJ50NH3LL	50H3LL-	PowerSO-8	Tape & reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
$V_{GS}^{(1)}$	Gate-source voltage	± 16	V
$V_{GS}^{(2)}$	Gate-source voltage	± 18	V
$I_D^{(4)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	50	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	12	A
$I_D^{(4)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	31.3	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	7.5	A
$I_{DM}^{(5)}$	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$ ⁽³⁾	3	W
	Total dissipation at $T_C = 25^\circ\text{C}$ ⁽⁴⁾	50	W
T_J	Operating junction temperature	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature		

1. Continuous mode
2. Guaranteed for test time $\leq 15\text{ms}$
3. This value is rated accordingly to $R_{thj-pcb}$
4. This value is rated accordingly to R_{thj-c}
5. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
R_{thj-c}	Thermal resistance junction-case Max	2.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb Max	42	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4 board, 2oz Cu ($t < 10\text{sec.}$)

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not repetitive avalanche current	7.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$, $I_D = 7.5\text{ A}$)	150	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ $T_C=125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$, $I_D = 6\ \text{A}$ $V_{GS} = 4.5\ \text{V}$, $I_D = 6\ \text{A}$		0.008 0.010	0.0105 0.013	Ω Ω
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$, $I_D = 6\ \text{A}$ @ 125°C $V_{GS} = 4.5\ \text{V}$, $I_D = 6\ \text{A}$ @ 125°C		0.012 0.016		Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10\ \text{V}$, $I_D = 12\ \text{A}$		38		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$		965 285 38		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 15\ \text{V}$, $I_D = 12\ \text{A}$ $V_{GS} = 4.5\ \text{V}$, (see Figure 16)		9 3.7 3	12	nC nC nC
R_G	Gate input resistance	$f = 1\ \text{MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	0.5	1.5	2.5	Ω

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=15\text{ V}$, $I_D=6\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 15)		15 32		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=15\text{ V}$, $I_D=6\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 15)		18 8.5		ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				12 48	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=12\text{ A}$, $V_{GS}=0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ (see Figure 20)		24 17.4 1.45		ns nC A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

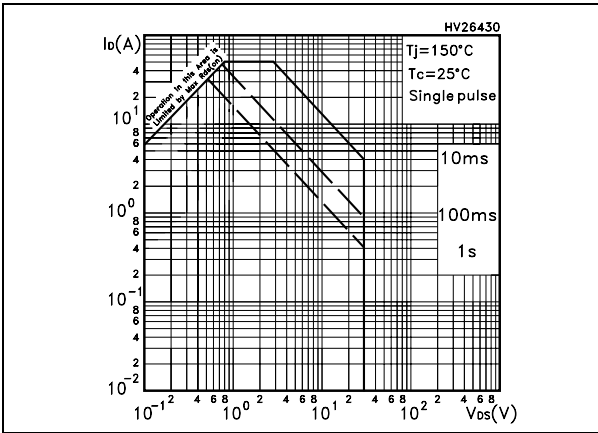


Figure 3. Thermal impedance

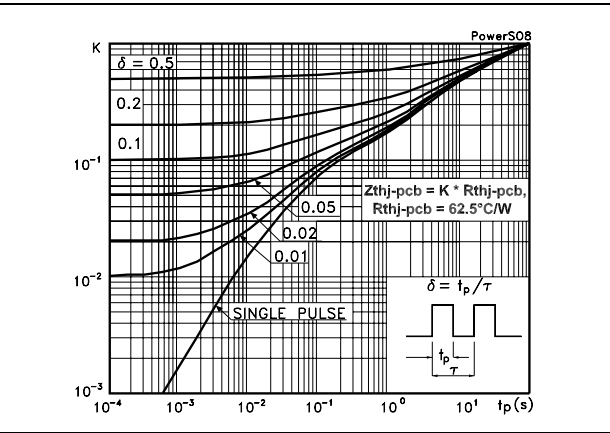


Figure 4. Output characteristics

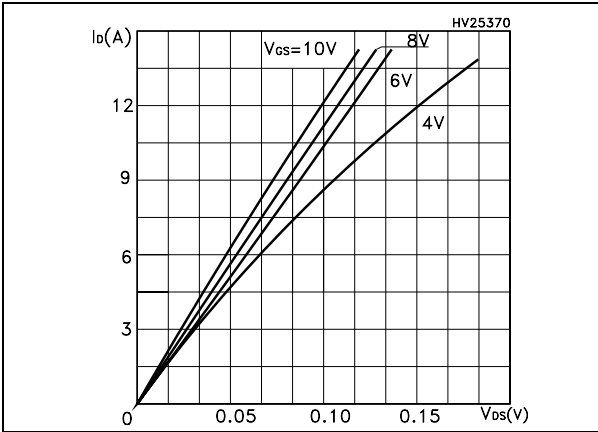


Figure 5. Transfer characteristics

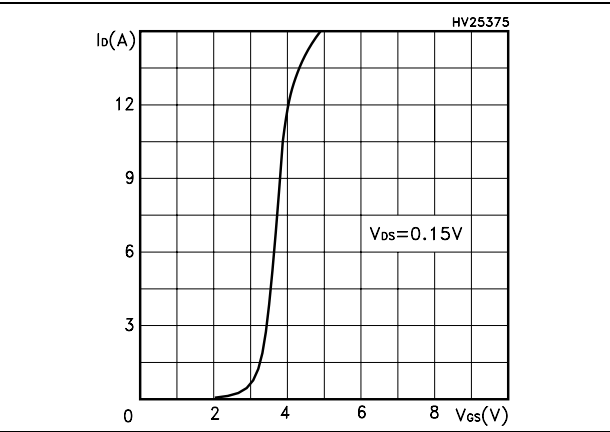


Figure 6. Transconductance

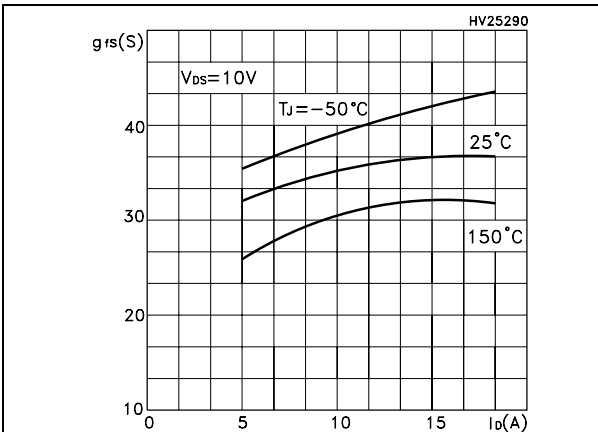


Figure 7. Static drain-source on resistance

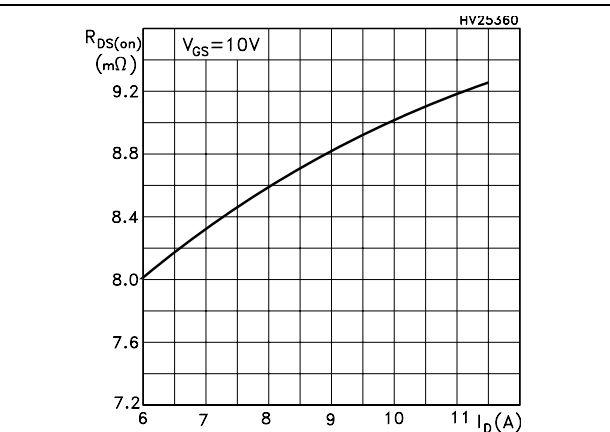


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

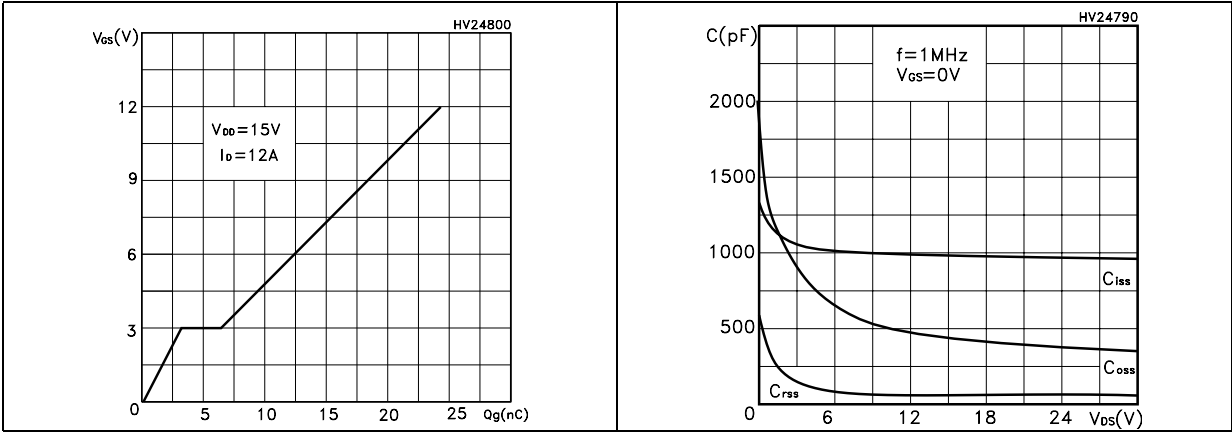


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

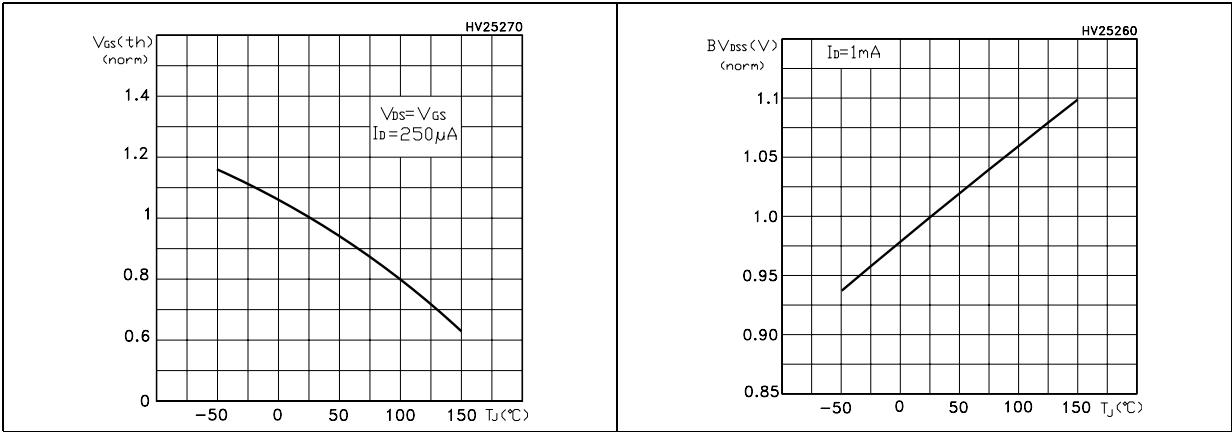


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized BV_{DSS} vs temperature

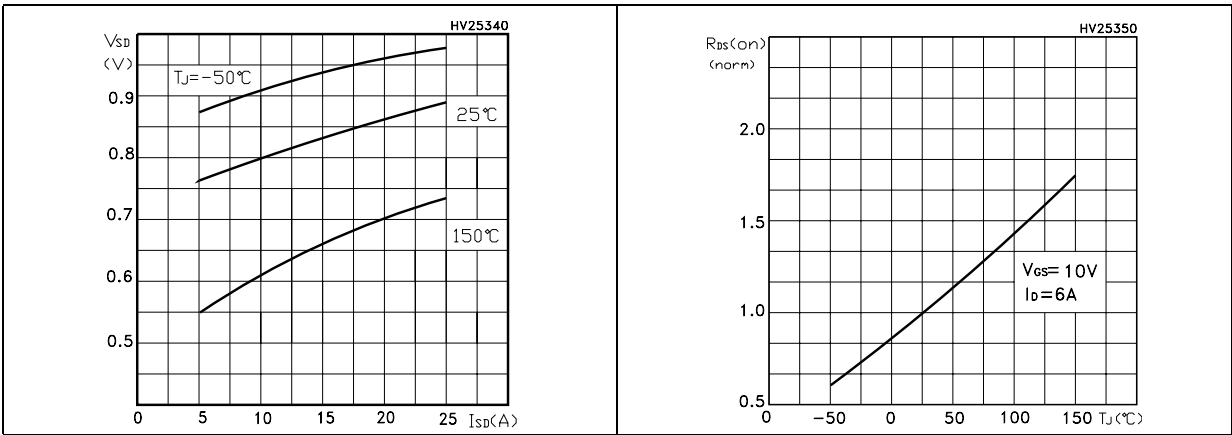
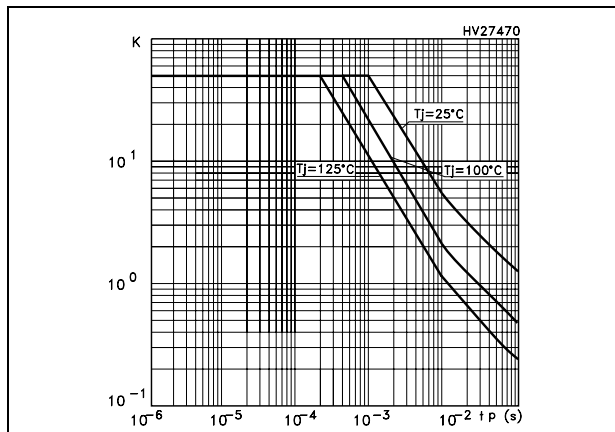


Figure 14. Allowable I_{AV} vs time in avalanche

The previous curve gives the single pulse safe operating area for unclamped inductive loads under the following conditions:

$$P_{D(AVE)} = 0.5 \cdot (1.3 \cdot BV_{DSS} \cdot I_{AV})$$

$$EAS_{(AR)} = P_{D(AVE)} \cdot t_{AV}$$

Where:

I_{AV} is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

t_{av} is the time in avalanche

3 Test circuit

Figure 15. Switching times test circuit for resistive load

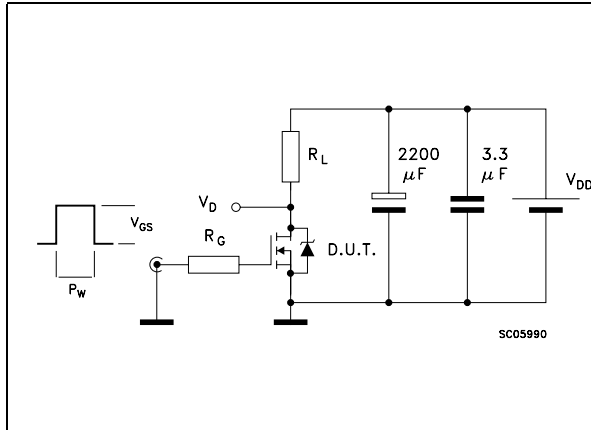


Figure 16. Gate charge test circuit

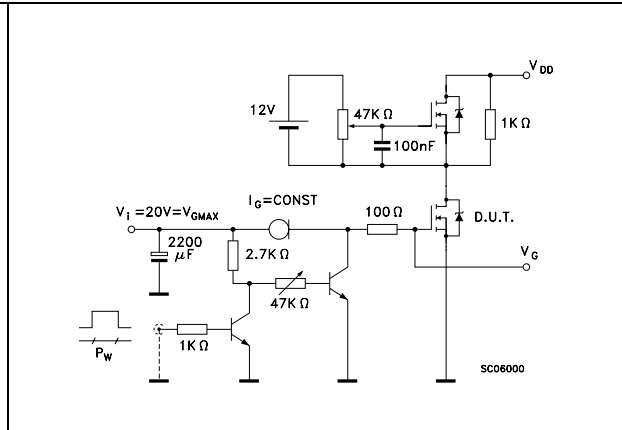


Figure 17. Test circuit for inductive load switching and diode recovery times

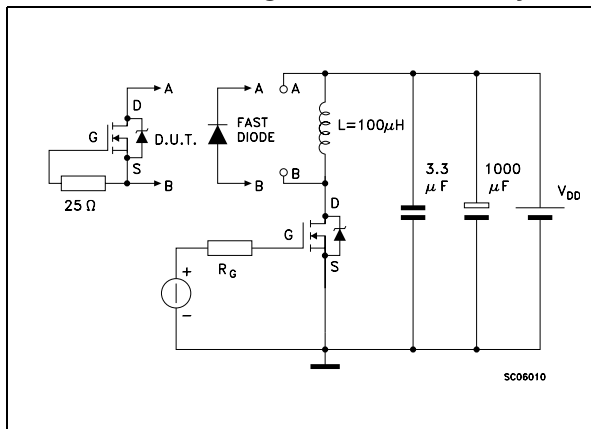


Figure 18. Unclamped inductive load test circuit

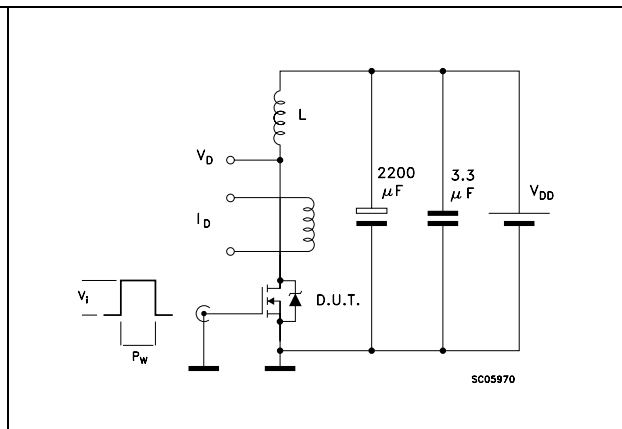


Figure 19. Unclamped inductive waveform

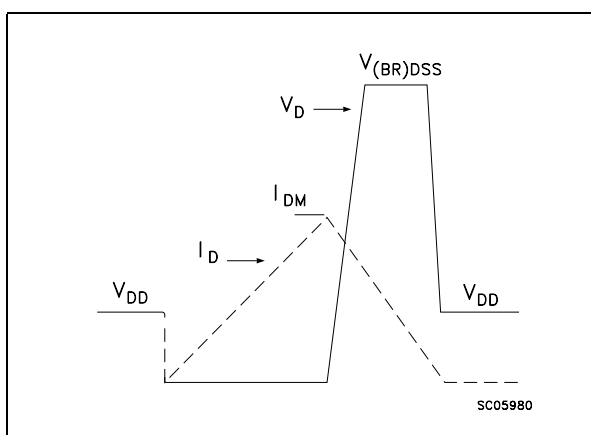
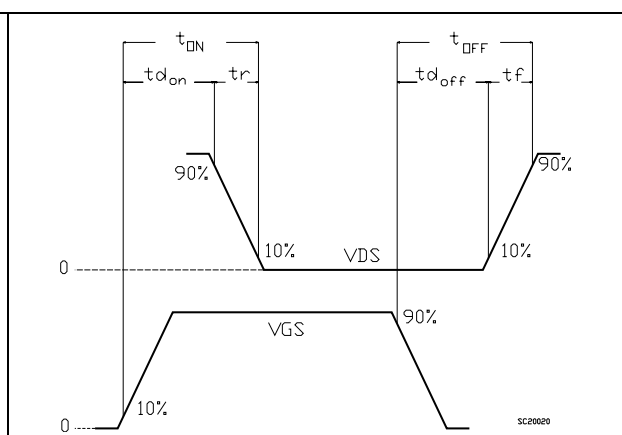


Figure 20. Switching time waveform

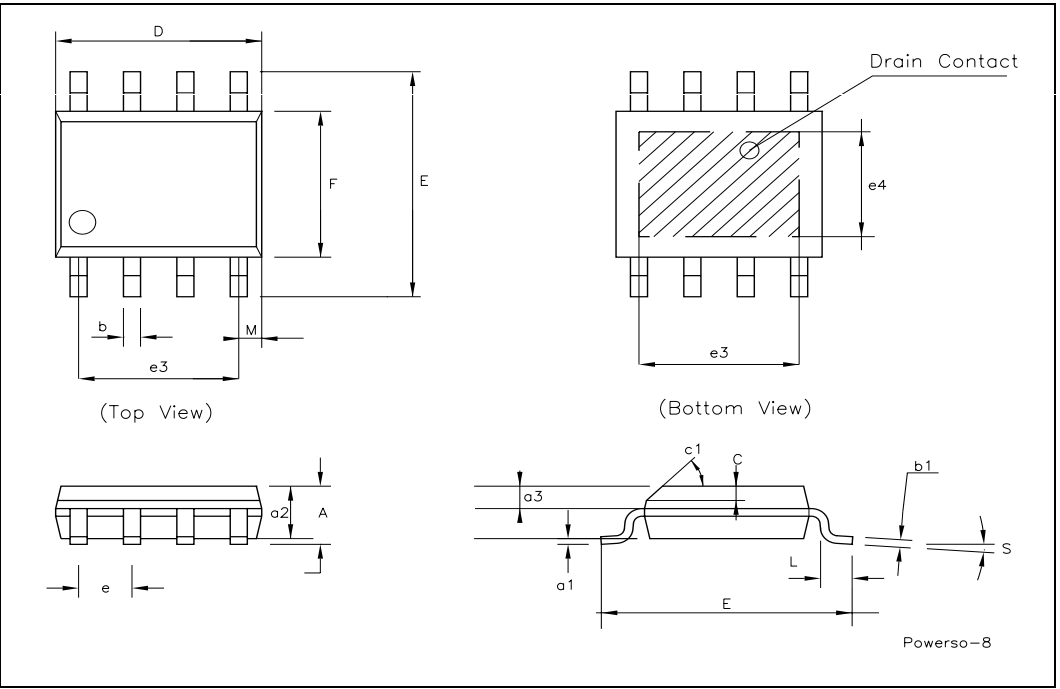


4 **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

PowerSO-8™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Jul-2004	1	Initial release.
24-May-2005	2	New value on Table 7
23-Jun-2005	3	New Rg value on Table 7
16-Nov-2005	4	Complete version
30-Mar-2006	5	New template
10-Dec-2007	6	Updated data on Table 4: Avalanche data

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