

STS5DPF20L

P-CHANNEL 20V - 0.045Ω - 5A SO-8 STripFETTM II MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS5DPF20L	20 V	$< 0.055 \Omega$	5 A

- TYPICAL $R_{DS(on)} = 0.045 \Omega$
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DRIVE
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY

DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low onresistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC/DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES
- DC MOTOR DRIVE

Figure 1: Package

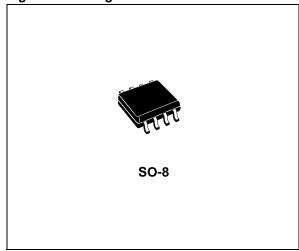


Figure 2: Internal Schematic Diagram

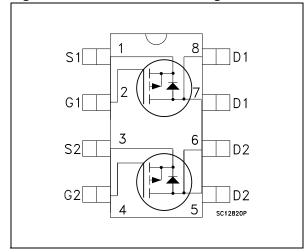


Table 2: Order Codes

PART NUMBER	MARKING	PACKAGE	PACKAGING
STS5DPF20L	S5DPF20L	SO-8	TAPE & REEL

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Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	20	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	20	V
V_{GS}	Gate- source Voltage	± 16	V
Ι _D	Drain Current (continuous) at T _C = 25°C Single Operating	5	А
Ι _D	Drain Current (continuous) at T _C = 100°C Single Operating	4	А
I _{DM} (•)	Drain Current (pulsed)	20	Α
Ртот	Total Dissipation at $T_C = 25^{\circ}C$ Dual Operating Total Dissipation at $T_C = 25^{\circ}C$ Single Operating	1.6 2	W W
T _j T _{stg}	Operating Junction Temperature Storage Temperature	150 -55 to 150	°C °C

(•) Pulse width limited by safe operating area
Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

Table 4: Thermal Data

Rthj-cas	e Thermal Resistance Junction-case Single Operating Dual Operating	62.5 78	°C/W
Tı	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 5: On/Off

Symbol	Parameter	Test Conditions	Min.	Тур.	Max	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0$	20			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	Voltage $V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$		1.6	2.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 2.5 A V _{GS} = 4.5 V, I _D = 2.5 A		0.045 0.070	0.055 0.075	Ω

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (1)	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_{D} = 2.5 \text{ A}$		10		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 16V, f = 1 \text{ MHz}, V_{GS} = 0$		1350 490 130		pF pF pF

(1) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

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ELECTRICAL CHARACTERISTICS(CONTINUED)

Table 7: Switching On

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	$V_{DD} = 15 \text{ V}, I_{D} = 2 \text{ A},$ $R_{G} = 4.7 \Omega, V_{GS} = 4.5 \text{ V}$ (see Figure 15))		25 35		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 24 V, I _D = 4 A, V _{GS} = 5 V (see, Figure 18)		12.5 5 3	16	nC nC nC

Table 8: Switching Off

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(off)}	Turn-off Delay Time Fall Time	$V_{DD} = 15 \text{ V}, I_D = 2.5 \text{ A}, R_{G} = 4.7 \Omega, V_{GS} = 4.5 \text{ V} $ (see, Figure 15)		125 35		ns ns

Table 9: Source-Drain Diodef

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain Current				5	Α
I _{SDM} (2)	Source-drain Current (pulsed)				20	Α
V _{SD} (1)	Forward On Voltage	I _{SD} = 5 A, V _{GS} = 0			1.2	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5 \text{ A}$, di/dt = 100 A/µs $V_{DD} = 15V$, $T_j = 150^{\circ}\text{C}$ (see, Figure 16)		45 36 1.6		ns nC A

⁽¹⁾ Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

⁽²⁾ Pulse width limited by safe operating area.

Figure 3: Safe Operating

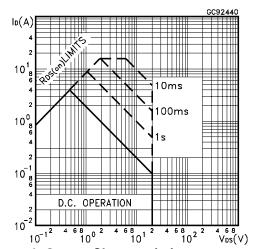


Figure 4: Output Characteristics

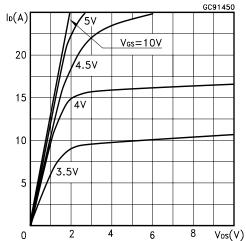


Figure 5: Transconductance

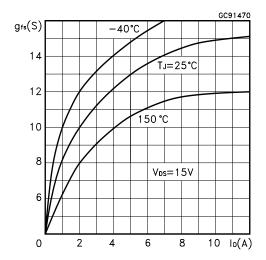


Figure 6: Thermal Impedance

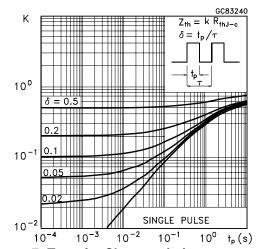


Figure 7: Transfer Characteristics

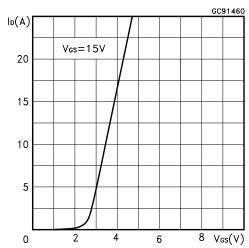
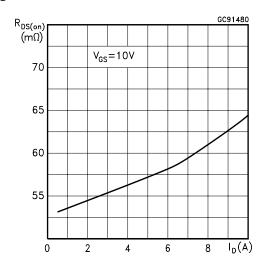


Figure 8: Static Drain-Source On Resistance



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Figure 9: Gate Charge vs Gate-Source Voltage

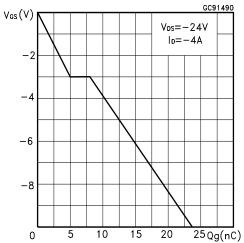


Figure 10: Normalized Gate Thereshlod Voltage vs Temperature

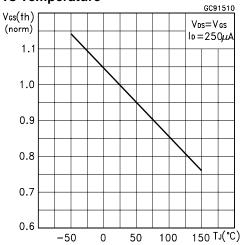


Figure 11: Source-Drain Diode Forward Characteristics

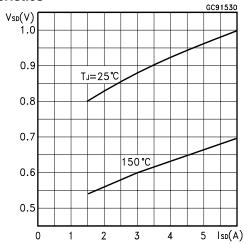


Figure 12: Capacitances Variations

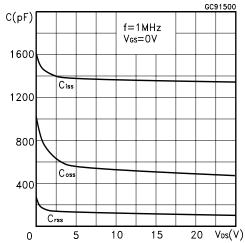


Figure 13: Normalized On Resistance vs Temperature

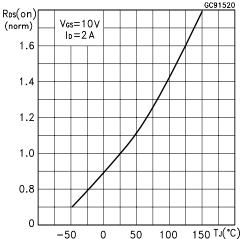


Figure 14: Unclamped Inductive Load Test Circuit

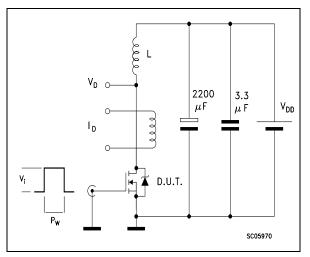


Figure 15: Switching Times Test Circuit For Resistive Load

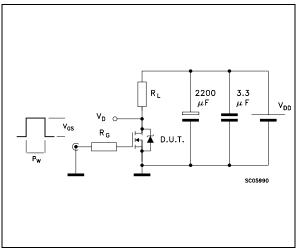


Figure 16: Test Circuit For Inductive Load Switching and Diode Recovery Times

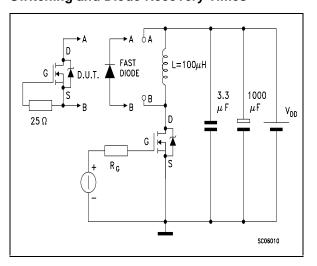


Figure 17: Unclamped Inductive Wafeform

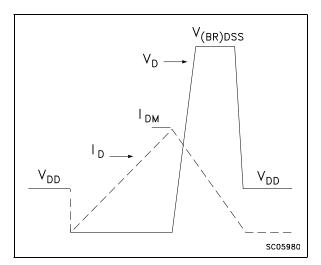
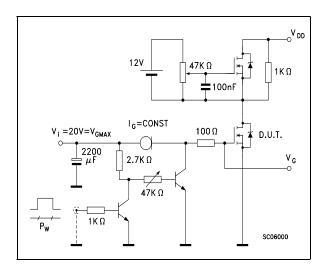


Figure 18: Gate Charge Test Circuit



SO-8	MECH	ANICA	L DATA
30-0			

DIM		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.019
c1			45 ((typ.)		•
D	4.8		5.0	0.188		0.196
Е	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
М			0.6			0.023
S		•	8 (n	nax.)	•	•

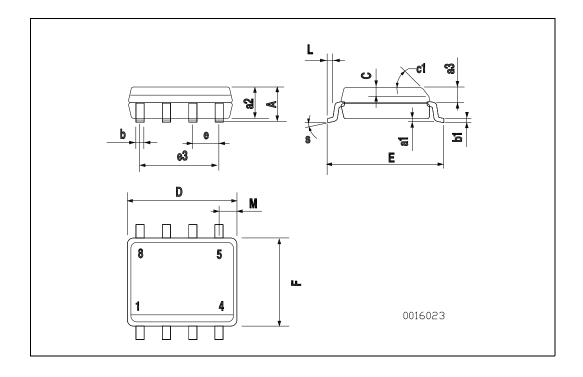


Table 10: Revision History

Date	Revision	Description of Changes
10-Sep-2004	2	Complete Version

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