



STB22NS25Z - STP22NS25Z

N-channel 250V - 0.13Ω - 22A - TO-220 / D²PAK
Zener-protected MESH OVERLAY™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STB22NS25Z	250V	<0.15Ω	22A
STP22NS25Z	250V	<0.15Ω	22A

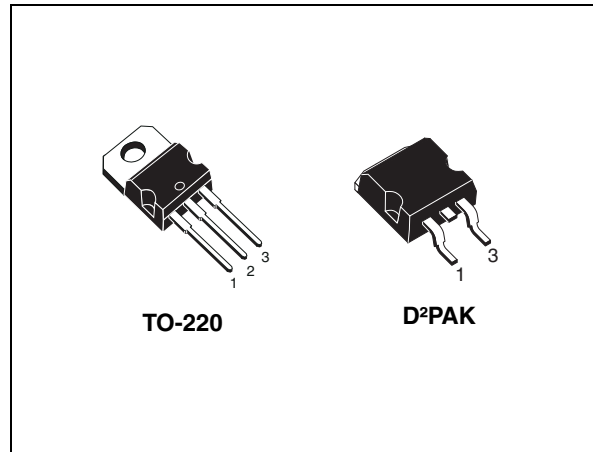
- 100% avalanche tested
- Extremely high dv/dt capability

Description

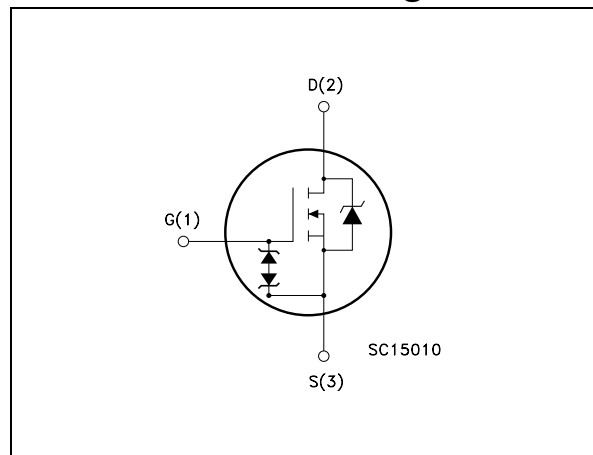
Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performance. The new patented STrip layout coupled with the Company's proprietary edge termination structure, makes it suitable in converters for lighting applications.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB22NS25Z	B22NS25Z	D ² PAK	Tape & reel
STP22NS25Z	P22NS25Z	TO-220	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	250	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	250	V
V_{GS}	Gate- source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	22	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	13.9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	88	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	135	W
	Derating factor	1.07	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	2500	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	5	V/ns
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 22\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 2. Thermal data

$R_{thj-case}$	Thermal resistance junction-case Max	0.93	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 3. Avalanche Characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	22	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$, $R_g = 47\Omega$)	350	mJ

2 Electrical characteristics

(T_{case} = 25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A$, $V_{GS} = 0$	250			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125^\circ C$			10 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 18V$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V$, $I_D = 11A$		0.13	0.15	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 11A$		22		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V$, $f = 1MHz$, $V_{GS} = 0$		2400 340 120		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 200V$, $I_D = 20A$, $V_{GS} = 10V$ (see Figure 13)		108 11 40	151	nC nC nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 125V$, $I_D = 11A$ $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see Figure 12)		20 30		ns ns
$t_{d(Voff)}$ t_f	Turn-off- delay time Fall time	$V_{DD} = 125V$, $I_D = 11 A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see Figure 12)		100 78		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	$V_{clamp} = 200V$, $I_D = 22 A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see Figure 12)		37 65 110		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				22	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				88	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 22 A$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 22 A$, $di/dt = 100A/\mu s$ $V_{DD} = 50V$, $T_j = 150^\circ C$ (see Figure 17)		292 3065 21		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{gs} = \pm 500\mu A$ (open drain)	20			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

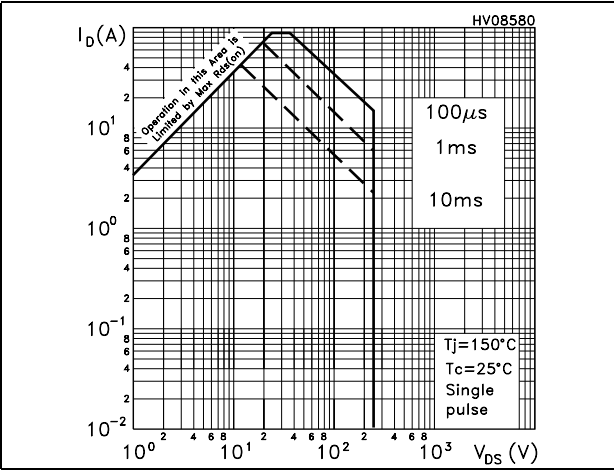


Figure 2. Thermal impedance

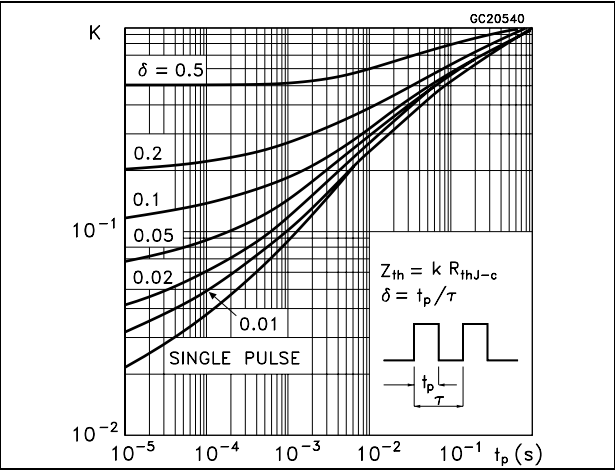


Figure 3. Output characteristics

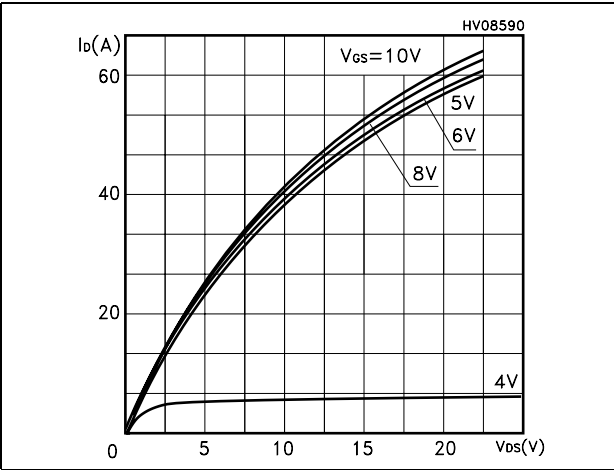


Figure 4. Transfer characteristics

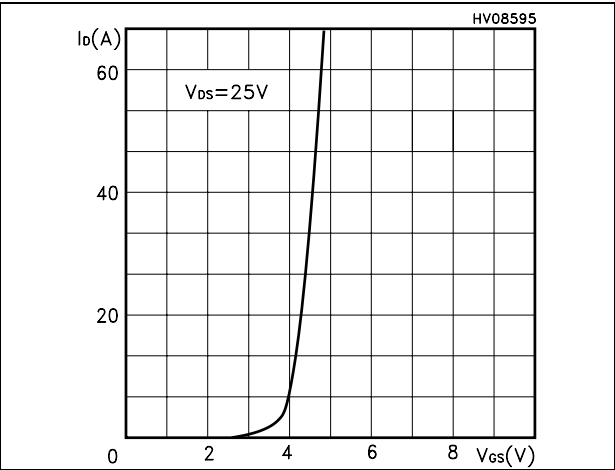


Figure 5. Transconductance

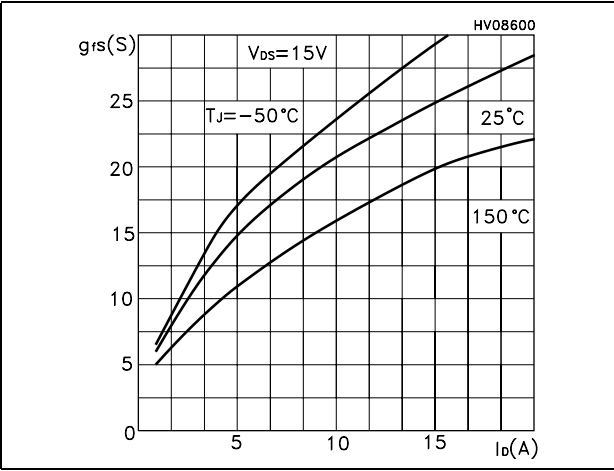


Figure 6. Static drain-source on resistance

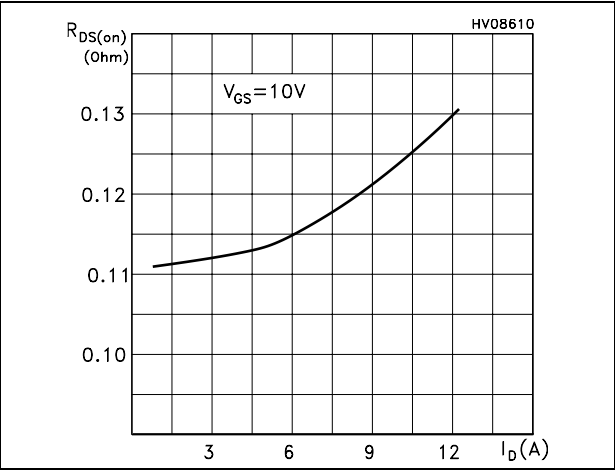


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

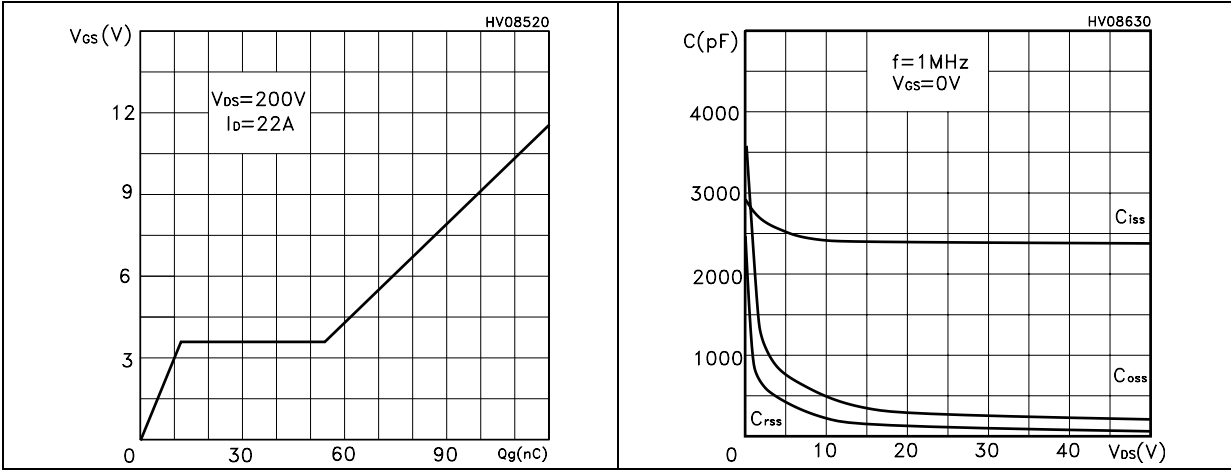


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

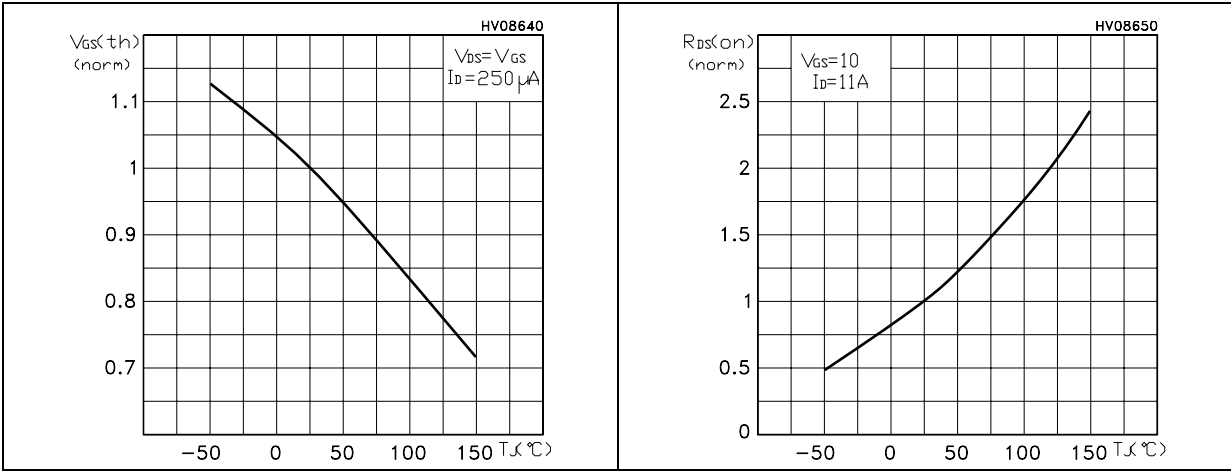
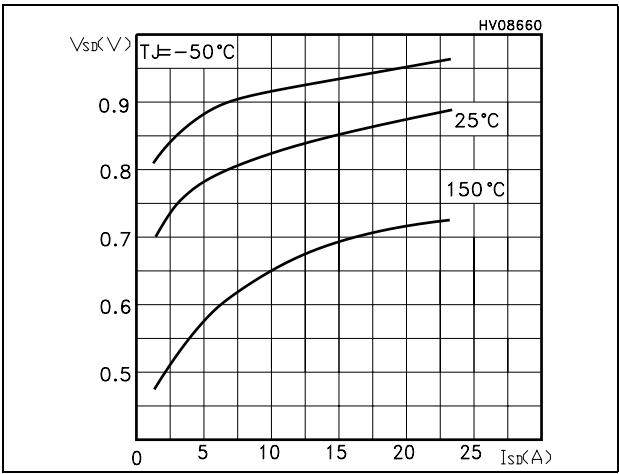


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Switching times test circuit for resistive load



Figure 13. Gate charge test circuit

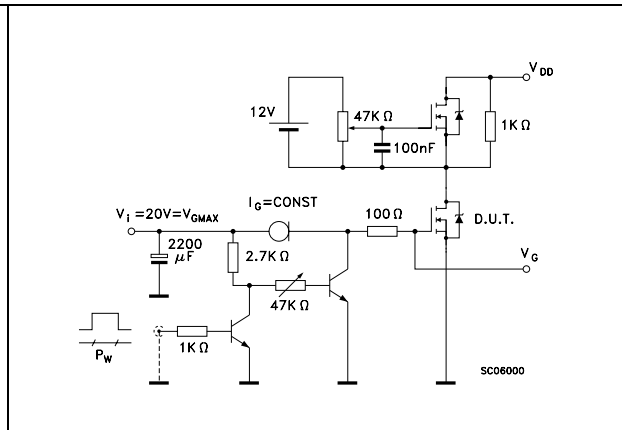


Figure 14. Test circuit for inductive load switching and diode recovery times

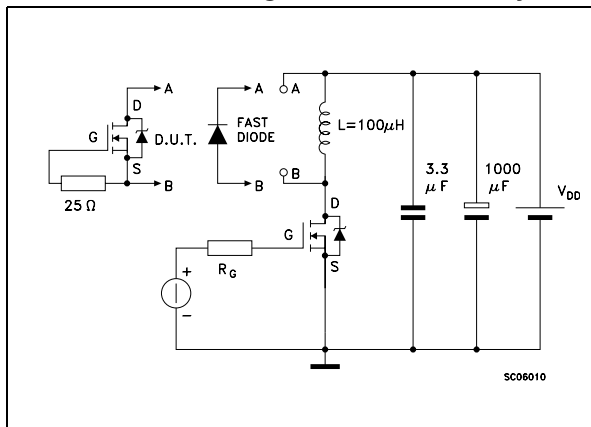


Figure 15. Unclamped Inductive load test circuit

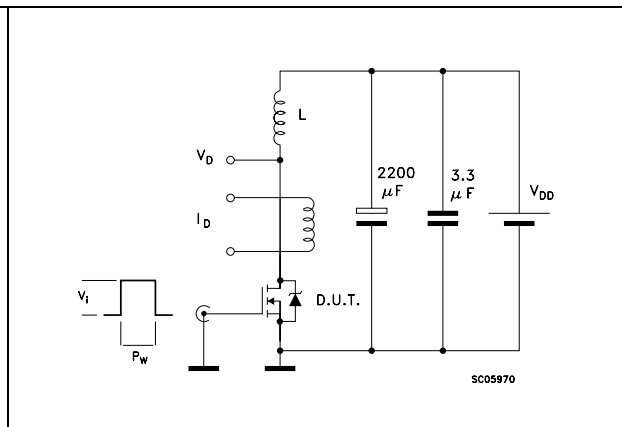


Figure 16. Unclamped inductive waveform

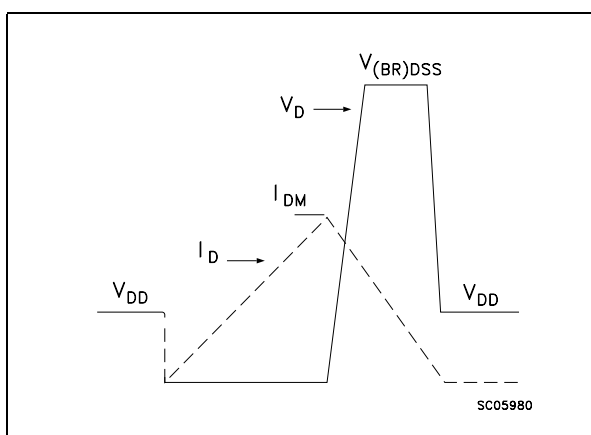
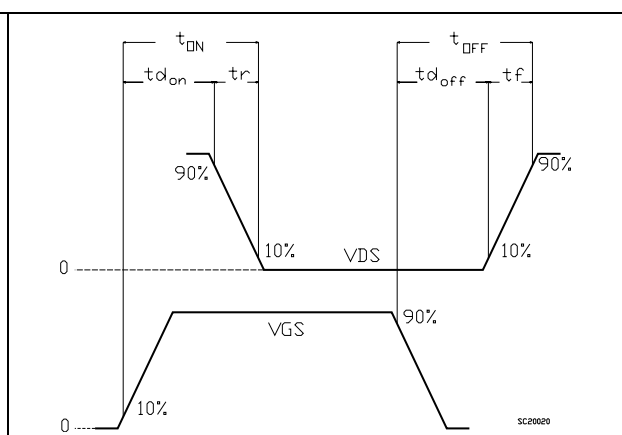


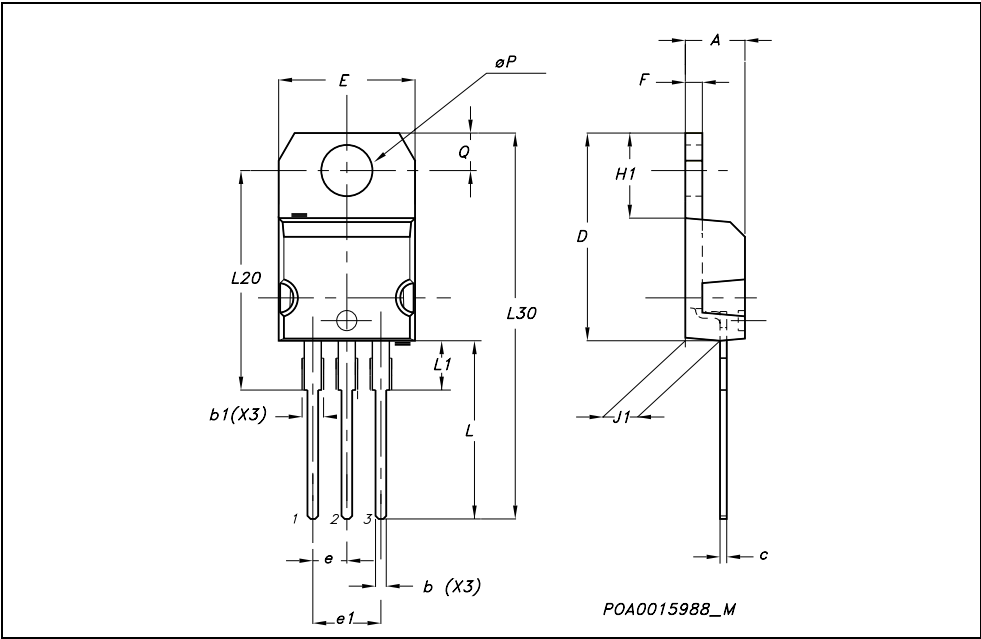
Figure 17. Switching time waveform



4 Package mechanical data

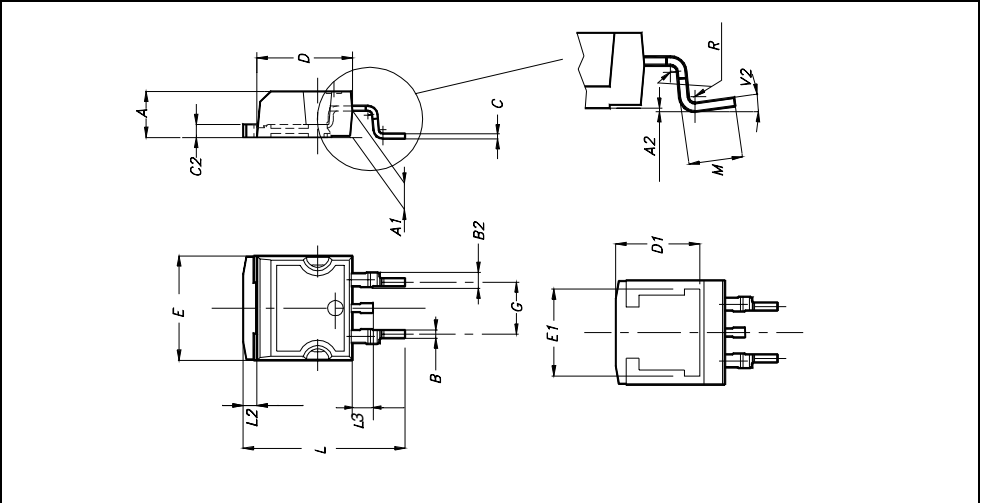
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



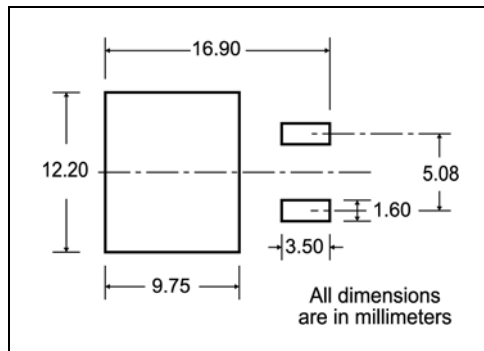
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

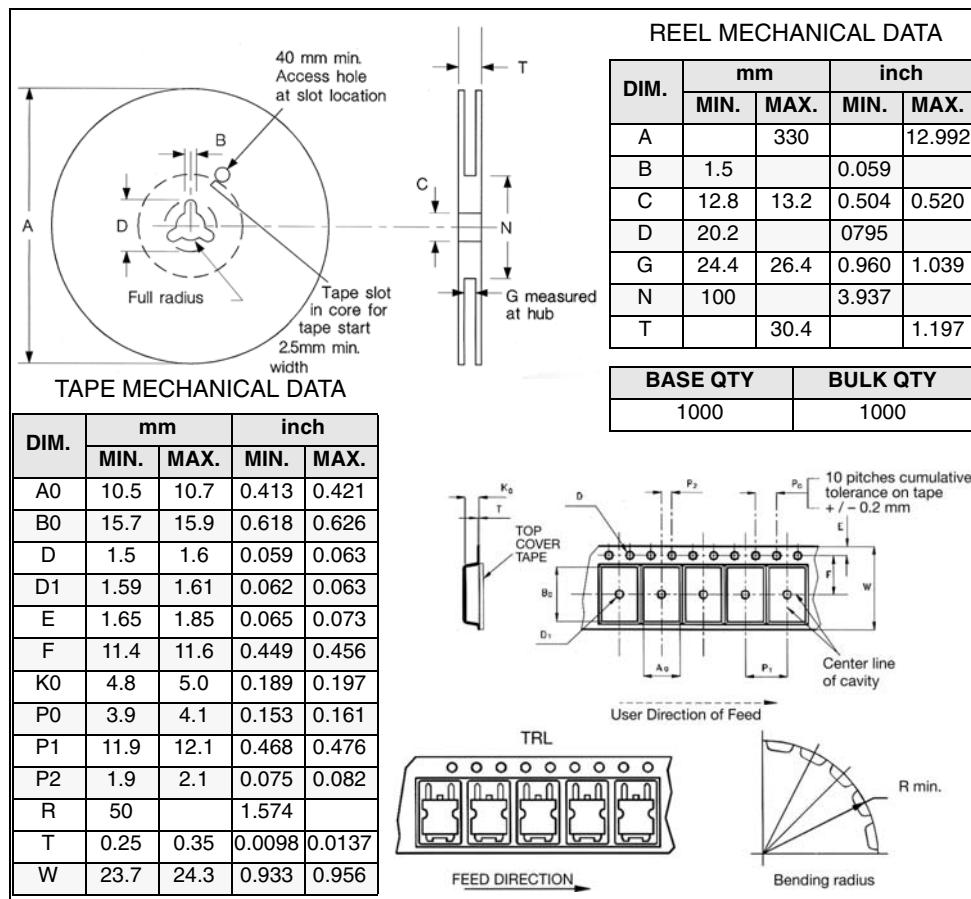


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 9.

Date	Revision	Changes
06-Jun-2006	2	New template

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