STOD1412

Step-up and inverting DC-DC converter

Features

- 2.7 V to 5.5 V input voltage range
- 120 mA max output current for each converter
- Output voltages:
  - Step-up from 4.3 V to 6.0 V
  - Inverting from -8.0 V to -2.0 V
- Synchronous rectification for both DC-DC converters
- Efficiency:
  - 80% I_O = 10 mA - 30 mA
  - 85% I_O = 30 mA - 120 mA
- 1.3 MHz PWM mode control
- Shutdown mode with Enable pin
- Inrush current protection
- Adjustable output voltages
- True shutdown mode
- Less than 1 µA current consumption in shutdown mode
- Over-temperature protection
- Package: 16 pin - QFN 3X3
- Temperature range: -40°C to 85°C

Applications

- Active matrix organic LED power supplies
- Mobile phones
- PDAs
- Camcorders
- Digital still cameras

QFN16L (3mm x 3mm)

Description

The STOD1412 is a dual DC-DC converter capable of providing a positive and negative voltage from a positive input voltage ranging from 2.7 V to 5.5 V. It integrates two complete power stages, one step-up and one inverting, each of which need just one inductor, and input and output capacitor.

The STOD1412 works in PWM mode, switching at a 1.3 MHz frequency, thus reducing the size and values of external components. An Enable pin makes it possible to turn off the device to reduce the quiescent current to less than 1 µA. The output voltages can be set easily by using two external resistors for each converter.

The device integrates a “soft start” with controlled inrush current limit, thermal shutdown and short circuit protection.

High efficiency and low quiescent current, combined with the small number and tiny size of external components, make the STOD1412 suitable for battery-operated systems, particularly for powering Active Matrix OLED display panels.

Table 1. Device summary

Order code	Package	Packaging
STOD1412PUR	QFN16L (3x3 mm)	4500 parts per reel

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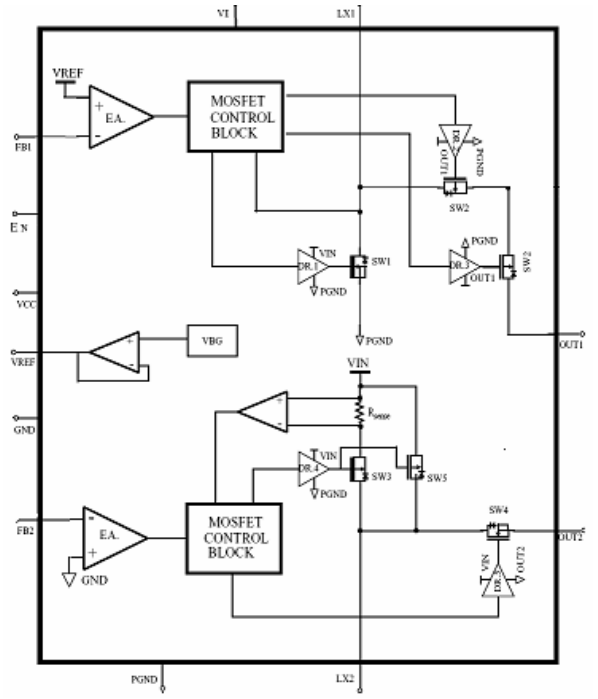
1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connections (top view)

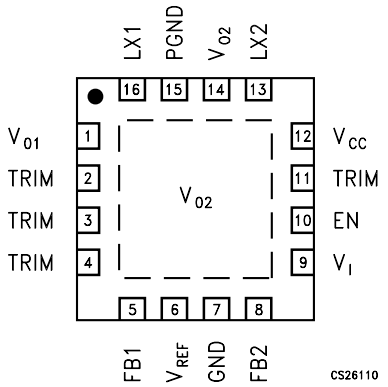


Table 2. Pin description

Pin n°	Symbol	Description
1	V_{O1}	Step-up converter output voltage.
2	TRIM	Trimming pin. This pin must be left floating.
3	TRIM	Trimming pin. This pin must be left floating.
4	TRIM	Trimming pin. This pin must be left floating.
5	FB1	Feedback pin of the step-up converter.
6	V_{REF}	External voltage reference. A C_{REF} = 100 nF ceramic capacitor must be connected to this pin.
7	GND	Signal ground pin. This pin must be connected to PGND pin.
8	FB2	Feedback pin of the inverting converter.
9	V_I	Input supply voltage.
10	EN	Enable control pin. ON = V_I. When pulled low the device goes into shutdown mode.
11	TRIM	Trimming pin; this pin must be left floating.
12	V_{CC}	Power input supply voltage.
13	Lx2	Switching node of the inverting converter.
14	V_{O2}	Inverting converter output voltage.
15	PGND	Power ground pin.
16	Lx1	Switching node of the step-up converter.
	Exp pad	Exposed pad. This pin must be connected to V_{O2}.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I, V_{CC}	DC supply voltage	-0.3 to 6	V
EN	Enable pin	-0.3 to 6	V
ILx_2	Switching current of the converter	Internally limited	A
Lx_2	Inverting converter switching node	-10 to V_I+0.3	V
V_{O2}	Inverting converter output voltage	F10 to GND+0.3	V
FB_2	Inverting converter feedback pin	-1 to +1	V
FB_1	Step-up converter feedback pin	-0.3 to V_I+0.3	V
V_{O1}	Step-up converter output voltage	-0.3 to 6	V
Lx_1	Step-up converter switching node	-0.3 to OUT_1+0.3	V
ILx_1	Step-up converter's switching current	Internally limited	A
V_{REF}	Reference voltage	-0.3 to 3	V
P_D	Power dissipation	Internally Limited	mW
X	Storage temperature range	-65 to 150	°C
T_J	Operating junction temperature range	-40 to 85	°C

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	49	°C/W

4 Electrical characteristics

Table 5. Electrical characteristics
(T_J=25°C, V_I =V_{CC}=3.7 V, C_I=2.2 µF, $C_{O1,2}$=4.7 µF, C_3=1 µF, C_{REF}=100 nF, L1=4.7 µH, L2=6.8 µH, $I_{O1,2}$=I_{O1}-I_{O2}=30 mA, V_{EN}=V_I, V_{O1}=4.6 V, V_{O2}=-6.4 V, R_1=470 kΩ, R_2=166 kΩ, R_3=533 kΩ, R_4=100 kΩ, unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply section						
V_I	Supply input voltage		2.7		5.5	V
	Operating input voltage range		2.7		4.5	
UVLO_H	Under voltage lockout HIGH	VCC		2.55		V
UVLO_L	Under voltage lockout LOW			2.5		V
I_V_I	Input current	V_{FB1}=1.3 V, V_{FB2}= -0.5 V (no switching)		0.5	1	mA
		No Load		3.5		
I_Q	Quiescent current	V_{EN}=GND			1	µA
V_{EN} H	Enable high threshold	V_I=2.7 V to 4.5 V	1.2			
V_{EN} L	Enable low threshold	V_I=2.7 V to 4.5 V			0.6	V
I_{EN}	Enable input current	V_{EN}=V_I			1	µA
Dynamic performance						
Freq.	Frequency			1.3		MHz
$D1_{MAX}$	Maximum duty cycle	No load		90		%
$D2_{MAX}$	Maximum duty cycle	No load		90		%
	Total system efficiency	$I_{O1,2}$=10 to 30 mA, V_{O1}=4.6 V, V_{O2}= -6.4 V		80		%
		$I_{O1,2}$=30 to 120 mA, V_{O1}=4.6 V, V_{O2}= -6.4 V		85		
Step-up converter section						
V_{FB1}	Feedback voltage on step-up (1)	V_I=2.7 V to 4.5 V		1.20		V
ΔV_{O1}	Static line regulation	V_I=2.7 V to 4.2 V, I_{O1}=5 mA, I_{O2} no load, T_J= -40°C to 85°C		2		%
ΔV_{O1}	Static line regulation	V_I=2.7 V to 4.2 V, I_{O1}=100 mA, I_{O2} no load, T_J= -40°C to 85°C		2		%

Table 5. Electrical characteristics (continued)
(T_J=25°C, V_I =V_{CC}=3.7 V, C_I=2.2 µF, $C_{O1,2}$=4.7 µF, C_3=1 µF, C_{REF}=100 nF, L1=4.7 µH, L2=6.8 µH, $I_{O1,2}$=I_{O1}-I_{O2}=30 mA, V_{EN}=V_I, V_{O1}=4.6 V, V_{O2}=-6.4 V, R_1=470 kΩ, R_2=166 kΩ, R_3=533 kΩ, R_4=100 kΩ, unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ΔV_{O1}	Static load regulation	I_{O1}=5 to 100 mA, I_{O2} no load, V_I=2.7 V, T_J= -40°C to 85°C		2		%
ΔV_{O1}	Static load regulation	I_{O1}=5 to 100 mA, I_{O2} no load, V_I=4.2 V, T_J= -40°C to 85°C		2		%
ΔV_{O1}	Load transient regulation	I_{O1}=3 to 30 mA and I_{O1}=30 to 3 mA, T_R=T_F=30 µs			20	mV
ΔV_{O1}	Load transient regulation	I_{O1}=10 to 100 mA and I_{O1}=100 to 10 mA, T_R=T_F=30 µs			30	mV
ΔV_{O1}	Ripple output voltage range	I_{O1}=5 to 100 mA @ Low frequency typ.=20 kHz			20	mV
I_{O1}	Step-up range load current				120	mA
I-L_{1MAX}	I peak current	V_{O1} below 10% of nominal value		0.9		A
R_{DSON}P1				1.10		Ω
R_{DSON}N1				0.85		Ω
Inverting converter section						
V_{FB2}	Feedback voltage on inverting (1)	V_I=2.7 V to 4.5 V		-0.5		mV
ΔV_{O2}	Static line regulation	V_I=2.7 V to 4.2 V, I_{O2}=5 mA, I_{O1} no load, T_J= -40°C to 85°C		2		%
ΔV_{O2}	Static line regulation	V_I=2.7 V to 4.2 V, I_{O2}=100 mA, I_{O1} no load, T_J= -40°C to 85°C		2		%
ΔV_{O2}	Static load regulation	I_{O2}=5 to 100 mA, I_{O1} no load, V_I=2.7 V, T_J= -40°C to 85°C		2		%
ΔV_{O2}	Static load regulation	I_{O2}=5 to 100 mA, I_{O1} no load, V_I=4.2 V, T_J= -40°C to 85°C		2		%
ΔV_{O2}	Load transient regulation	I_{O2}=3 to 30 mA and I_{O2}=30 to 3 mA, T_R=T_F=30 µs			50	mV
ΔV_{O2}	Load transient regulation	I_{O2}=10 to 100 mA and I_{O2}=100 to 10 mA, T_R=T_F=30 µs			100	mV
ΔV_{O2}	Ripple output voltage range	I_{O2}=5 to 100 mA @ Low frequency typ.=20 kHz			20	mV
I_{O2}	Inverting range load current		-120			mA
I-L_{2MAX}	I peak current	V_{O2} below 10% of nominal value		-1		A
R_{DSON}P2				0.63		Ω
R_{DSON}N2				0.65		Ω
V_{REF}	Voltage reference	I_{REF}=10 µA	1.192	1.209	1.228	V

Table 5. Electrical characteristics (continued)
(T_J=25°C, V_I =V_{CC}=3.7 V, C_I=2.2 µF, $C_{O1,2}$=4.7 µF, C_3=1 µF, C_{REF}=100 nF, L1=4.7 µH, L2=6.8 µH, $I_{O1,2}$=I_{O1}-I_{O2}=30 mA, V_{EN}=V_I, V_{O1}=4.6 V, V_{O2}=-6.4 V, R_1=470 kΩ, R_2=166 kΩ, R_3=533 kΩ, R_4=100 kΩ, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
I_{REF}	Voltage reference current capability	V_{REF} = 1.192 V	100			µA
Thermal shutdown						
OTP	Over-temperature protection			140		°C
OTP_{HYST}	Over-temperature protection hysteresis			15		°C

1. Guaranteed by design.
2. The tolerance of external components is not included.

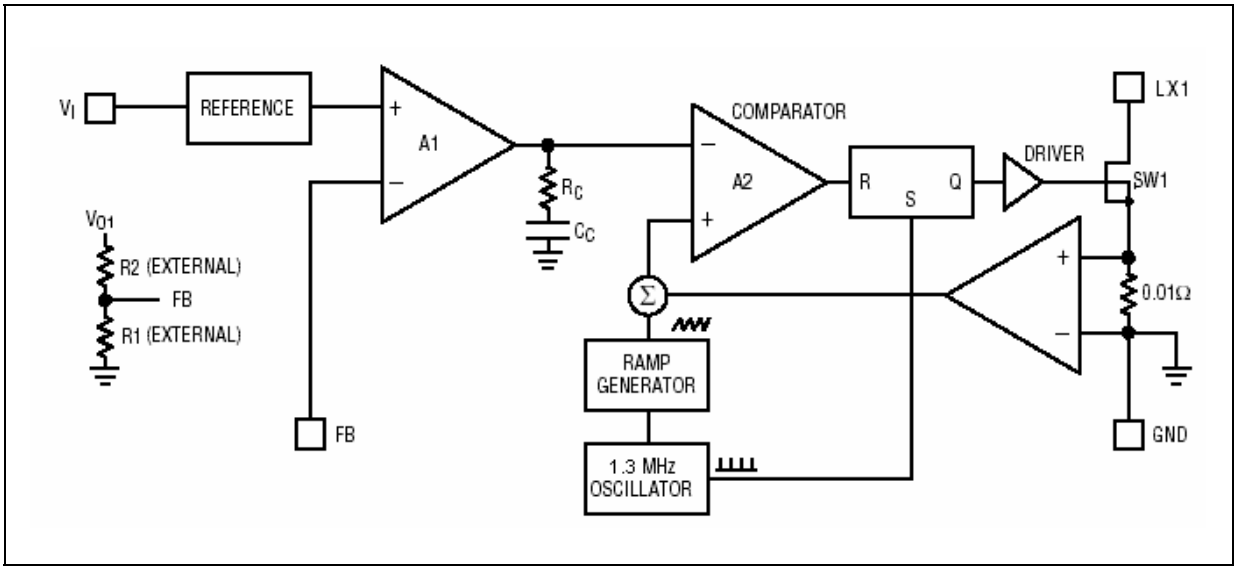
5 Introduction

The STOD1412 is a dual DC-DC converter which produces one positive and one negative output voltage that are each independently regulated and the values of which can be adjusted with external resistors. Each DC-DC converter is able to supply up to 120 mA of current with input voltage ranging from 2.7 V and 5.5 V. The device uses a fixed-frequency PWM controller at 1.3 MHz. This control scheme simplifies noise filtering in sensitive applications and provides excellent line regulation.

The operation of the STOD1412 can be best understood by referring to the block diagram in *Figure 3*, where the step-up control circuit is shown, and a similar scheme is adopted for the inverting section. At the start of each oscillator cycle, the SR latch is set, which turns on power switch SW1. A voltage proportional to the switch current is added to the sawtooth ramp and the resulting sum is fed into the positive terminal of the PWM comparator A2. When this voltage exceeds the level of the negative input of A2, the SR latch is reset, thus turning off the power switch. The voltage level of the negative input of A2 is set by the error amplifier A1, and it is simply an amplified version of the difference between the feedback voltage and the reference voltage. In this manner, the error amplifier sets the correct peak current level necessary to keep the output in regulation. If the error amplifier output increases, more current is delivered to the output; if it decreases, less current is delivered. The device also has a current limit circuit (not shown in Figure 2). The switch current is constantly monitored and not allowed to exceed the preset maximum switch current (IL_1-max, IL_2-max). If the switch current reaches this value, the SR latch is reset regardless of the state of comparator A2. This current limit helps protecting the power switch as well as the external components connected to the device.

The step up converter works in continuous mode detector (CMD) in the entire line and load range, while the inverting converter can work in both discontinuous mode detector (DMD) and CMD.

Figure 3. PWM control scheme



5.1 Setting output voltage

The output voltage can be set using external network resistors.

The positive output voltage range is 4.3 V minimum up to a maximum of 6.0 V. It is obtained by connecting FB1 to OUT1 through R2, and FB1 to PGND through R1 (see application circuit). The positive output value can be calculated using the following formula:

$V_{O1} = (R_1 + R_2)/R_1 \times V_{FB1}$

The negative output voltage range is -8.0 V minimum up to a maximum of -2.0 V. It is obtained connecting FB2 to VREF through R3 and FB2 to PGND through R4 (see application circuit). The value of negative output can be calculated using the following formula:

$V_{O2} = (R_4/R_3) \times V_{REF}$

5.2 Under voltage lockout

The device includes an under voltage lockout circuit. When the STOD1412 is enabled (EN pin is pulled high), the device will be OFF until the input voltage reaches the 2.55 V threshold. The UVLO circuit has a hysteresis of 50 mV, so once the device is on, it will keep working until V_{CC} voltage falls below 2.50 V.

5.3 Enable

This function allows switching ON and OFF the device using a logic level signal. If the EN pin is pulled high the device turns ON, given that the input voltage is higher than the under voltage lockout threshold. Pulling the EN pin low turns off the device regardless of the UVLO state. In this condition the current consumption is reduced to lower than 1 µA

5.4 Load disconnect

When the device is turned OFF, there is no path for the current to flow from the input power supply to the load. In the device there are two switches that allow complete disconnection of the load. This function is useful to improve battery life when the device is not in operation.

5.5 Soft start and inrush current

The device includes a soft start feature to limit inrush current when the device is turned on. This function is added to minimize battery loading at start-up.

5.6 Current limit

The step-up and inverter converters include peak current limit circuitry. The inductor peak current cannot exceed 900mA for the step-up stage and 1A for the inverting stage.

5.7 External components

5.7.1 Inductor

The 1.3 MHz frequency allows the use of small inductors for both converters. In typical applications, a 4.7 µH and a 6.8 µH are recommended for step-up and inverting respectively. Larger values of inductor reduce the ripple inductor current. The inductor's current saturation rating must exceed the peak current.

5.7.2 Capacitors

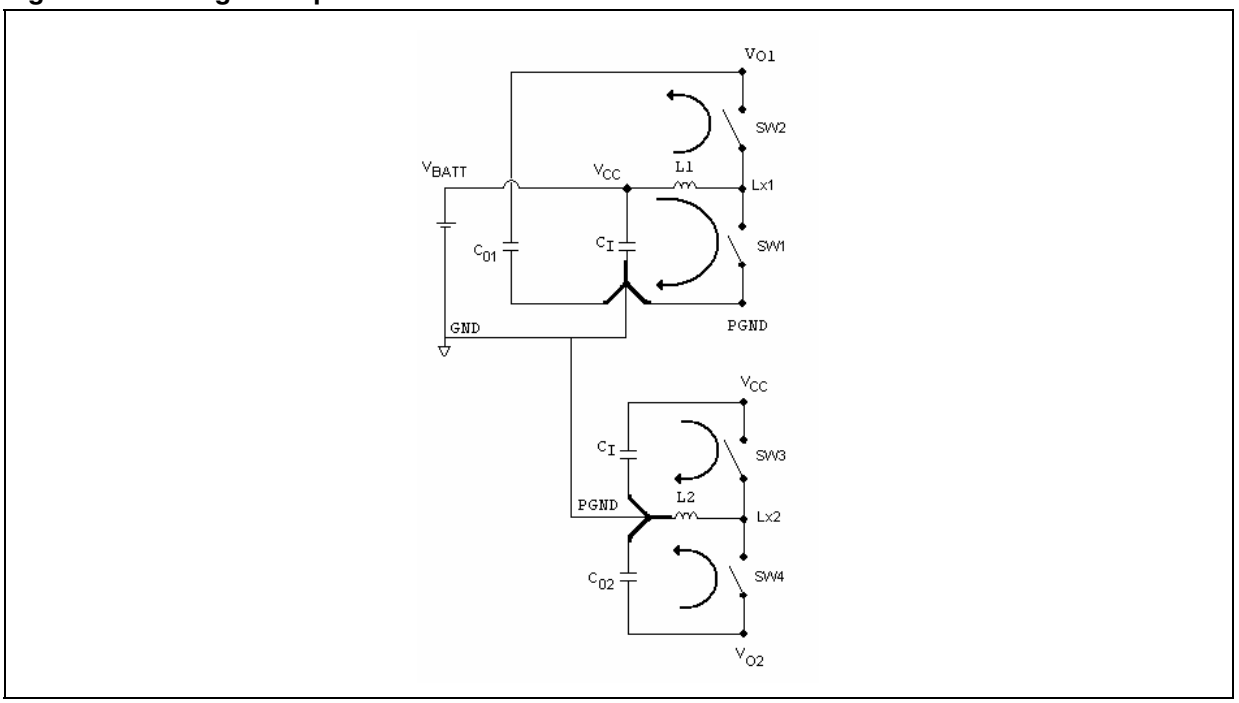
In order to reduce the ripple voltage on the outputs it is recommended to use capacitors with low equivalent series resistance (ESR) on output filters. The interaction between the ESR value of the capacitor and peak inductor current determines the amplitude of the ripple on the output voltage. The suggested value for output capacitors is 4.7 µF.

In order to filter the input voltage variations, a ceramic capacitor must be connected between V_{CC} and PGND. A minimum value of 2.2 µF is recommended. This value may be increased to further reduce the noise coming from input power supply. A 100 nF to 1 µF capacitor on the VREF pin is also recommended.

5.7.3 PCB Layout

Board layout is important due to high current levels and high switching frequency that could radiate noise. It is important to connect the signal GND pin, the input and output capacitor ground leads and power ground to a single connection point to obtain a star ground configuration. This minimizes ground noise and improves regulation. It is useful to minimize lead lengths in order to reduce stray capacitance, trace resistance to avoid voltage drops and noise irradiation, especially to the feedback circuit, ground circuit and LX_ traces. Place feedback resistors close to their respective feedback pins. Place input capacitors as close as possible to V_{CC} and PGND.

Figure 4. Star ground plane



6 Typical application

Figure 5. Typical application circuit

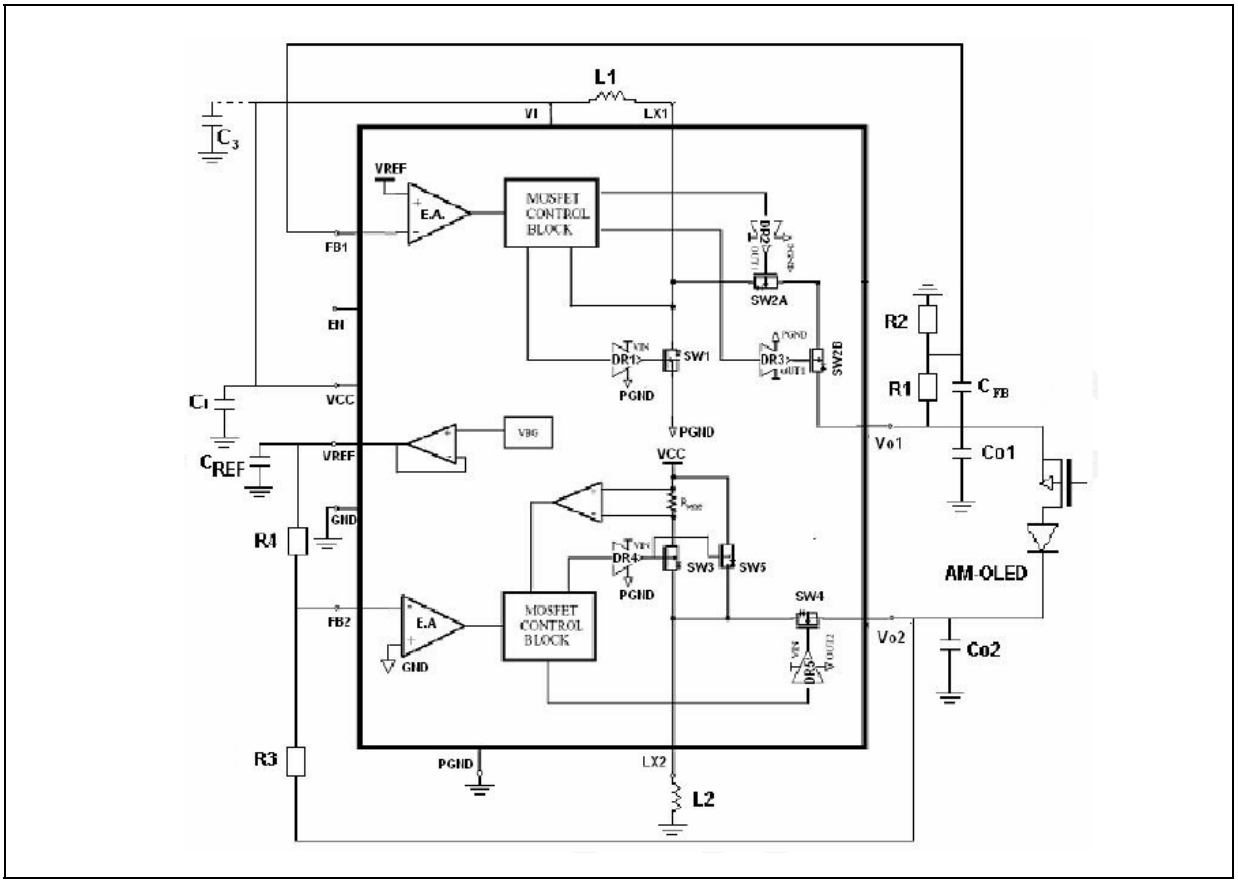


Table 6. External components (see *Figure 5.*)

Symbol	Parameter	Min	Typ.	Max	Unit
L_1	Inductor		4.7		µH
L_2	Inductor		6.8		µH
C_I	Ceramic capacitor SMD		2.2		µF
C_3	Ceramic capacitor SMD – OPTIONAL		1		µF
$C_{01,2}$	Ceramic capacitor SMD		4.7		µF
C_{Fb}	Ceramic capacitor SMD		22		nF
C_{REF}	Ceramic capacitor SMD		1		µF
R1	Feedback resistors		470		kΩ
R2	Feedback resistors		166		kΩ
R3	Feedback resistor		533		kΩ
R4	Feedback resistor		100		kΩ

7 Typical performance characteristics

Figure 6. System efficiency vs. output current

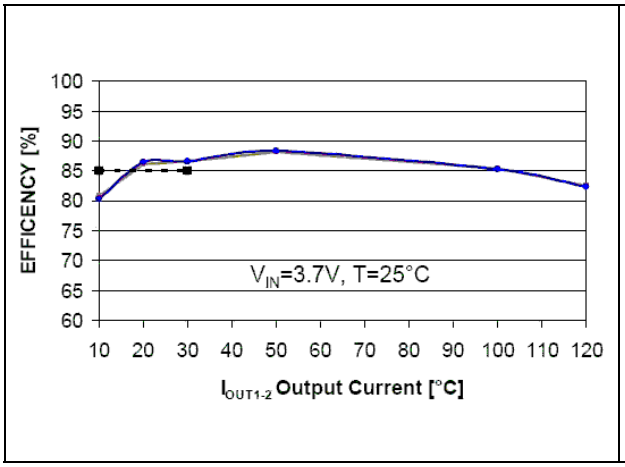


Figure 7. I_{PK} current step-up vs. input voltage

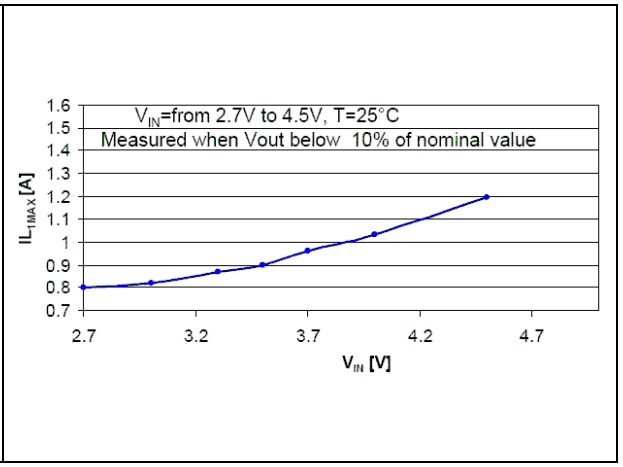


Figure 8. I_{PK} current inverting vs. input voltage

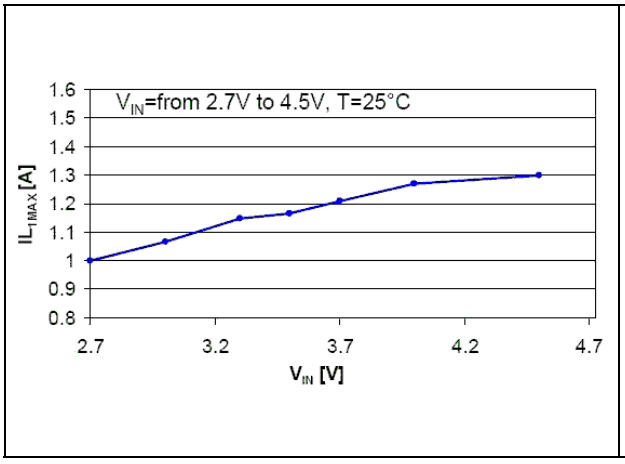


Figure 9. Voltage reference vs. temperature

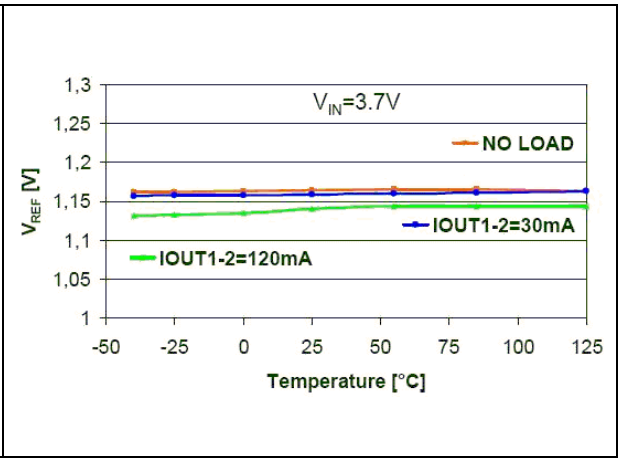


Figure 10. V_{FB1} on step-up vs. temperature

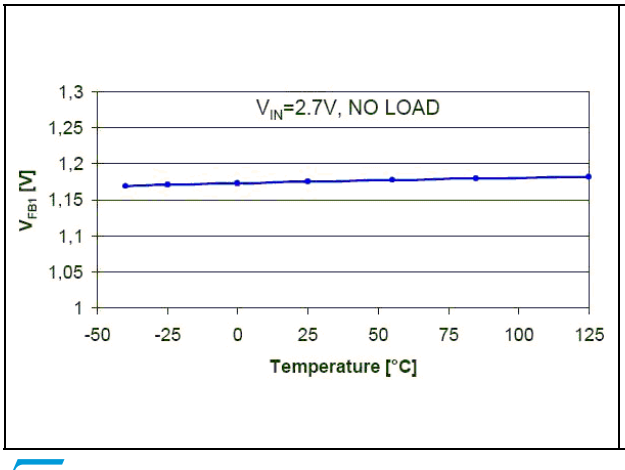


Figure 11. Line V_{FB1} on step-up vs. temperature

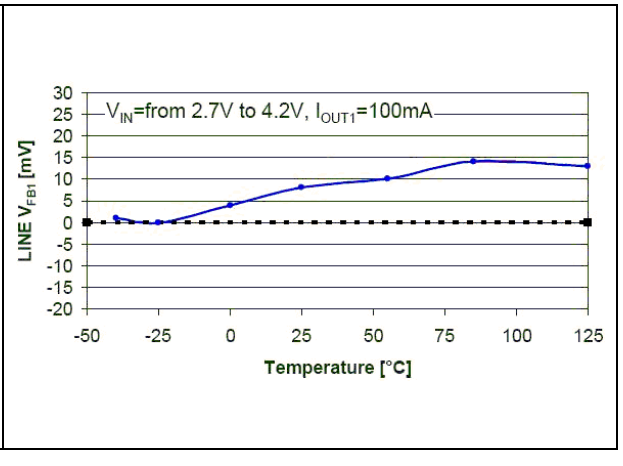


Figure 12. V_{FB2} on inverting vs. temperature

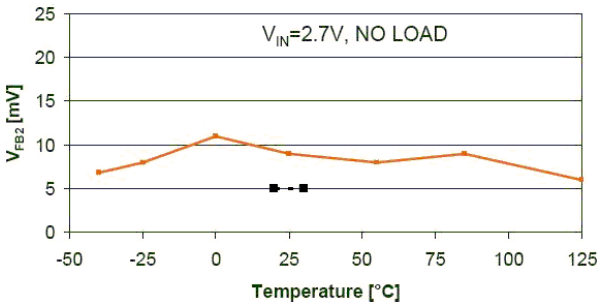


Figure 13. Line V_{FB2} on inverting vs. temperature

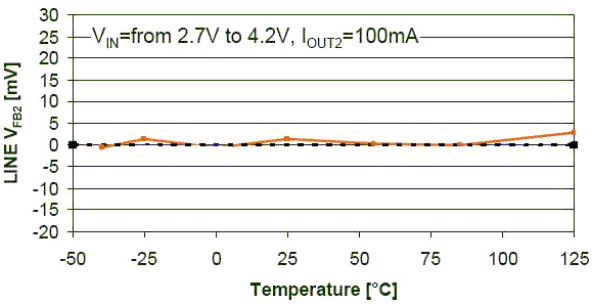
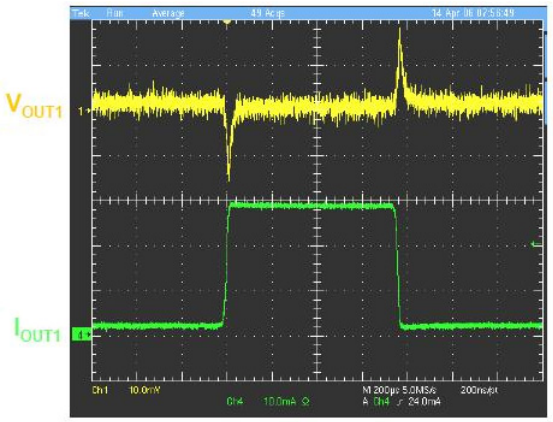
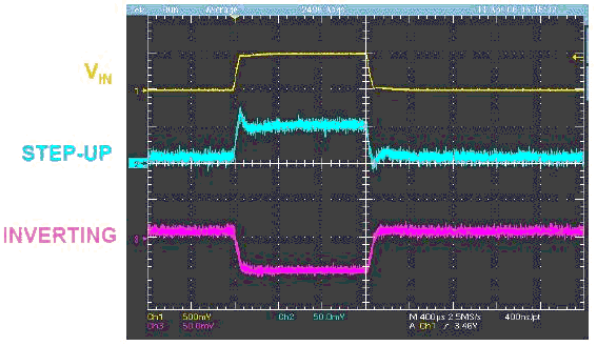


Figure 14. Load transient response (step-up)



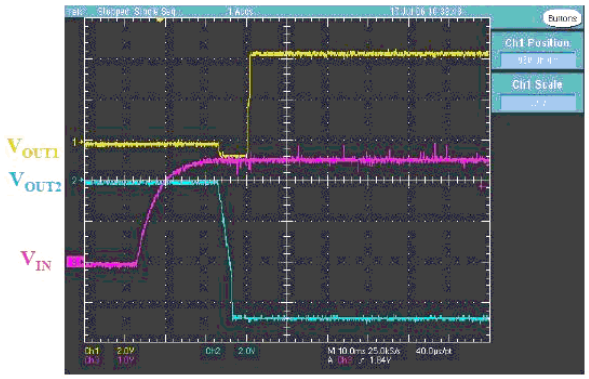
V_{IN}=3.7V, I_{OUT}=3mA to 30mA, T_{RISE}=T_{FALL}=30µs, T=25°C

Figure 15. Line transient response



V_{IN}=3V to 3.5V, $I_{OUT1,2}$ = 120mA, T_{RISE}=T_{FALL}=50µs, T=25°C

Figure 16. Start-up voltage



V_{IN}=0V to 2.5V, T=25°C

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 17. QFN16L package outline

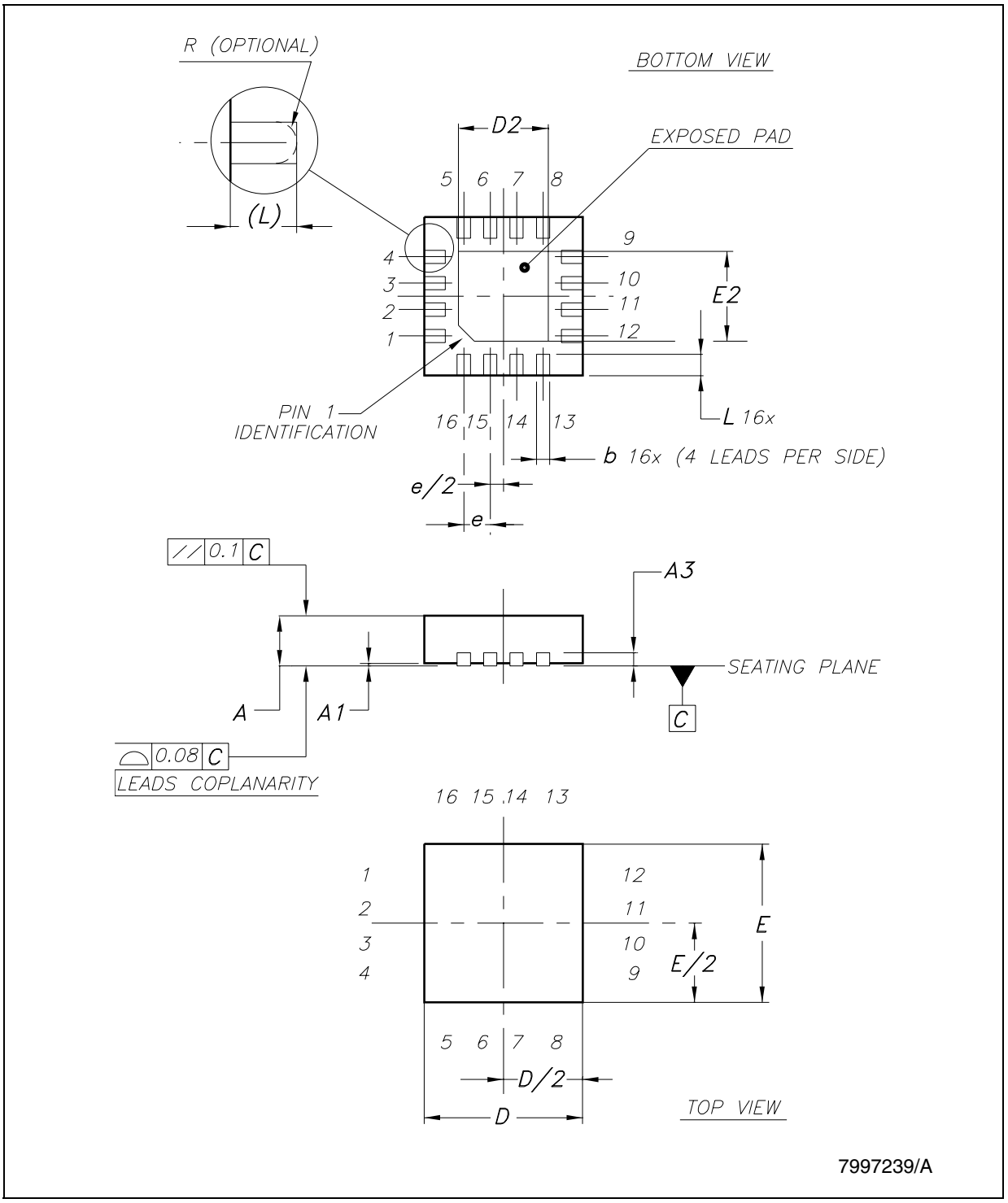


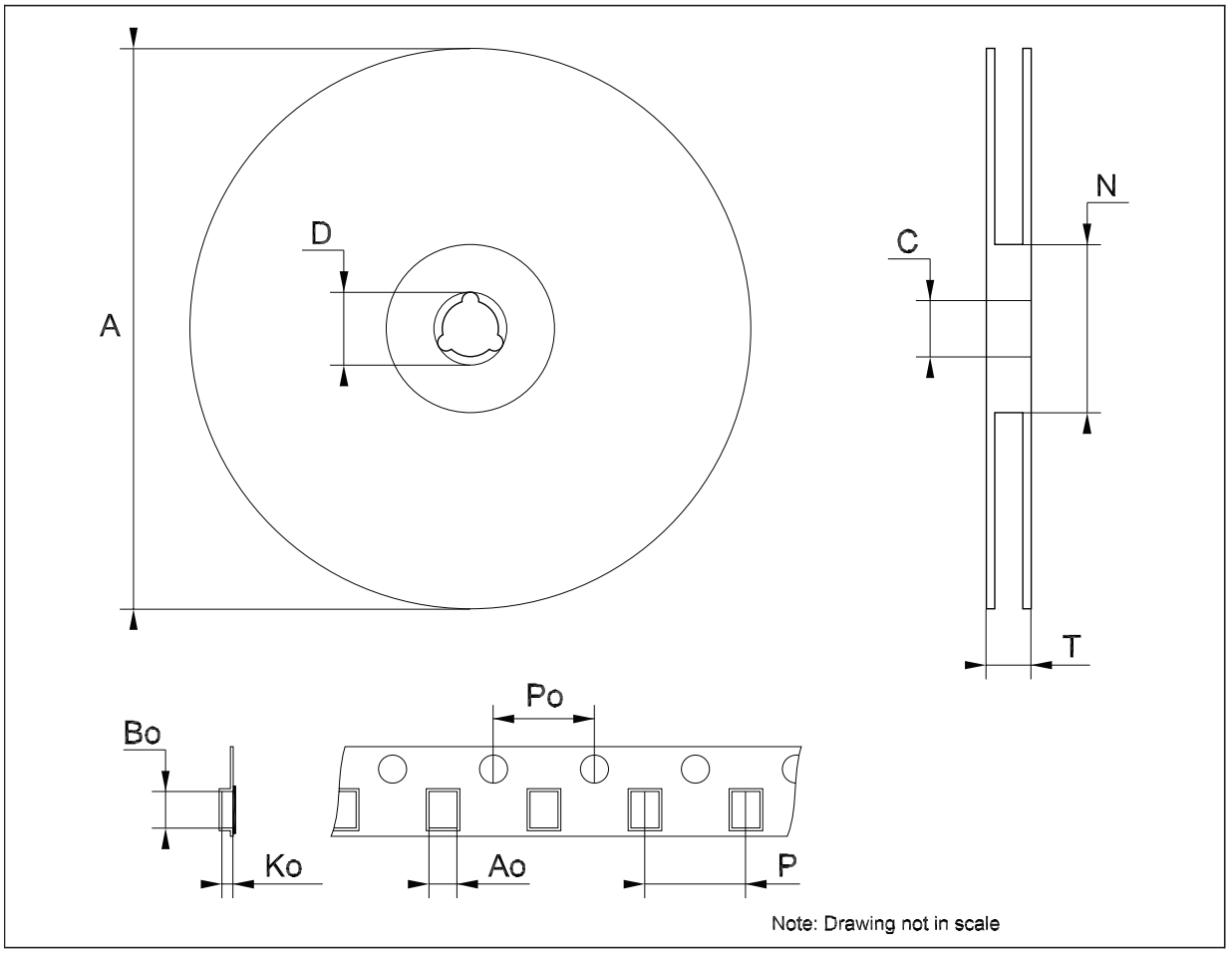
Table 7. QFN16L mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	2.90	3	3.10	0.114	0.118	0.122
D2	1.50	1.70	1.80	0.059	0.067	0.071
E	2.90	3	3.10	0.114	0.118	0.122
E2	1.50	1.70	1.80	0.059	0.067	0.071
e		0.50			0.020	
L (1)	0.30	0.40	0.50	0.012	0.016	0.020

1. The value of "L" a JEDEC norm is MIN 0.35 - MAX 0.45.

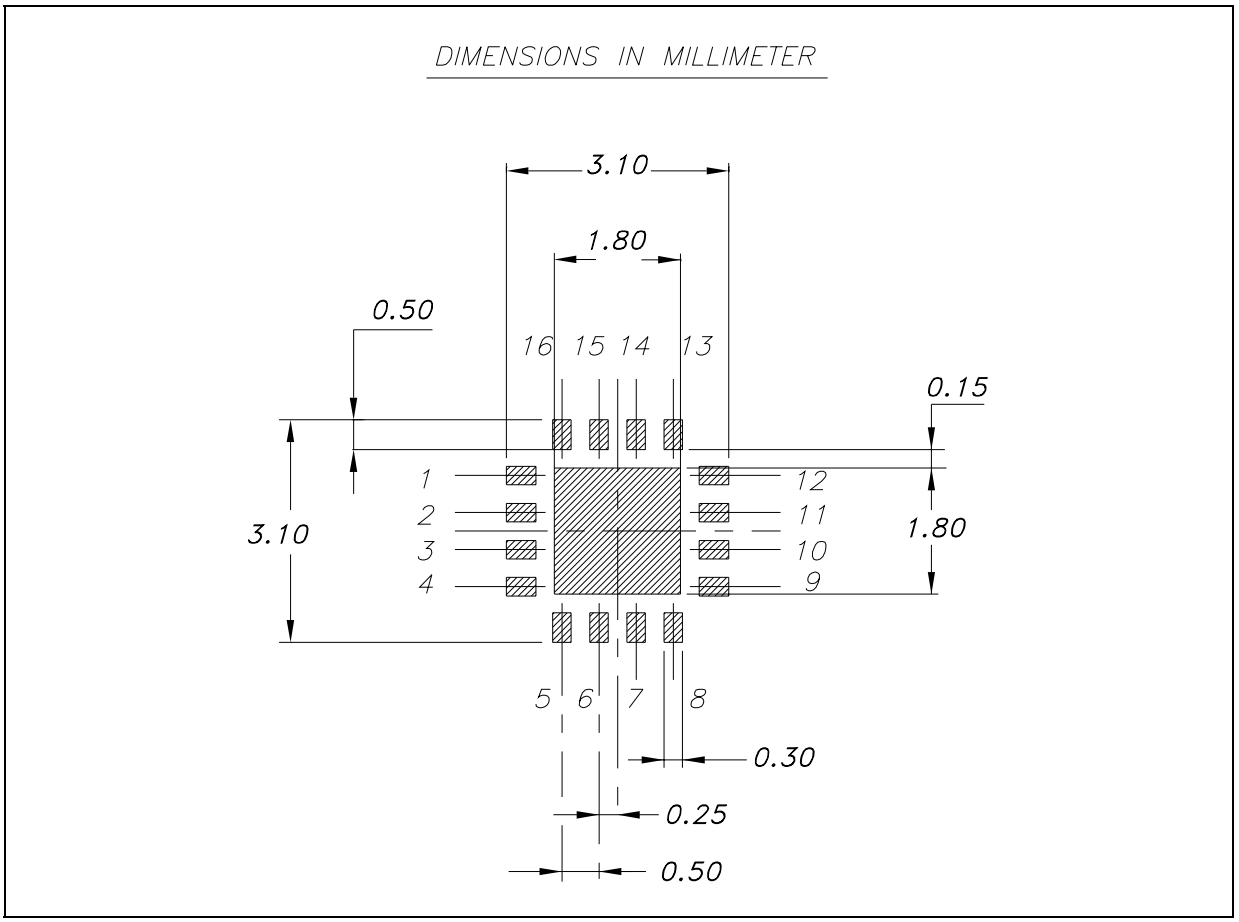
Tape & reel QFNxx/DFNxx (3x3) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.087
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

Figure 18. QFN16L footprint - recommended data



9 Revision history

Table 8. Document revision history

Date	Revision	Changes
31-Aug-2007	1	Initial release.

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