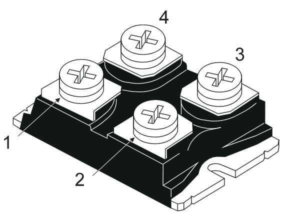
STGE50NC60VD

N-channel 50A - 600V - ISOTOP
Very fast PowerMESH™ IGBT

Features

Type	V_{CES}	$V_{CE(sat)}$ (Max) @25°C	I_C @100°C
STGE50NC60VD	600V	2.5V	50A

- High current capability
- High frequency operation
- Low C_{RES}/C_{IES} ratio (no cross-conduction susceptibility
- Very soft ultra fast recovery antiparallel diode



ISOTOP

Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "V" identifies a family optimized for high frequency.

Applications

- High frequency inverters
- SMPS and PFC in both hard switching and resonant topologies
- UPS
- Motor drivers

Figure 1. Internal schematic diagram

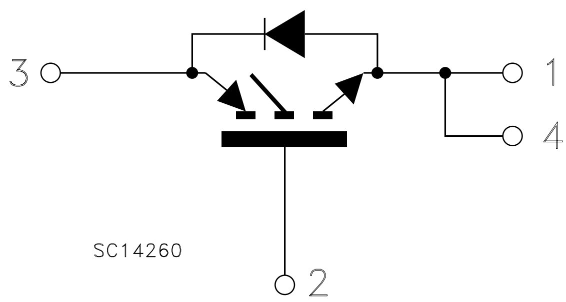


Table 1. Device summary

Order code	Marking	Package	Packaging
STGE50NC60VD	GE50NC60VD	ISOTOP	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GS} = 0)	600	V
I_C (1)	Collector current (continuous) at T_C = 25°C	80	A
I_C (1)	Collector current (continuous) at T_C = 100°C	50	A
I_{CL} (2)	Collector current (pulsed)	200	A
V_{GE}	Gate-emitter voltage	± 20	V
I_F	Diode RMS forward current at Tc=25°C	30	A
P_{TOT}	Total dissipation at T_C = 25°C	260	W
T_{stg}	Storage temperature	-55 to 150	°C
Tj	Operating junction temperature		

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Pulse width limited by Tjmax

Table 3. Thermal resistance

Symbol	Parameter	Min	Typ	Max	Unit
Rthj-case	Thermal resistance junction-case (IGBT)	--	--	0.48	°C/W
Rthj-case	Thermal resistance junction-case (diode)	--	--	1.5	°C/W
Rthj-amb	Thermal resistance junction-amb	--	--	50	°C/W

2 Electrical characteristics

(T_J = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	I_C= 1mA, V_{GE}= 0	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE}= 15V, I_C= 40A V_{GE}= 15V, I_C=40A,Tc=125°C		1.9 1.7	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	V_{CE}= V_{GE}, I_C= 250 µA	3.75		5.75	V
I_{CES}	Collector cut-off current (V_{GE} = 0)	V_{CE}= Max rating,T_C= 25°C V_{CE}= Max rating,T_C= 125°C			150 1	µA mA
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE}= ±20V, V_{CE}= 0			±100	nA
g_{fs}	Forward transconductance	V_{CE} = 15V, I_C= 20A		20		S

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	V_{CE} = 25V, f = 1MHz, V_{GE} = 0		4550 350 105		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 390V, I_C = 40A, V_{GE} = 15V, *Figure 17*		214 30 96		nC nC nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390V, I_C = 40A R_G= 3.3Ω, V_{GE}= 15V, *Figure 16*		43 17 2060		ns ns A/µs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390V, I_C = 40A R_G= 3.3Ω, V_{GE}= 15V, Tj = 125°C *Figure 16*		42 19 1900		ns ns A/µs
$t_{r(Voff)}$ $t_{d(Voff)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 390V, I_C = 40A R_G= 3.3Ω, V_{GE}= 15V, *Figure 16*		25 140 45		ns ns ns
$t_{r(Voff)}$ $t_{d(Voff)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 390V, I_C = 40A R_G= 3.3Ω, V_{GE}= 15V, Tj = 125°C *Figure 16*		60 170 77		ns ns ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}(1) E_{off}(2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 40A R_G= 3.3Ω, V_{GE}= 15V, *Figure 18*		330 720 1050	450 970 1420	µJ µJ µJ
E_{on}(1) E_{off}(2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 40A R_G= 3.3Ω, V_{GE}= 15V, Tj = 125°C *Figure 18*		640 1400 2040		µJ µJ µJ

1. Eon is the turn-on losses when a typical diode is used in the test circuit in *Figure 18* If the IGBT is offered in a package with a co-pak diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)
2. Turn-off losses include also the tail of the collector current

Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_f	Forward on-voltage	I_f = 20A I_f = 20A, Tj = 125°C		1.5 1	2.2	V V
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_f = 20A,V_R = 40V, Tj = 25°C, di/dt = 100 A/µs *Figure 19*		44 66 3		ns nC A
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_f = 20A,V_R = 40V, Tj =125°C, di/dt = 100A/µs *Figure 19*		88 237 5.4		ns nC A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

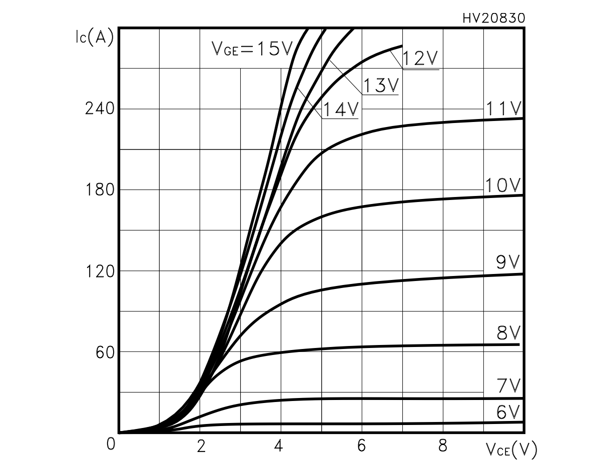


Figure 3. Transfer characteristics

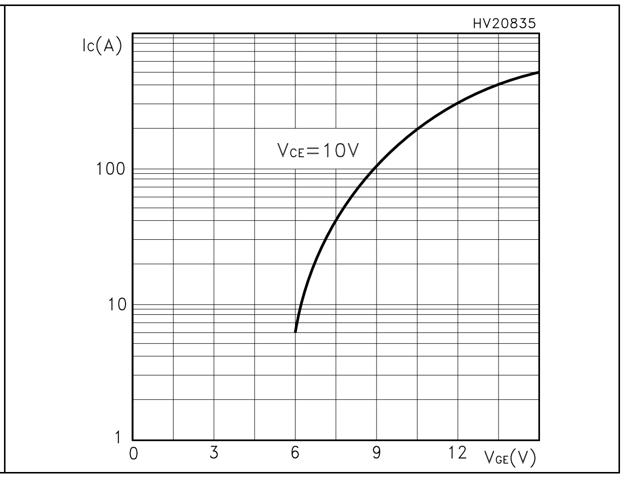


Figure 4. Transconductance

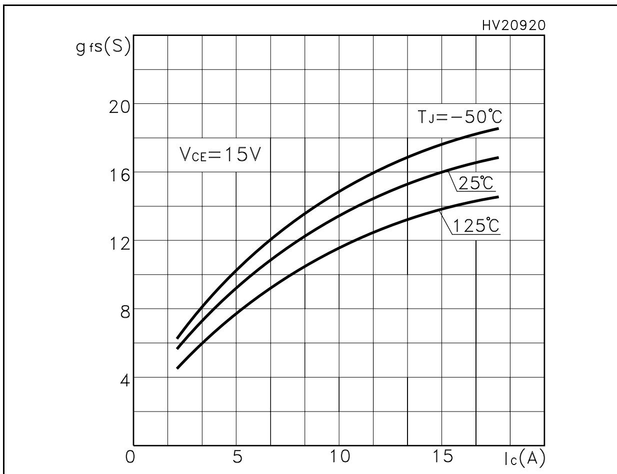


Figure 5. Collector-emitter on voltage vs temperature

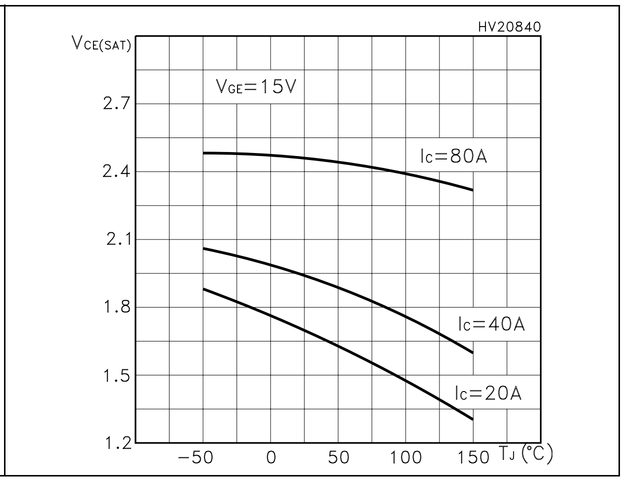


Figure 6. Collector-emitter on voltage vs collector current

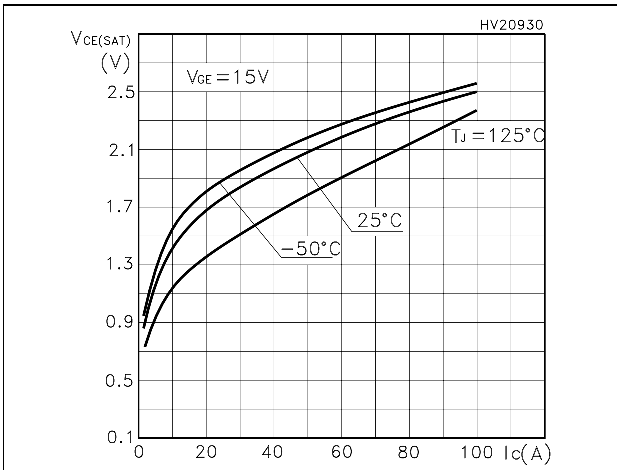


Figure 7. Normalized gate threshold vs temperature

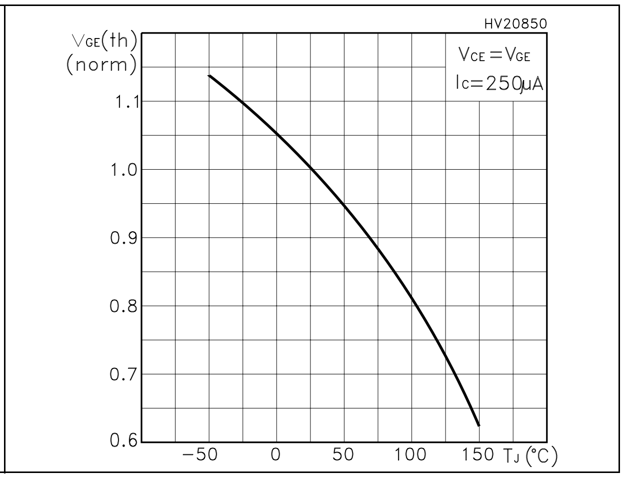


Figure 8. Normalized breakdown voltage vs temperature

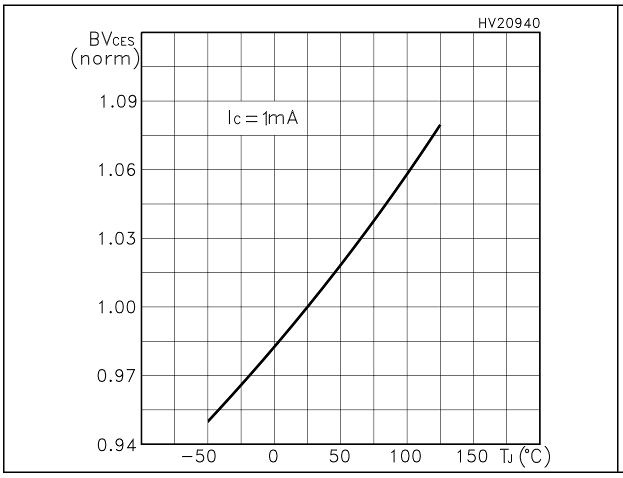


Figure 9. Gate charge vs gate-emitter voltage

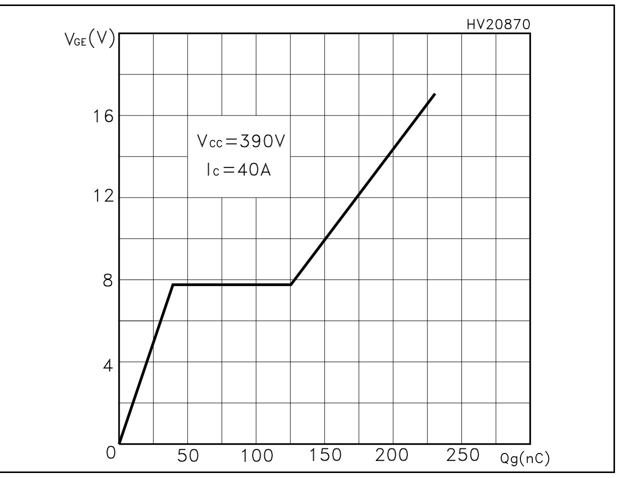


Figure 10. Capacitance variations

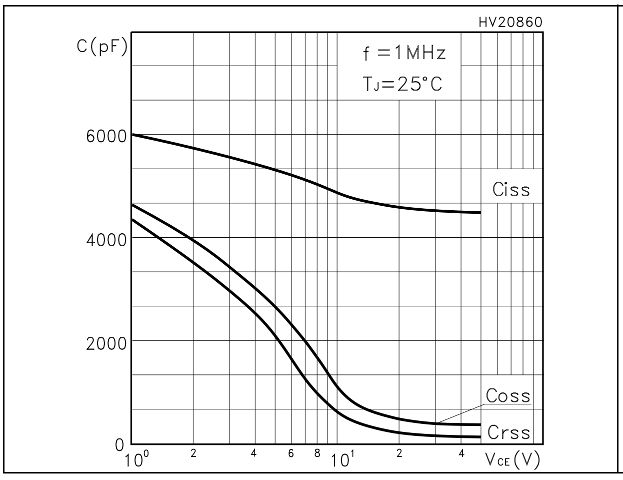


Figure 11. Total switching losses vs temperature

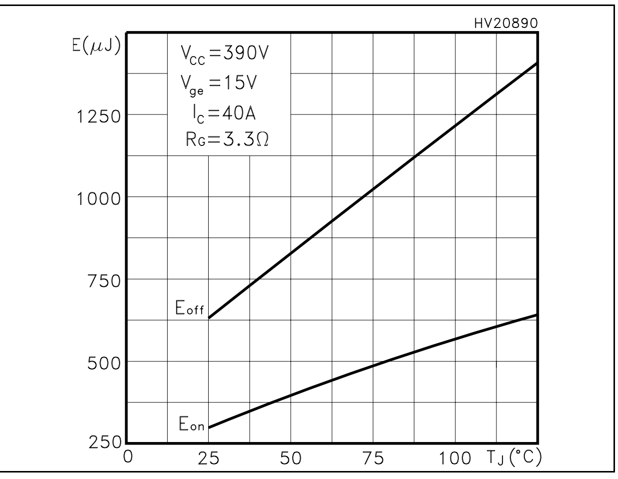


Figure 12. Total switching losses vs gate charge resistance

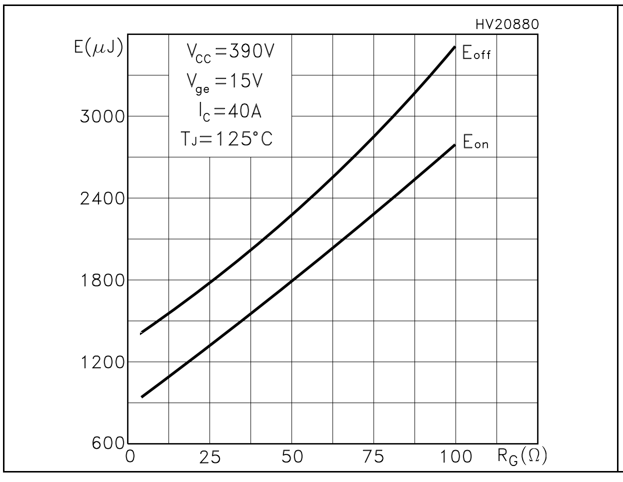


Figure 13. Total switching losses vs collector current

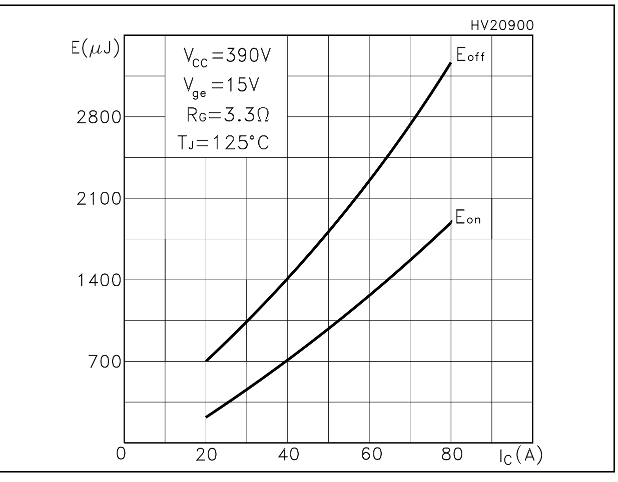


Figure 14. Turn-off SOA

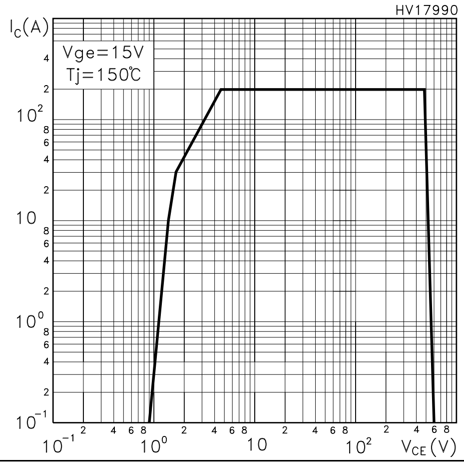
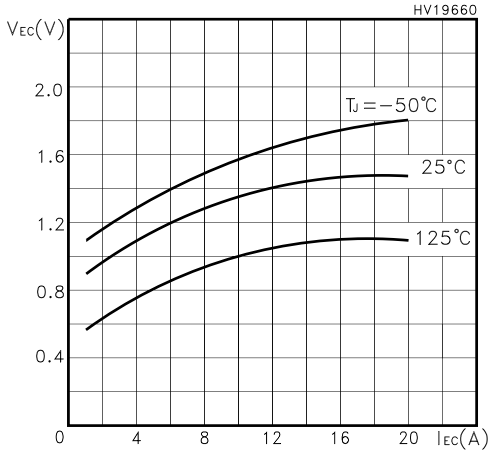


Figure 15. Emitter-collector diode characteristics



3 Test circuit

Figure 16. Test circuit for inductive load switching

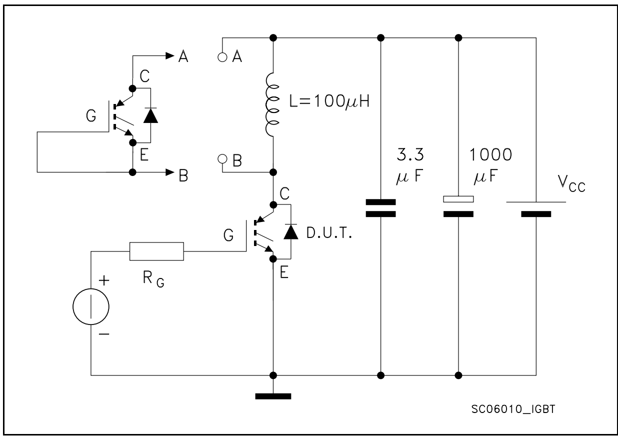


Figure 17. Gate charge test circuit

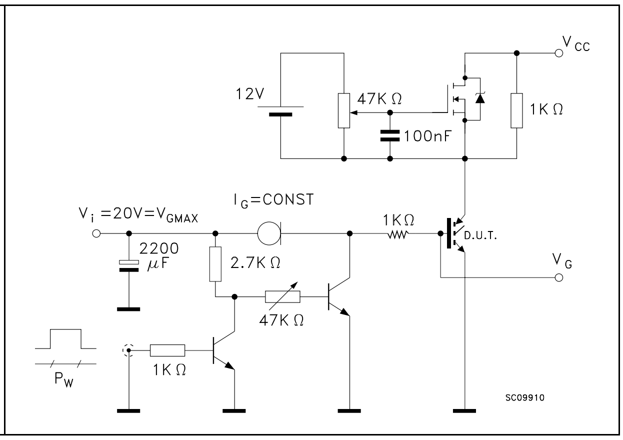


Figure 18. Switching waveform

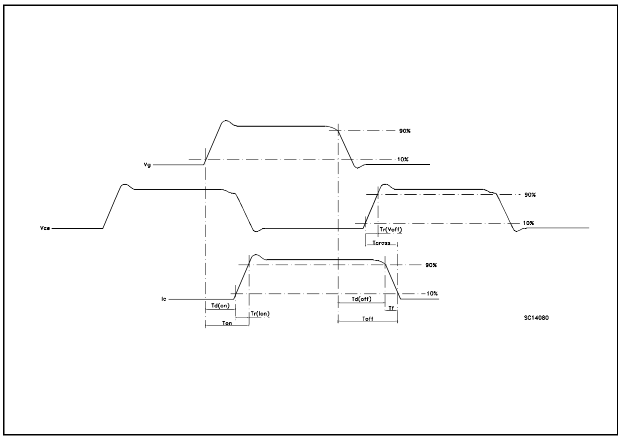
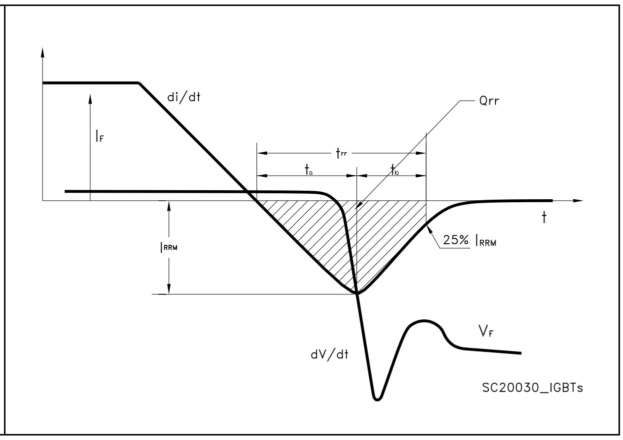


Figure 19. Diode recovery time waveform

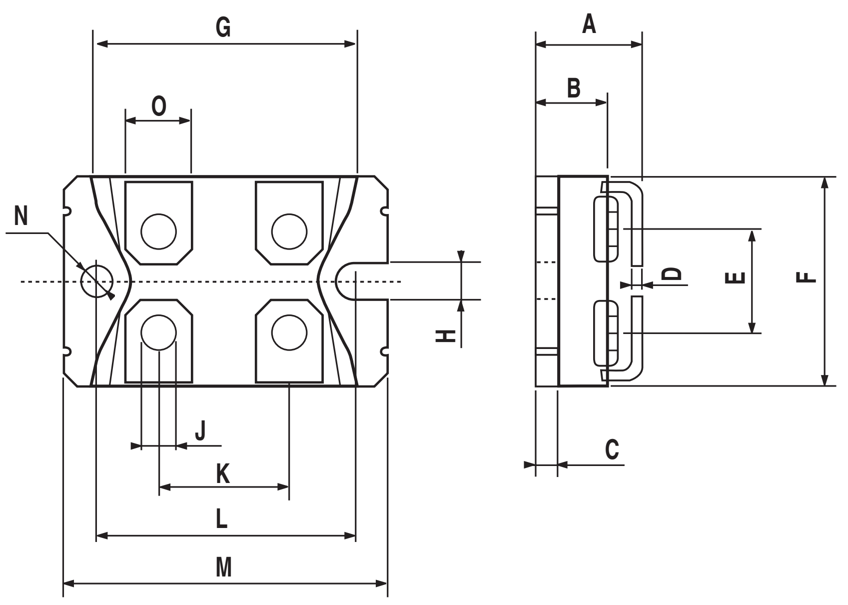


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



5 Revision History

Table 9. Revision history

Date	Revision	Changes
11-Oct-2006	1	First release
24-Jul-2007	2	Internal schematic diagram has been updated *Figure 1*