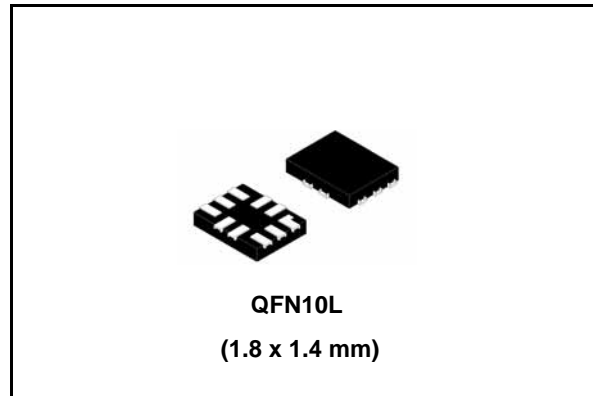


Low voltage 0.5 Ω max dual SPDT switch with break-before-make

Features

- Ultra low power dissipation:
 $I_{CC} = 0.2 \mu A$ (max.) at $T_A = 85^\circ C$
- Low ON resistance:
 - $R_{ON} = 0.50 \Omega$ (max. $T_A = 25^\circ C$) at $V_{CC} = 4.3 V$
 - $R_{ON} = 0.55 \Omega$ (max. $T_A = 25^\circ C$) at $V_{CC} = 3.6 V$
 - $R_{ON} = 0.55 \Omega$ (max. $T_A = 25^\circ C$) at $V_{CC} = 3.0 V$
- Wide operating voltage range:
 V_{CC} (opr) = 1.65 V to 4.3 V single supply
- 5 V tolerant and 1.8 V compatible threshold on digital control input at $V_{CC} = 1.65$ to 4.3 V
- Latch-up performance exceeds 300 mA (JESD 17)
- ESD performance:
HMB > 2 kV (MIL STD 883 method 3015)



exists between the two ports) when nIN is held low. The switches $nS2$ are ON (connected to common ports Dn) when the nIN input is held low and OFF (high impedance state exists between the two ports) when IN is held high. Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage immunity.

Description

The STG5223 is a high-speed CMOS dual analog SPDT (single pole dual throw) switch or dual 2:1 multiplexer/demultiplexer bus switch fabricated in silicon gate C²MOS technology. It is designed to operate from 1.65 to 4.3 V, making this device ideal for portable applications.

It offers very low ON resistance (<0.5 Ω) at $V_{CC} = 3.0 V$. The nIN inputs are provided to control the switches. The switches $nS1$ are ON (connected to common ports Dn) when the nIN input is held high and OFF (high impedance state

Table 1. Device summary

Order code	Package	Packaging
STG5223QTR	QFN10L (1.8 x 1.4 mm)	Tape and reel

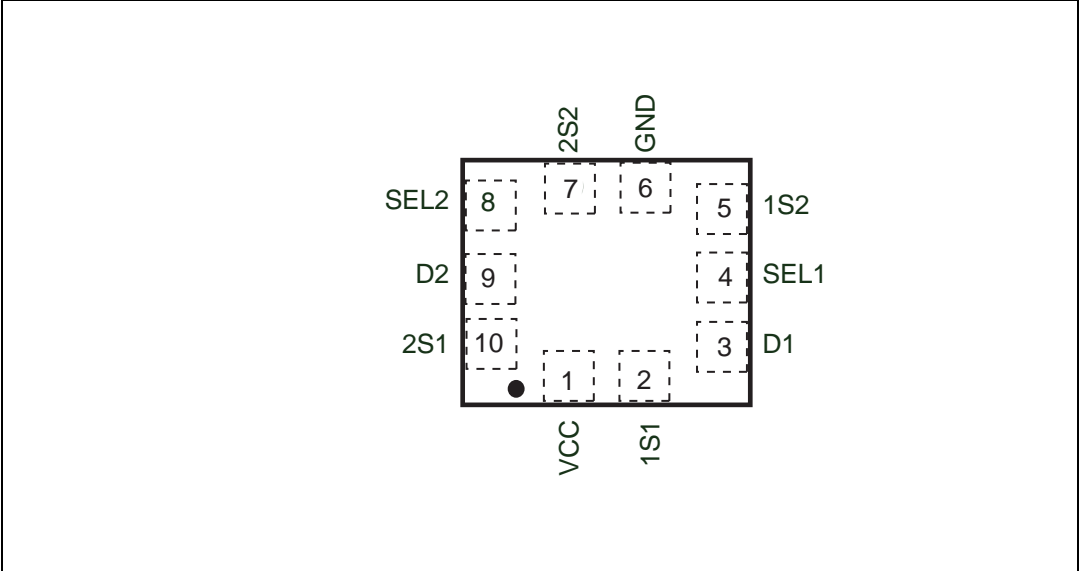
Contents

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1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (top through view)



1.2 Pin description

Table 2. Pin description

Pin number	Symbol	Name and function
1	V _{CC}	Positive supply voltage
2,	1S1 to 2S1 1S2 to 2S2	Independent channels
3	D1, D2	Common channels
4	SEL1, SEL2	Controls
5	1S1 to 2S1 1S2 to 2S2	Independent channels
6	GND	Ground (0V)
7	1S1 to 2S1 1S2 to 2S2	Independent channels
8	SEL1, SEL2	Controls
9	D1, D2	Common channels
10,	SEL1, SEL2	Controls

1. Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground.

2 Input equivalent circuit and truth table

Figure 2. Input equivalent circuit

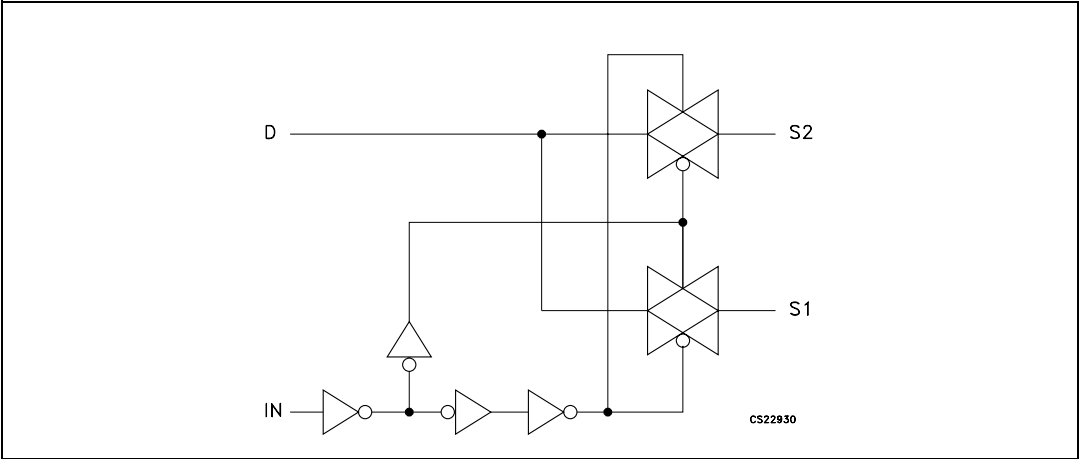


Table 3. Truth table

IN	Switch S1	Switch S2
H	ON	OFF ⁽¹⁾
L	OFF ⁽¹⁾	ON

1. High impedance

3 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IKC}	DC input diode current on control pin ($V_{SEL} < 0$ V)	-50	mA
I_{IK}	DC input diode current ($V_{IN} < 0$ V)	± 50	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 300	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	± 500	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 100	mA
P_D	Power dissipation at $T_A=70$ °C ⁽¹⁾	1120	mW
T_{STG}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	300	°C

1. Derate above 70 °C by 18.5 mW/ °C

3.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.3	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.3	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0 to 20	ns/V
		$V_{CC} = 3.0\text{ V to }4.3\text{ V}$	0 to 10	

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V _{CC} (V)	Test condition	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
V _{IH}	High level input voltage	1.65 – 1.95		0.65 V _{CC}			0.65 V _{CC}		V
		2.3 – 2.5		1.2			1.2		
		2.7 – 3.0		1.3			1.3		
		3.0 – 3.6		1.4			1.4		
		4.3		1.5			1.5		
V _{IL}	Low level input voltage	1.65 – 1.95				0.25		0.25	V
		2.3 – 2.5				0.25		0.25	
		2.7 – 3.0				0.25		0.25	
		3.0 – 3.6				0.30		0.30	
		4.3				0.40		0.40	
R _{ON}	Switch ON resistance	4.3	V _S = 0 V to V _{CC} I _S = 100 mA		0.45	0.50		0.55	Ω
		3.6			0.50	0.55		0.65	
		3.0			0.50	0.55		0.65	
		2.3			0.60	0.70		0.80	
		1.8			0.90	1.0		1.1	
ΔR _{ON}	ON resistance match between channels ⁽¹⁾	2.3	V _S = 0 V to V _{CC} I _S = 100 mA		0.1				Ω
R _{FLAT}	ON resistance flatness ⁽²⁾	4.3	V _S = 0 V to V _{CC} I _S = 100 mA		0.15	0.20		0.20	Ω
		3.6			0.15	0.20		0.20	
		3.0			0.15	0.20		0.20	
		2.3			0.20	0.25		0.25	
		1.8			0.35	0.45		0.45	
I _{OFF}	OFF state leakage current (nSn), (Dn)	4.3	V _S = 0.3 or 4 V			±20		±100	nA
I _{IN}	Input leakage current	0 – 4.3	V _{SEL} = 0 to 4.3 V			±0.05		±1	μA
I _{CC}	Quiescent supply current	1.65 – 4.3	V _{SEL} = V _{CC} or GND			±0.05		±0.2	μA

Table 6. DC specifications

Symbol	Parameter	V _{CC} (V)	Test condition	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
I _{CCLV}	Quiescent supply current low voltage driving	4.3	V _{1IN} , V _{2IN} = 1.65 V		±37	±50		±100	μA
			V _{1IN} , V _{2IN} = 1.80 V		±33	±40		±50	
			V _{1IN} , V _{2IN} = 2.60 V		±12	±20		±30	

1. $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$.

2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, t_r = t_f ≤ 5 ns)

Symbol	Parameter	V _{CC} (V)	Test condition	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation delay	1.65 —1.95			0.30				ns
		2.3 —2.7			0.25				
		3.0 —3.3			0.20				
		3.6 —4.3			0.20				
t _{ON}	Turn-ON time	1.65 —1.95	V _S = 0.8 V		120				ns
		2.3 —2.7	V _S = 1.5 V		65	85		90	
		3.0 —3.3			42	55		65	
		3.6 —4.3			40	55		65	
t _{OFF}	Turn-OFF time	1.65 —1.95	V _S = 0.8 V		45				ns
		2.3 —2.7	V _S = 1.5 V		18	30		40	
		3.0 —3.3			16	30		40	
		3.6 —4.3			15	30		40	
t _D	Break-before- make time delay	1.65 —1.95	C _L = 35 pF R _L = 50 Ω V _S = 1.5 V	2	17				ns
		2.3 —2.7		2	10				
		3.0 —3.3		2	8				
		3.6 —4.3		2	7				

Table 7. AC electrical characteristics ($C_L = 35 \text{ pF}$, $R_L = 50 \Omega$, $t_r = t_f \leq 5 \text{ ns}$)

Symbol	Parameter	V _{CC} (V)	Test condition	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
Q	Charge injection	1.65 —1.95	C _L = 100 pF R _L = 1 MΩ V _{GEN} = 0 V R _{GEN} = 0 Ω		43				pC
		2.3 —2.7			51				
		3.0 —3.3			51				
		3.6 —4.3			49				

Table 8. Analog switch characteristics ($C_L = 5 \text{ pF}$, $R_L = 50 \Omega$, $T_A = 25 \text{ }^\circ\text{C}$)

Symbol	Parameter	V _{CC} (V)	Test condition	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
OIRR	Off isolation ⁽¹⁾	1.65 —4.3	V _S = 1 V _{RMS} f = 100 kHz		-66				dB
Xtalk	Crosstalk	1.65 —4.3	V _S = 1 V _{RMS} f = 100 kHz		-72				dB
THD	Total harmonic distortion	2.3 —4.3	R _L = 600 Ω V _{SEL} = 2 V _{PP} f = 20 Hz to 20 kHz		0.02				%
BW	-3dB bandwidth	1.65 —4.3	R _L = 50 Ω		55				MHz
C _{IN}	Control pin input capacitance				7				pF
C _{ON}	Sn port capacitance when switch is enabled	3.3	f = 1 MHz		114				
C _{OFF}	Sn port capacitance when switch is disabled	3.3	f = 1 MHz		40				
C _D	D port capacitance when the switch is enabled	3.3	f = 1 MHz		114				

1. Off isolation = $20 \text{ Log}_{10} (V_D/V_S)$, V_D = output. V_S = input at off switch

5 Test circuit

Figure 3. ON resistance

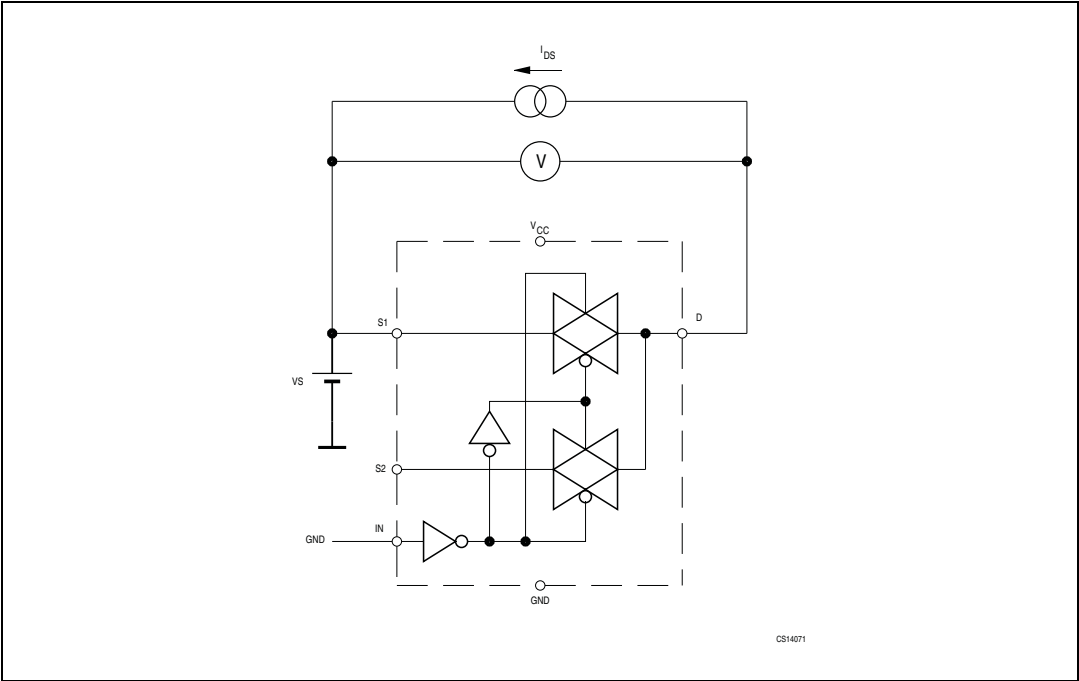


Figure 4. OFF leakage

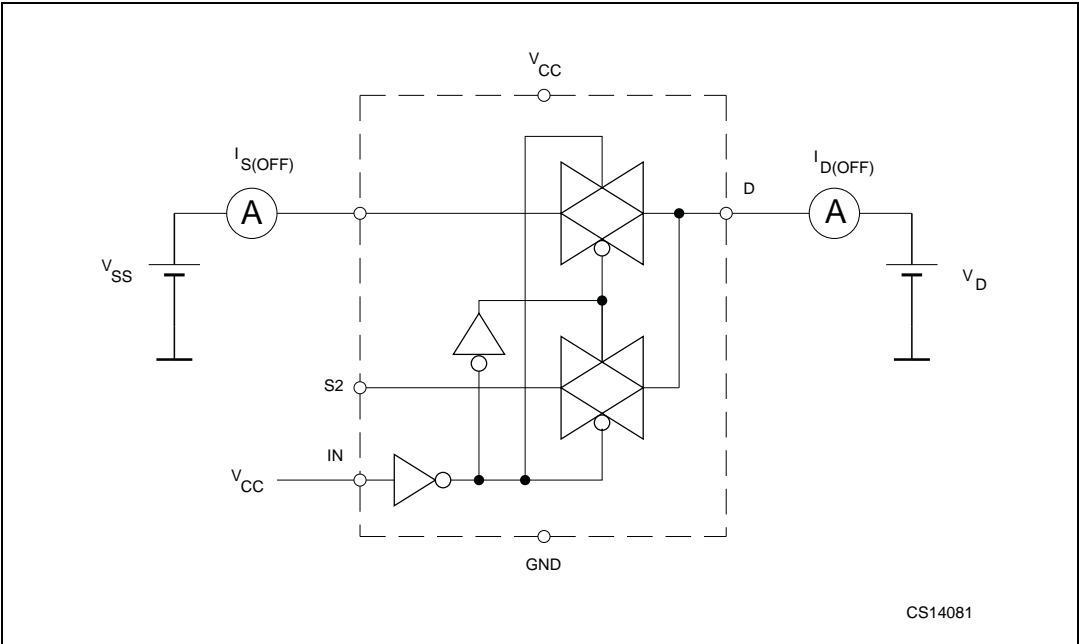


Figure 5. OFF isolation

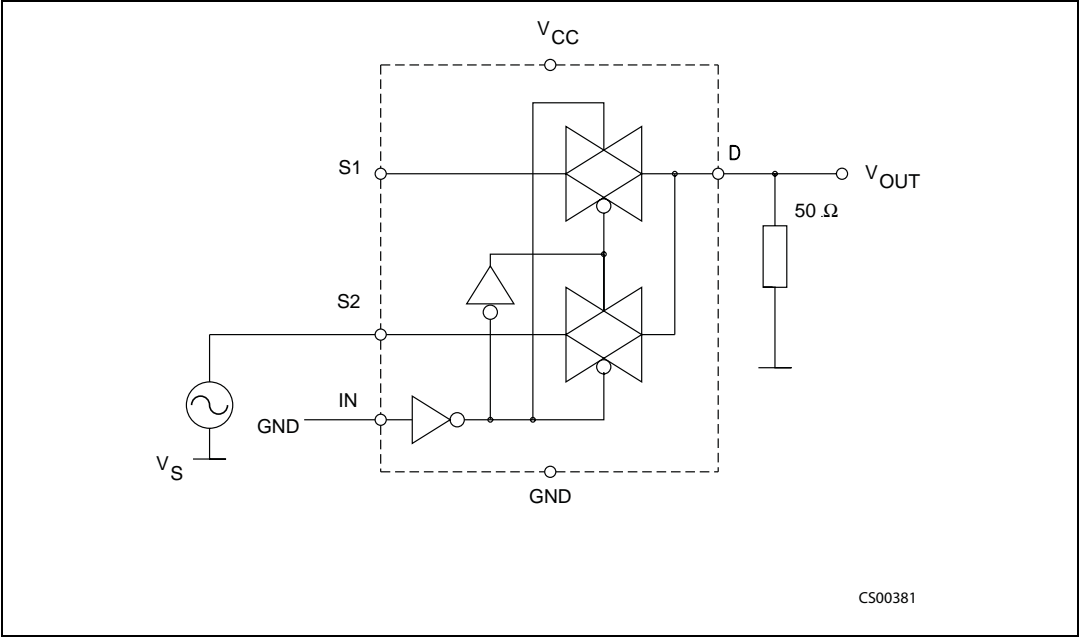


Figure 6. Bandwidth

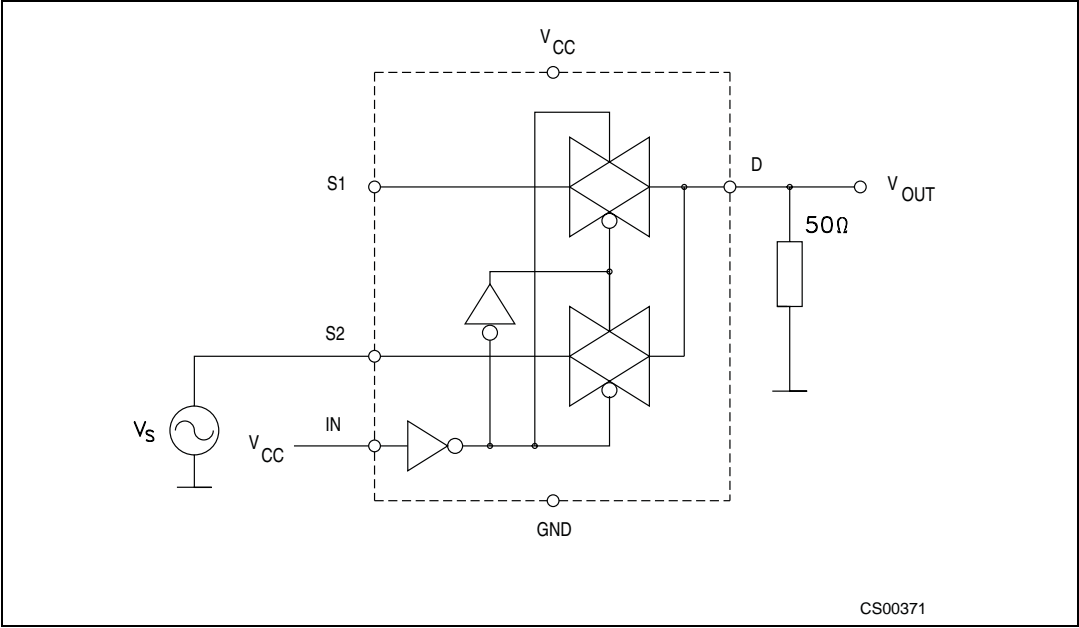
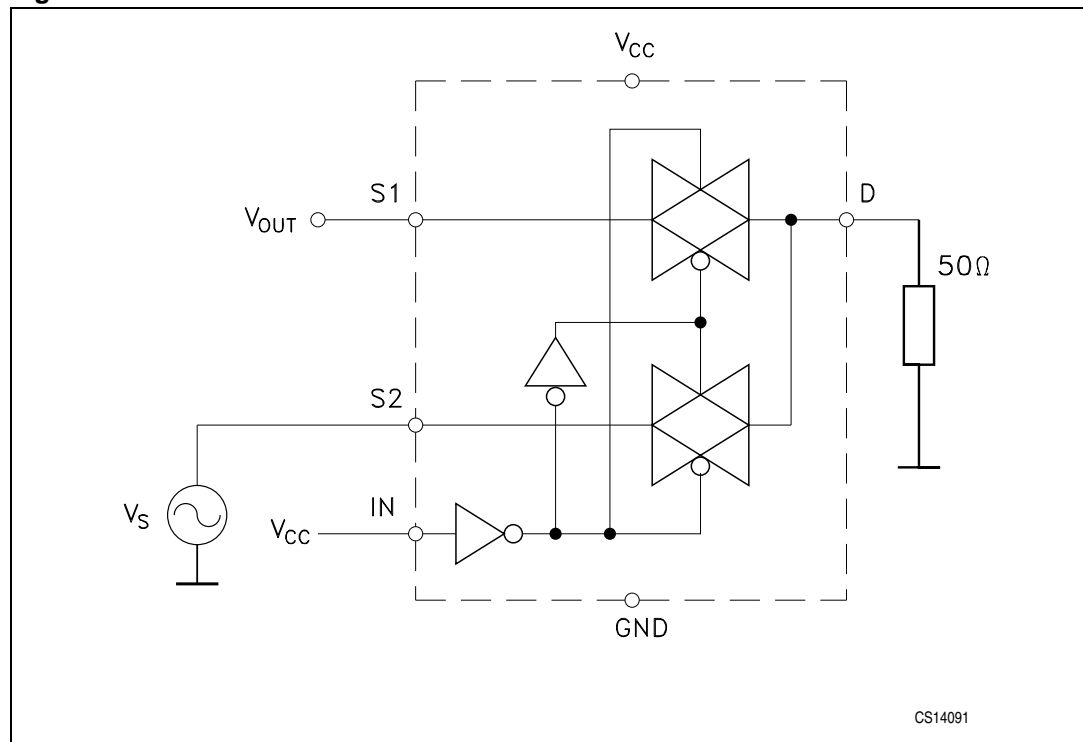
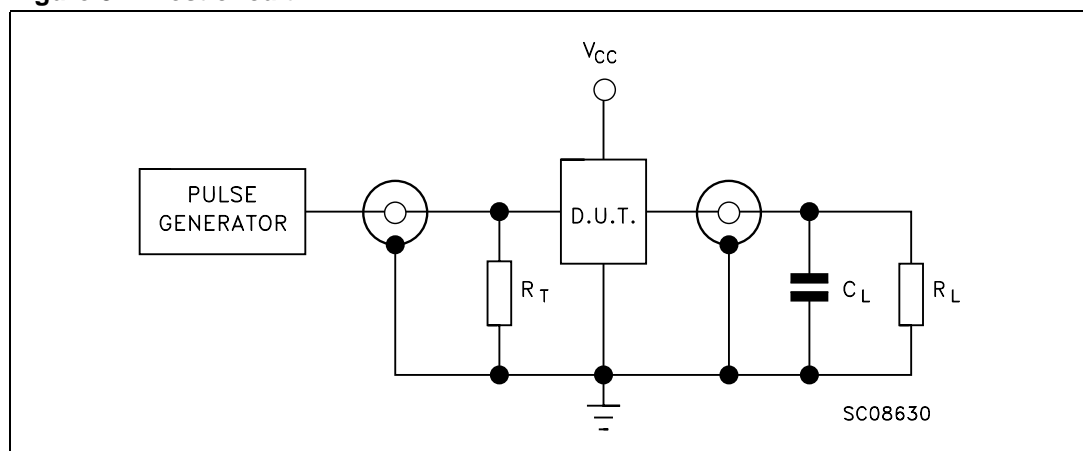
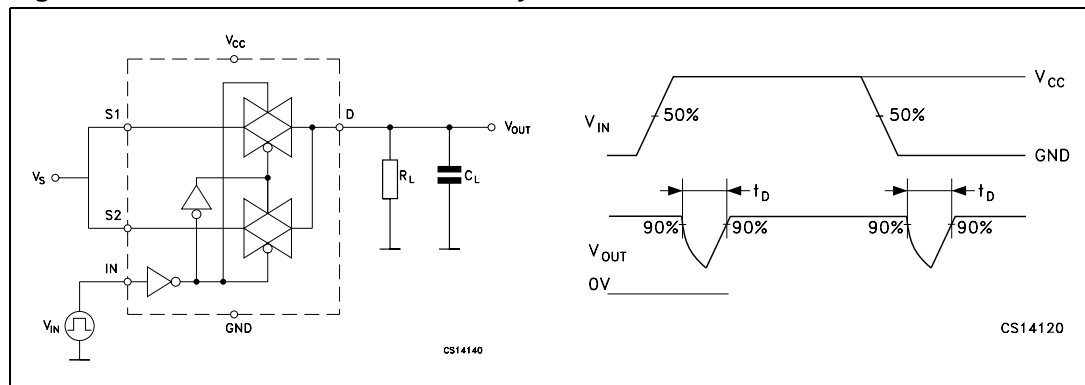
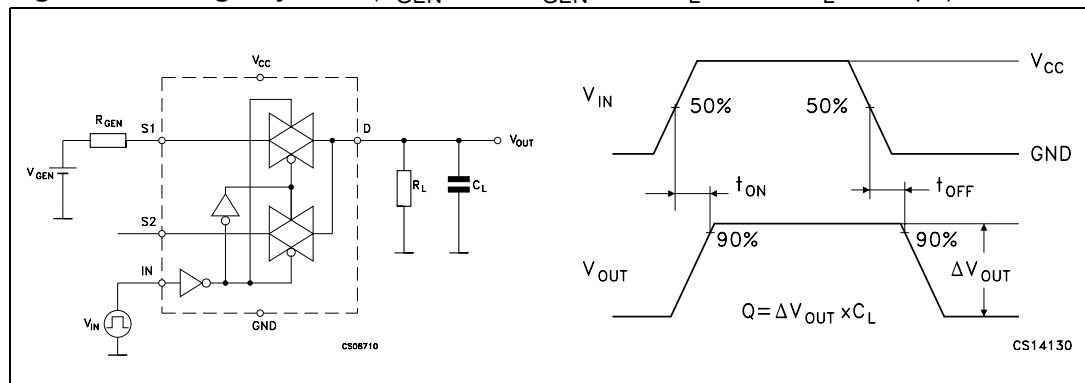
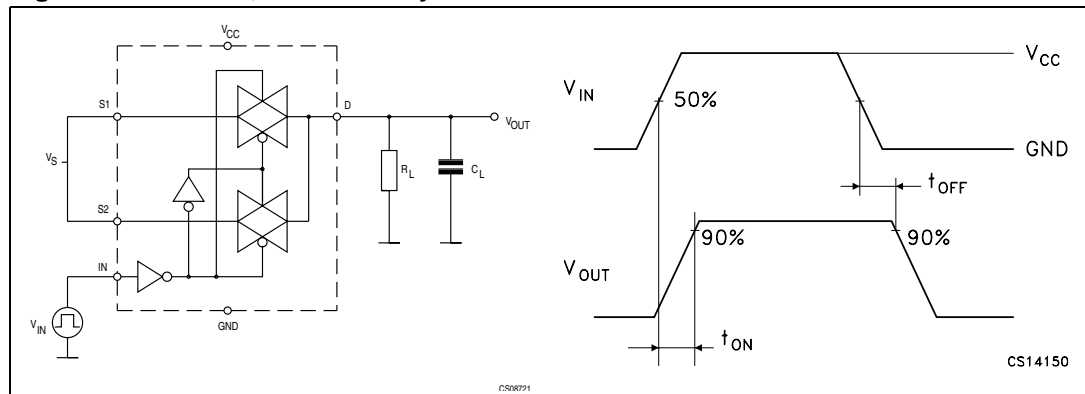


Figure 7. Channel-to-channel crosstalk**Figure 8. Test circuit**

1. $C_L = 5/35$ pF or equivalent (includes jig and probe capacitance)
2. $R_L = 50\ \Omega$ or equivalent
3. $R_T = Z_{OUT}$ of pulse generator (typically $50\ \Omega$)

Figure 9. Break-before-make time delay**Figure 10. Charge injection** ($V_{GEN} = 0\text{ V}$, $R_{GEN} = 0\ \Omega$, $R_L = 1\text{ M}\Omega$, $C_L = 100\text{ pF}$)**Figure 11. Turn on, turn off delay time**

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 12. QFN10L (1.8 x 1.4 x 0.5 mm) package outline

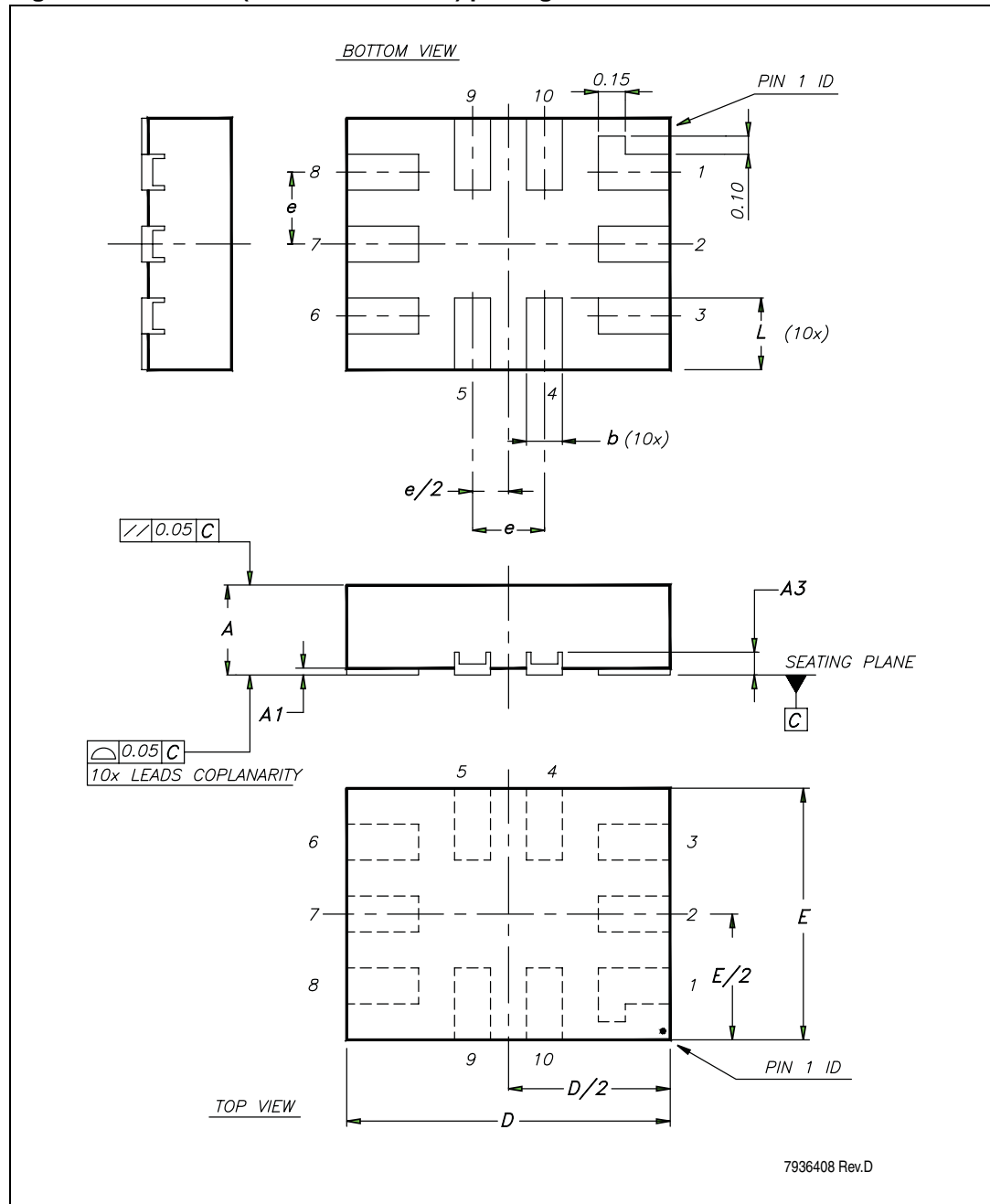


Table 9. QFN10L (1.8 x 1.4 x 0.5 mm) mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	0.45	0.50	0.55
A1	0	0.02	0.05
A3		0.127	
b	0.15	0.20	0.25
D	1.75	1.80	1.85
E	1.35	1.40	1.45
e		0.40	
L	0.35	0.40	0.45
L1	0.45	0.50	0.55

Figure 13. QFN10L (1.8 x 1.4 x 0.5 mm) recommended footprint

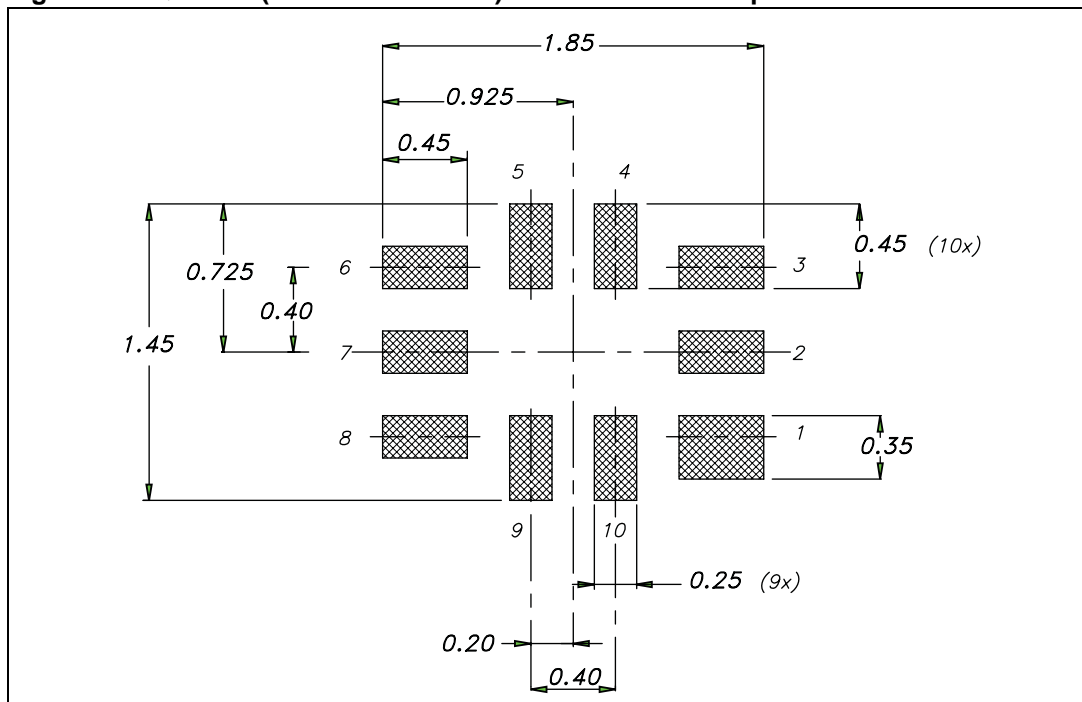


Figure 14. QFN10L (1.8 x 1.4 mm) carrier tape

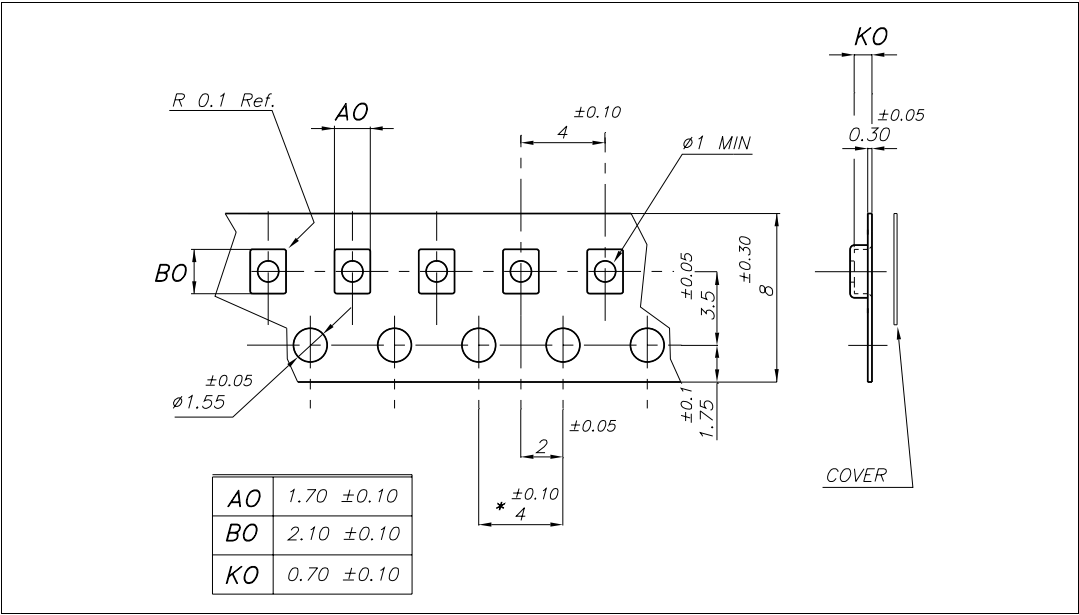


Figure 15. QFN10L (1.8 x 1.4 mm) reel information - back view

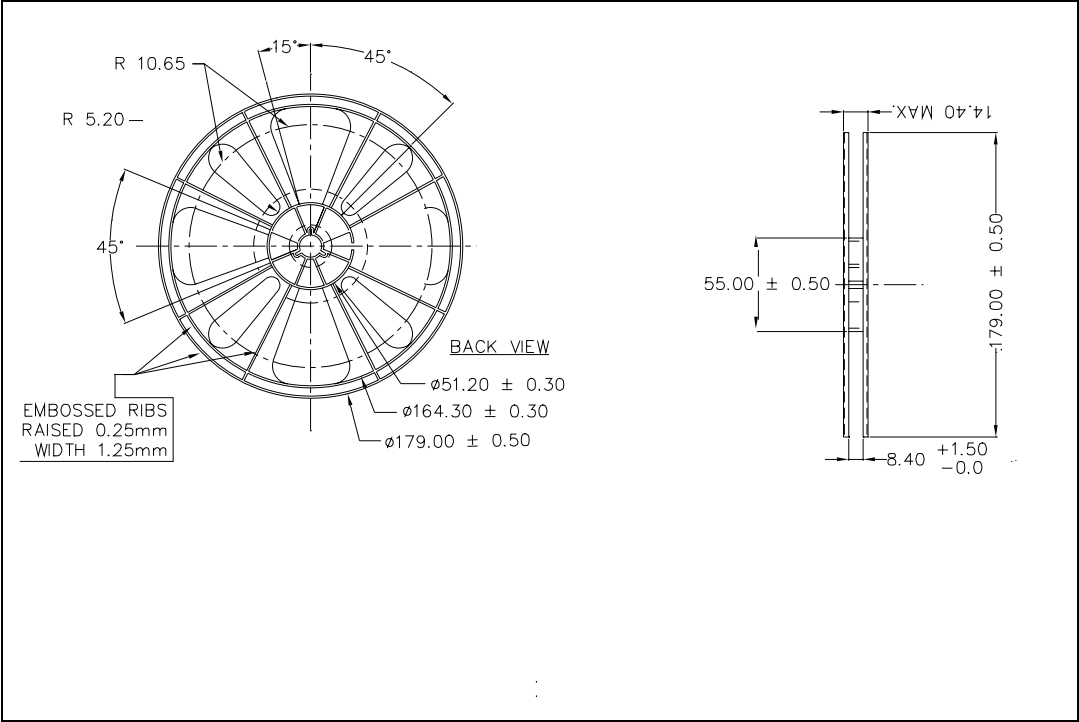
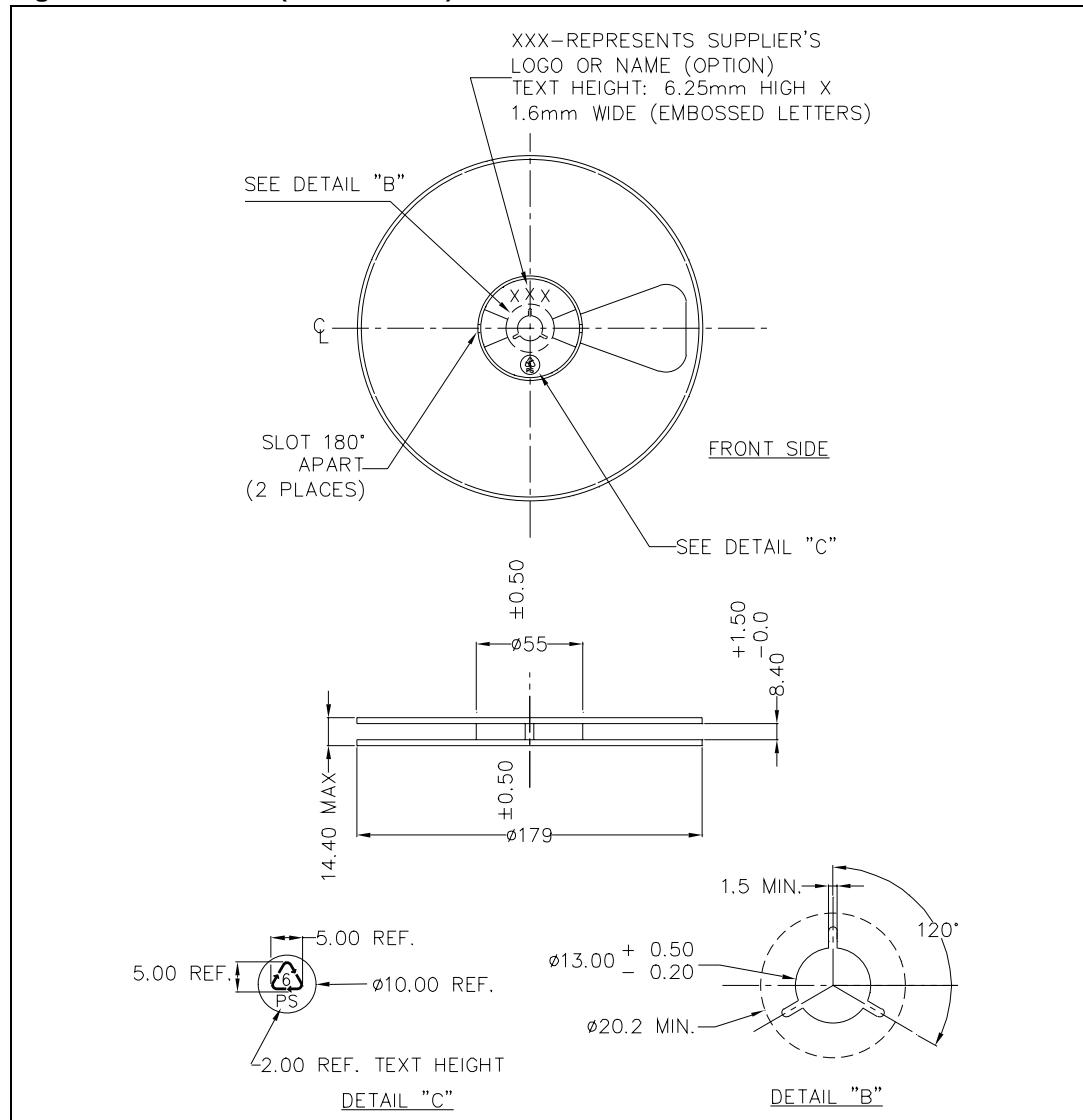


Figure 16. QFN10L (1.8 x 1.4 mm) reel information - front side



7 Revision history

Table 10. Document revision history

Date	Revision	Changes
06-Dec-2007	1	Initial release.
10-Jul-2008	2	Updated ΔR_{ON} and R_{FLAT} in Table 6 .

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