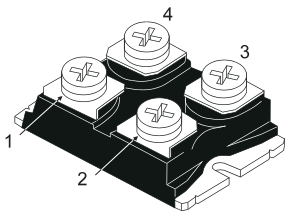
STE250NS10

N-channel 100V - 0.0045Ω - 220A - ISOTOP STripFET™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STE250NS10	100V	<0.0055Ω	220A

- Standard threshold drive
- 100% avalanche tested

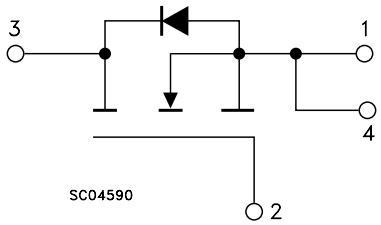


ISOTOP

Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STE250NS10	E250NS10	ISOTOP	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (v_{gs} = 0)	100	V
V_{GS}	Gate- source voltage	±20	V
I_D	Drain current (continuos) at T_C = 25°C	220	A
I_D	Drain current (continuos) at T_C = 100°C	156	A
I_{DM} (1)	Drain current (pulsed)	880	A
P_{TOT}	Total dissipation at T_C = 25°C	500	W
	Derating factor	4	W/°C
dv/dt(2)	Peak diode recovery voltage slope	3.5	V/ns
V_{ISO}	Insulation winthstand voltage (DC)	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	150 -55 to 150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 220A$, di/dt $\leq 200A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

Table 2. Thermal data

$R_{thj\text{-}case}$	Thermal resistance junction-case Max	0.25	°CW
$R_{thj\text{-}a}$	Thermal resistance junction-ambient Max	50	°CW

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	220	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=64V)	800	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 1 mA, V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating			50	µA
		V_{DS}= Max rating, T_C=125°C			500	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			±400	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 125A		0.0045	0.0055	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	V_{DS} = 20V, I_D=70A		60		S
C_{iss}	Input capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		31		nF
C_{oss}	Output capacitance			4.3		nF
C_{rss}	Reverse transfer capacitance			1.2		nF
Q_g	Total gate charge	V_{DD} = 50V, I_D = 22A, V_{GS} = 10V		900		nC
Q_{gs}	Gate-source charge			160		nC
Q_{gd}	Gate-drain charge			330		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=50 V, I_D=125A, R_G=4.7Ω, V_{GS}= 10V (see Figure 13)		110		ns
t_r	Rise time			380		ns
$t_{d(off)}$	Turn-off-delay time	V_{DD}=50 V, I_D=125A, R_G=4.7Ω, V_{GS}= 10V (see Figure 13)		1100		ns
t_f	Fall time			300		ns
$t_{r(Voff)}$	Off-voltage rise time	V_{DD}=80V, I_D=220A, R_G=4.7Ω, V_{GS}=10V (see Figure 15)		950		ns
t_f	fall time			330		ns
t_c	cross-over time			600		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				220	A
I_{SDM} (1)	Source-drain current (pulsed)				880	A
V_{SD} (2)	Forward on voltage	I_{SD} = 220A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 220A, V_{DD} = 30V di/dt = 100A/µs, T_j = 150°C (see Figure 15)		200 1.35 13.5		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

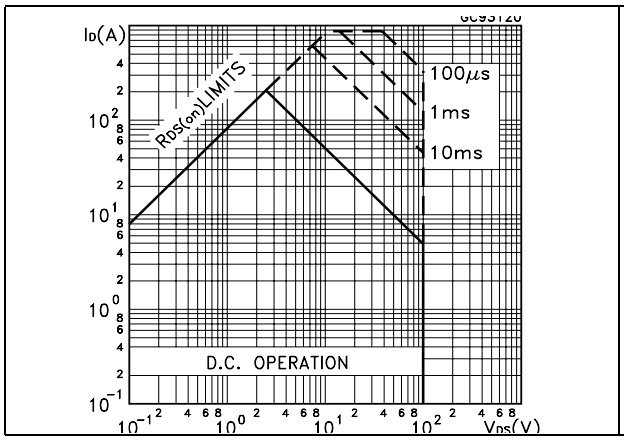


Figure 2. Thermal impedance

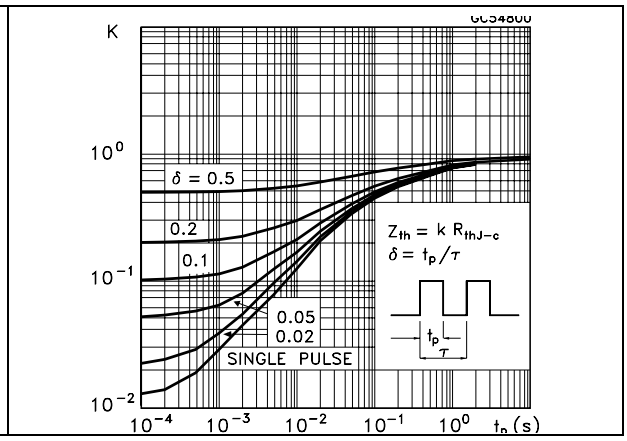


Figure 3. Output characterisics

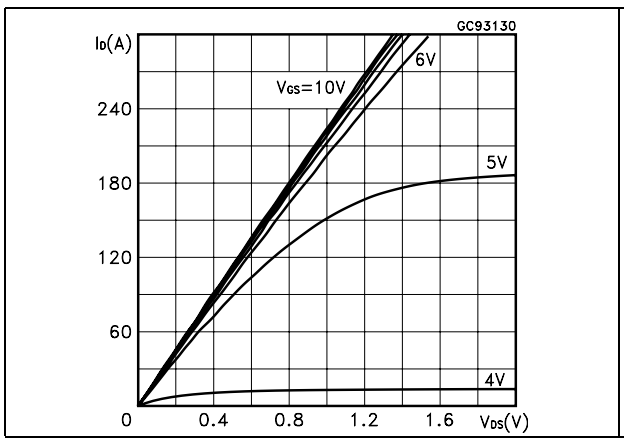


Figure 4. Transfer characteristics

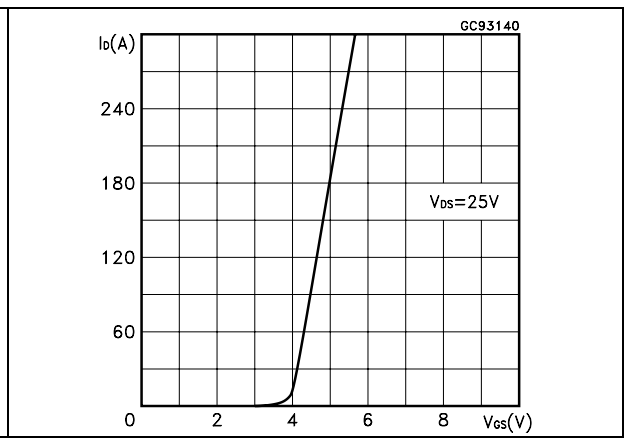


Figure 5. Transconductance

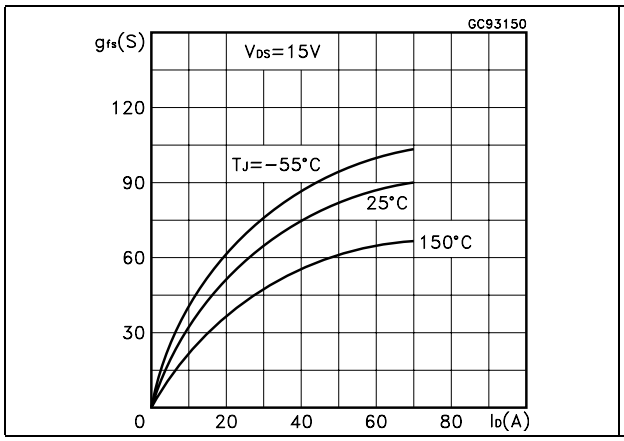


Figure 6. Static drain-source on resistance

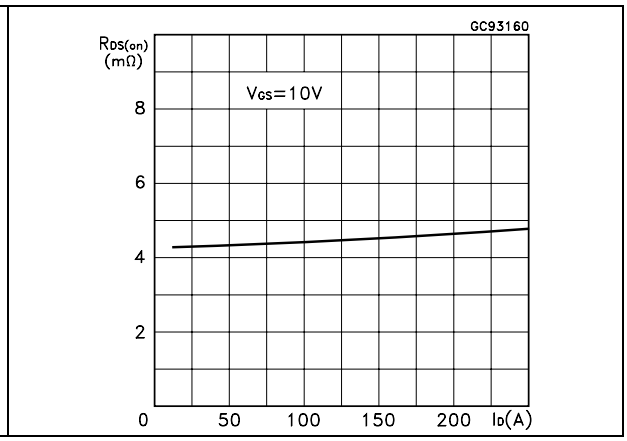


Figure 7. Gate charge vs gate-source voltage

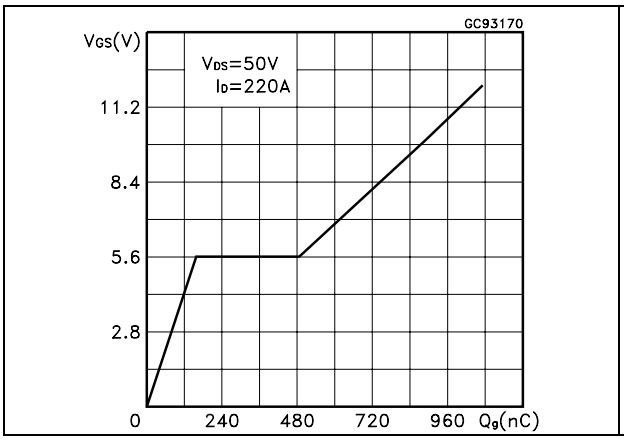


Figure 8. Capacitance variations

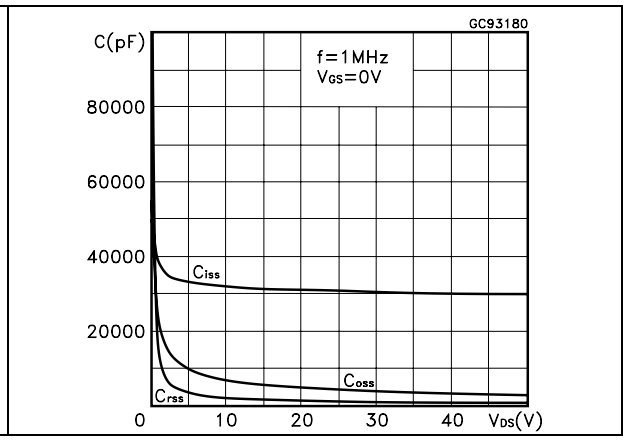


Figure 9. Normalized gate threshold voltage vs temperature

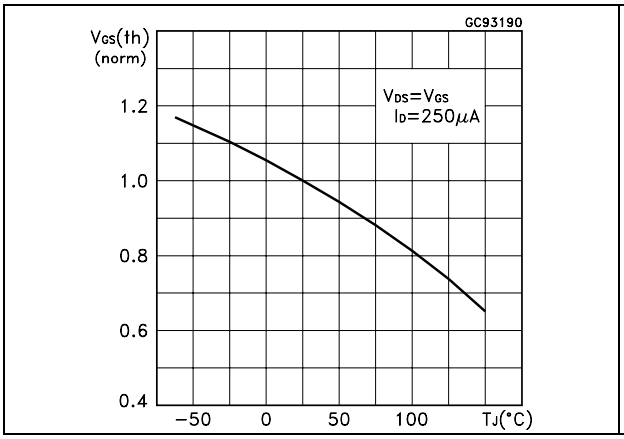


Figure 10. Normalized on resistance vs temperature

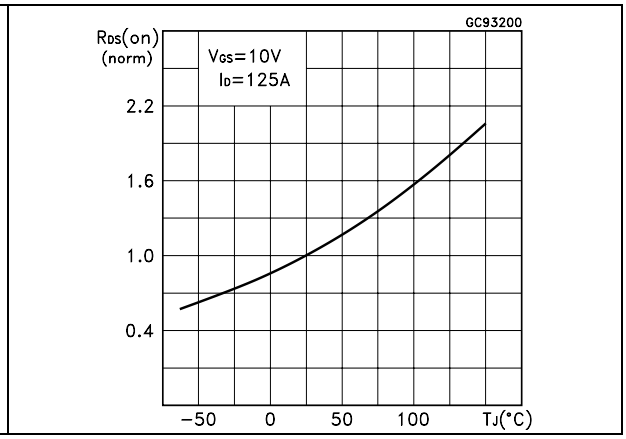


Figure 11. Source-drain diode forward characteristics

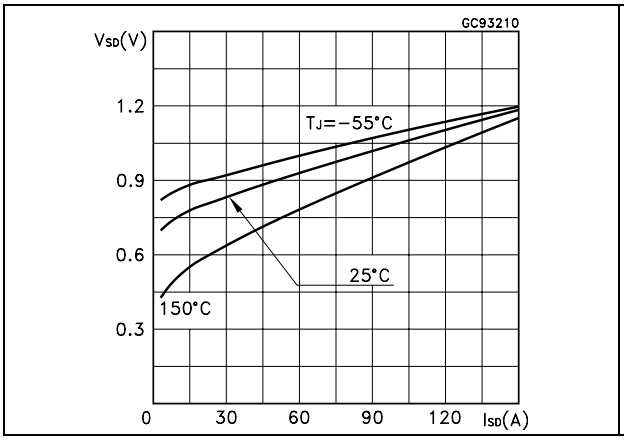
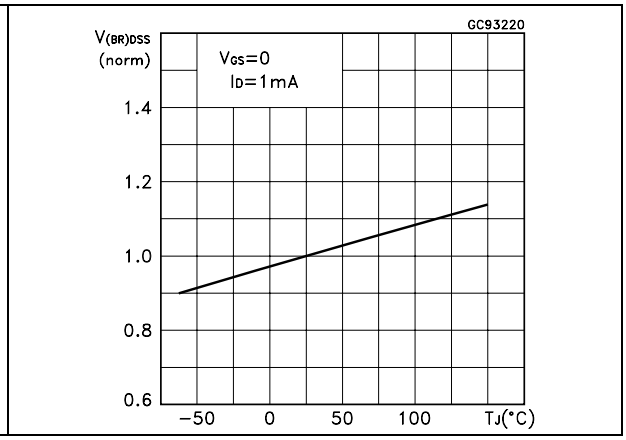


Figure 12. Normalized breakdown voltage vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

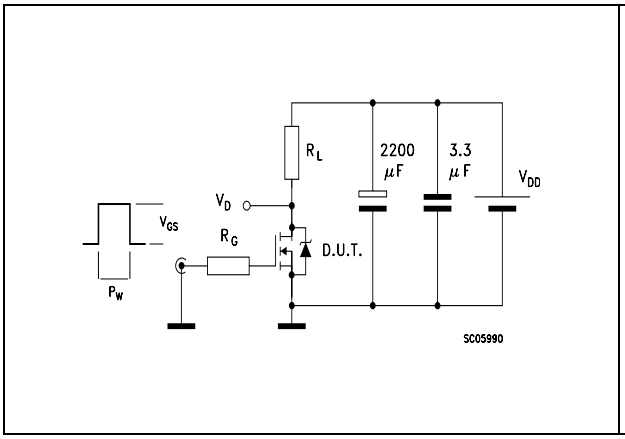


Figure 14. Gate charge test circuit

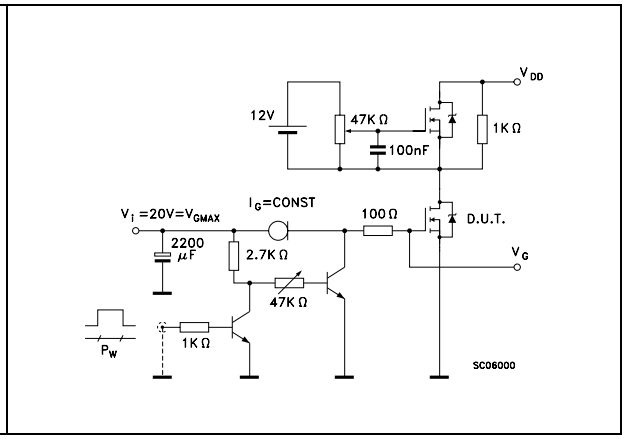


Figure 15. Test circuit for inductive load switching and diode recovery times

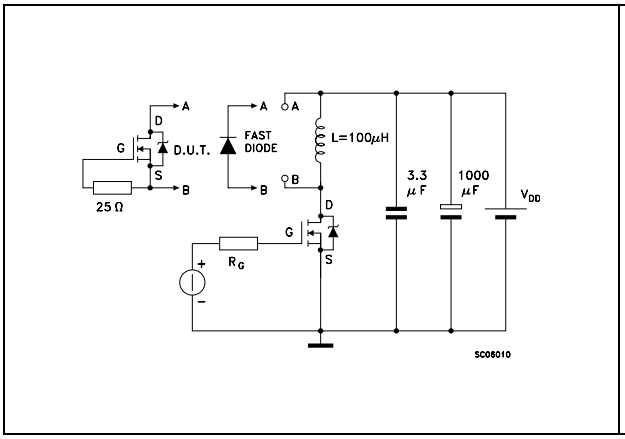


Figure 16. Unclamped Inductive load test circuit

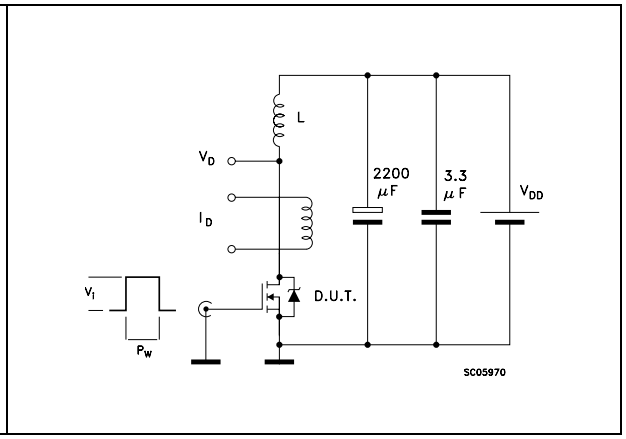


Figure 17. Unclamped inductive waveform

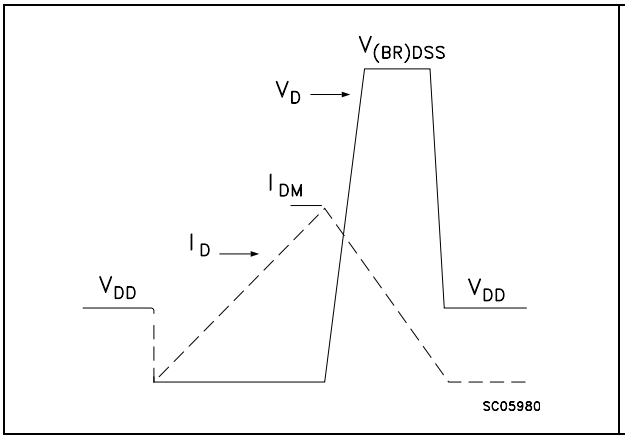
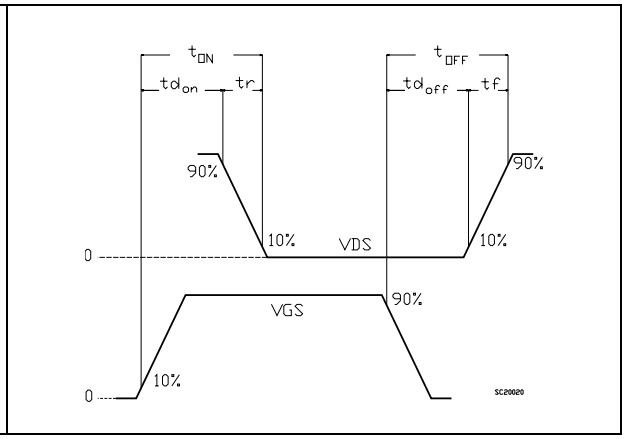


Figure 18. Switching time waveform

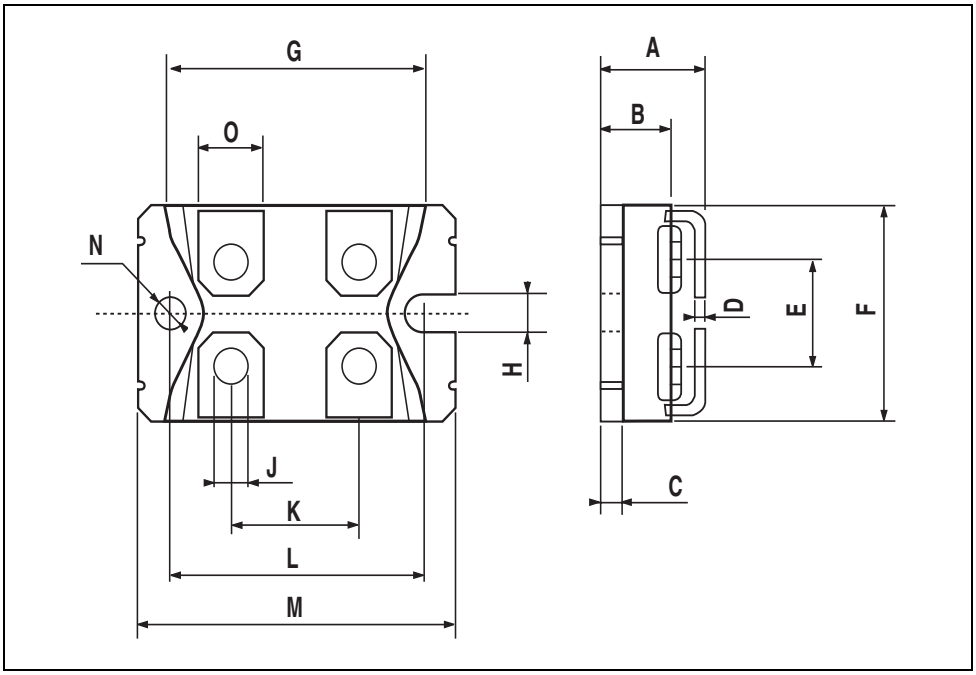


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : *www.st.com*

ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



5 Revision history

Table 8. Revision history

Date	Revision	Changes
21-Jun-2004	1	Complete version
04-Oct-2006	2	New template, no content change

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