



STB85NS04Z STB85NS04Z-1

N-channel 11mΩ - 80A - D²PAK - I²PAK
SAFeFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STB85NS04Z	Clamped	< 0.015Ω	80A ⁽¹⁾
STB85NS04Z-1	Clamped	< 0.015Ω	80A ⁽¹⁾

1. Current limited by wire bonding

- 100% avalanche tested
- Low capacitance and gate charge
- 175°C maximum junction temperature

Description

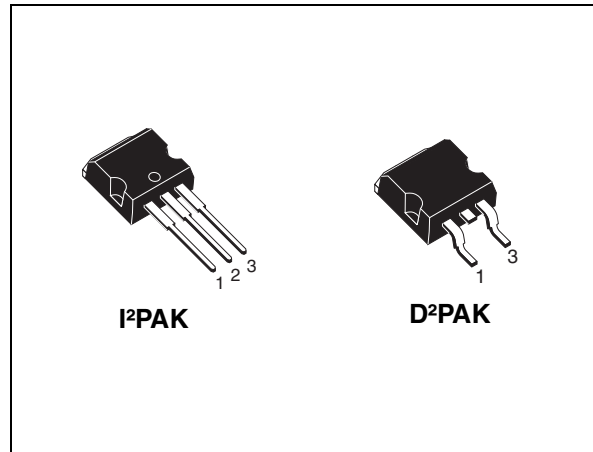
This fully clamped Power MOSFET is produced by using the latest advanced Company's Mesh Overlay™ process which is based on a novel strip layout. The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

Applications

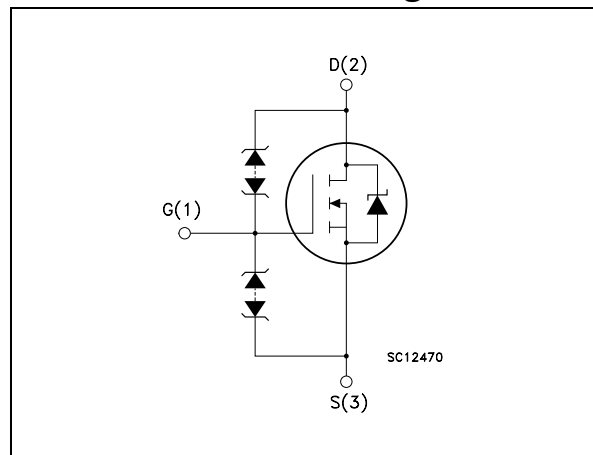
- Switching application
 - Automotive

Order codes

Part number	Marking	Package	Packaging
STB85NS04ZT4	B85NS04Z	D ² PAK	Tape & reel
STB85NS04Z-1	B85NS04Z-1	I ² PAK	Tube



Internal schematic diagram



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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	33 ⁽¹⁾	V
V_{GS}	Gate-source voltage	± 18	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80 ⁽²⁾	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	60	A
I_{DG}	Drain gate current (continuous)	± 50	mA
I_{GS}	Gate source current (continuous)	± 50	mA
$I_{DM}^{(3)}$	Drain current (pulsed)	320	A
	Derating factor	1.43	W/ $^\circ\text{C}$
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	215	W
$V_{ESD(G-S)}$	Gate-source ESD (HBM-C=100pF, R=1.5k Ω)	2	kV
$V_{ESD(G-D)}$	Gate-drain ESD (HBM-C=100pF, R=1.5k Ω)	4	kV
$V_{ESD(D-S)}$	Drain-source ESD (HBM-C=100pF, R=1.5k Ω)	4	kV
T_j	Operating junction temperature	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		

1. Voltage is limited by zener diodes
2. Current limited by wire bonding
3. Pulse width limited by safe operating area

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	I ² PAK	
$R_{thj-case}$	Thermal resistance junction-case max	0.7		$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	--	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5		$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300		$^\circ\text{C}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	60	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25^{\circ}\text{C}$, $I_D=I_{AS}$, $V_{DD}=30\text{V}$)	550	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$, $V_{GS} = 0$	33			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 16\text{V}$, $V_{DS} = 16\text{V}$, $T_c=125^{\circ}\text{C}$			10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 10\text{V}$			10	μA
V_{GSS}	Gate-source breakdown voltage	$I_{GS} = 100\mu\text{A}$	18		25	V
R_G	Series gate resistance			14		Ω
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 1\text{mA}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 30\text{A}$		11	15	$\text{m}\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	$V_{DS} = 25\text{V}$, $I_D = 30\text{A}$		50		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		2500		pF
C_{oss}	Output capacitance			800		pF
C_{rss}	Reverse transfer capacitance			150		pF
Q_g	Total gate charge	$V_{DD} = 16\text{V}$, $I_D = 60\text{A}$		68	100	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{V}$		15		nC
Q_{gd}	Gate-drain charge	(see Figure 14)		19		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage rise time	$V_{clamp}=30V$, $I_D=60A$ $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 15)		85		ns
t_f	Fall time			145		ns
t_c	Cross-over time			90		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				80	A
I_{SDM}	Source-drain current (pulsed)				320	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD}=60A$, $V_{GS}=0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=60A$, $V_{DD}=100V$ $di/dt=25A/\mu s$, $T_j=150^\circ C$ (see Figure 18)		65		ns
Q_{rr}	Reverse recovery charge			0.15		μC
I_{RRM}	Reverse recovery current			4.5		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

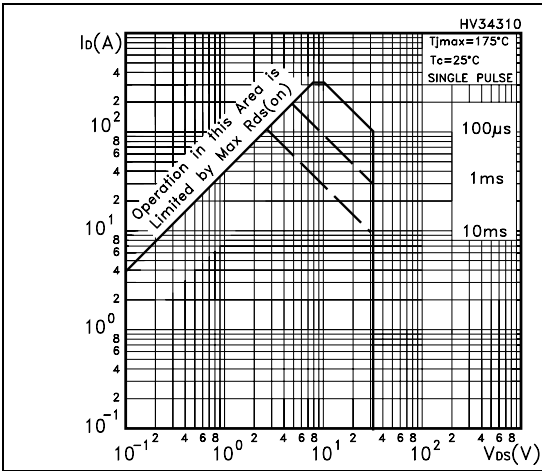


Figure 2. Thermal impedance

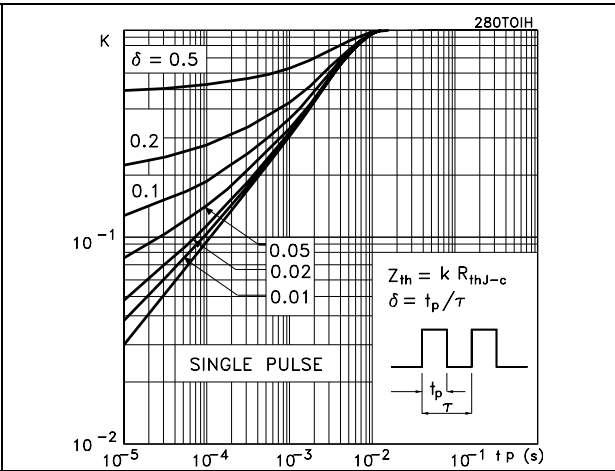


Figure 3. Output characteristics

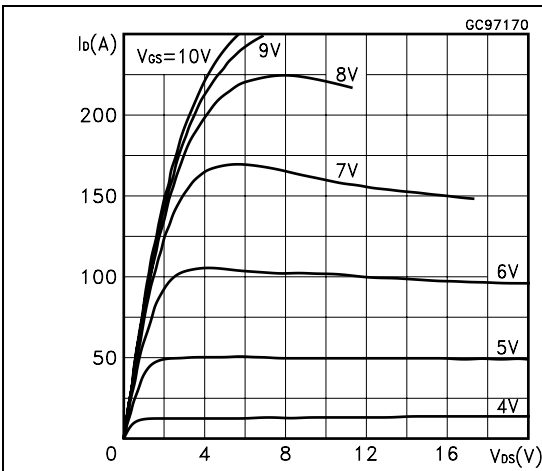


Figure 4. Transfer characteristics

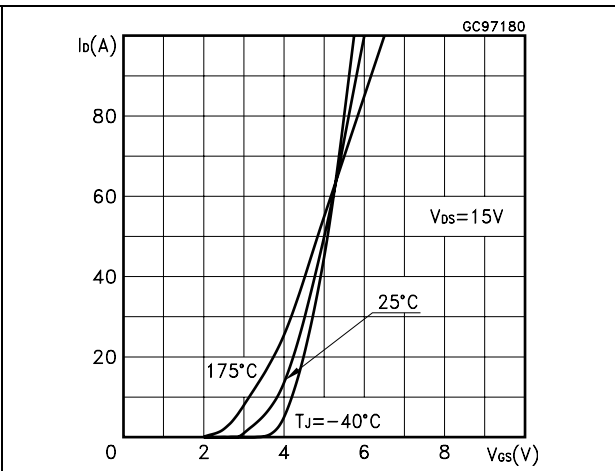


Figure 5. Transconductance

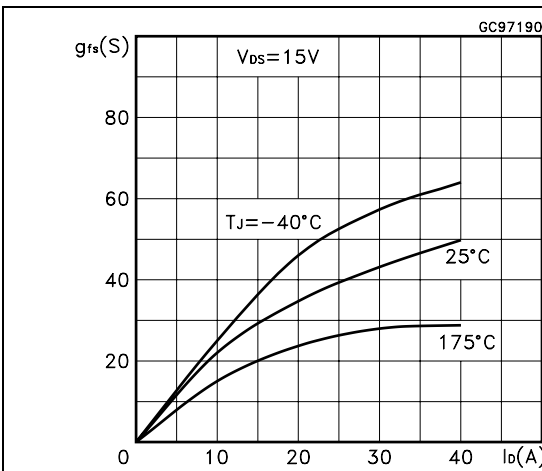


Figure 6. Static drain-source on resistance

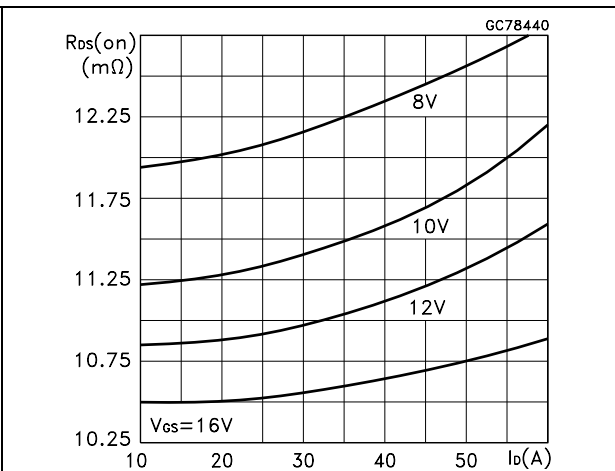


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

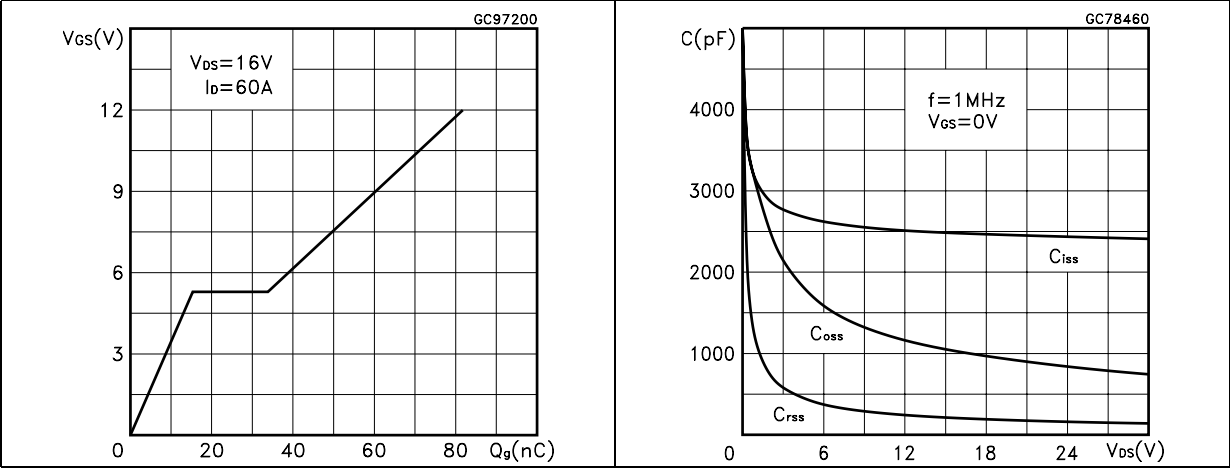


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

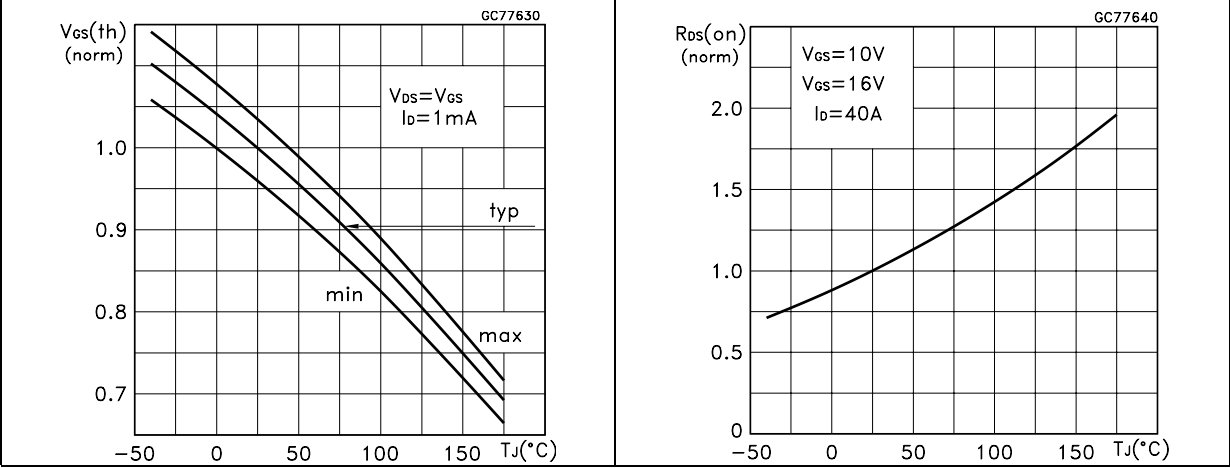
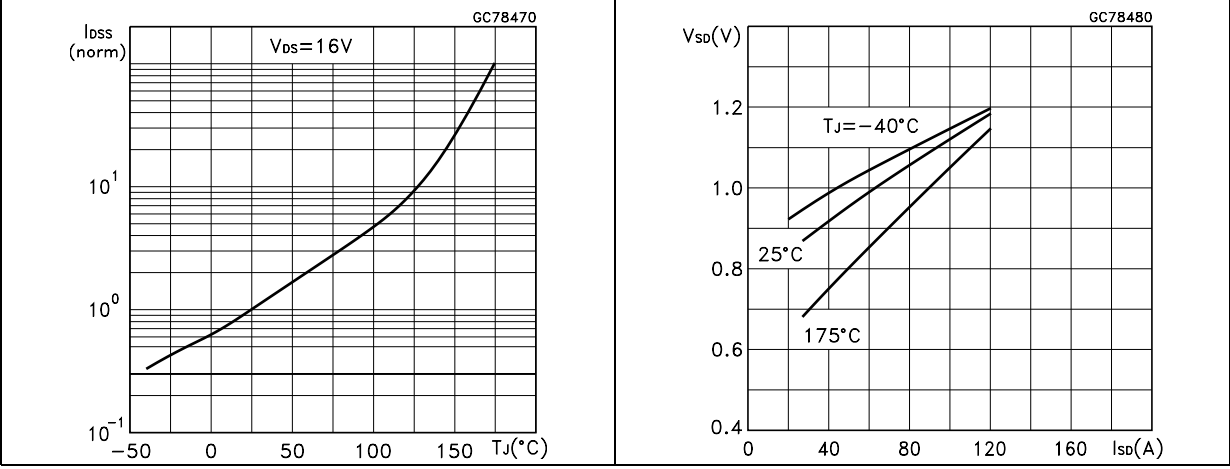


Figure 11. Zero gate voltage drain current vs temperature Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

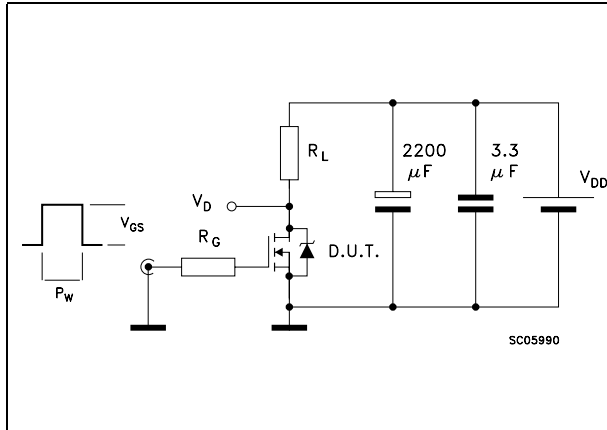


Figure 14. Gate charge test circuit

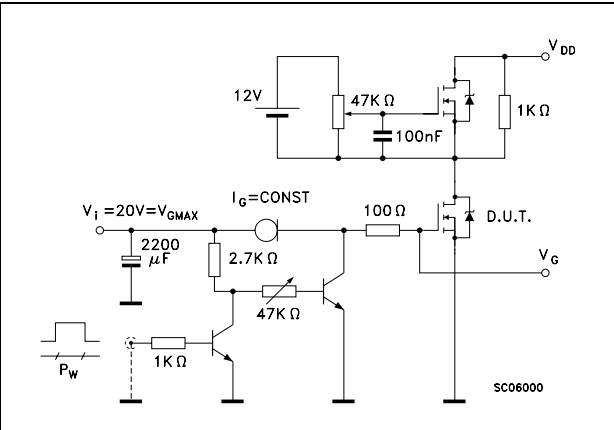


Figure 15. Test circuit for inductive load switching and diode recovery times

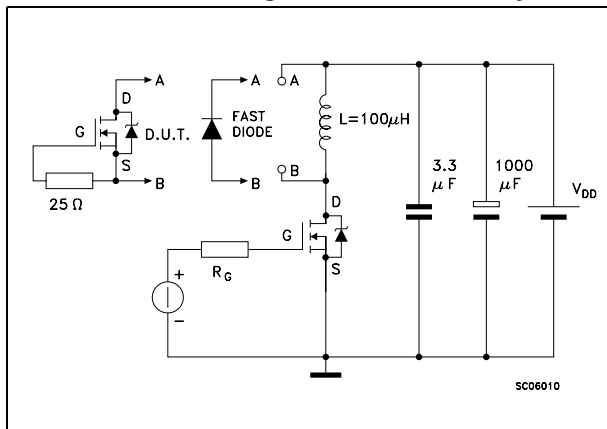


Figure 16. Unclamped inductive load test circuit

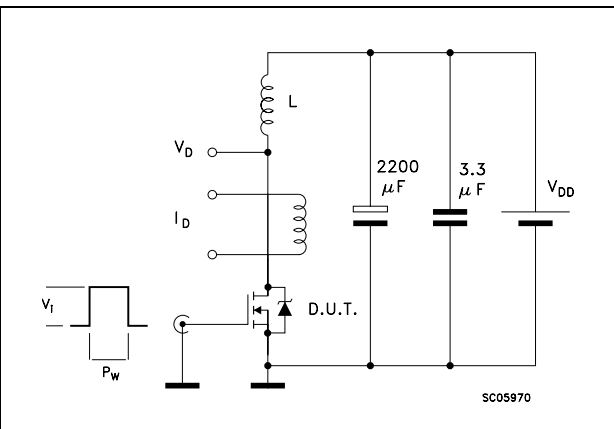


Figure 17. Unclamped inductive waveform

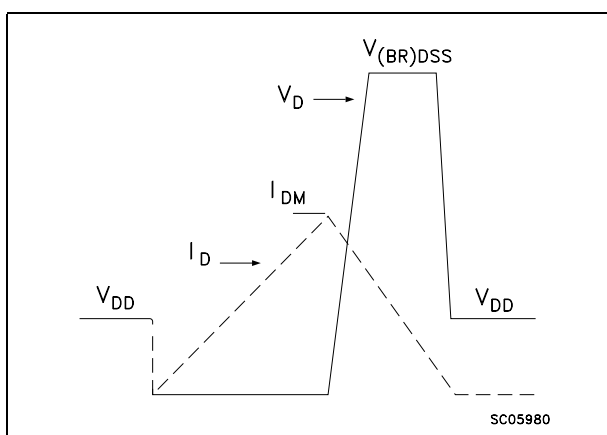
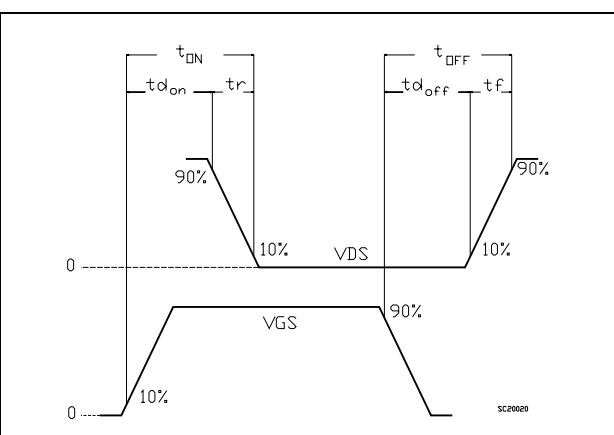


Figure 18. Switching time waveform

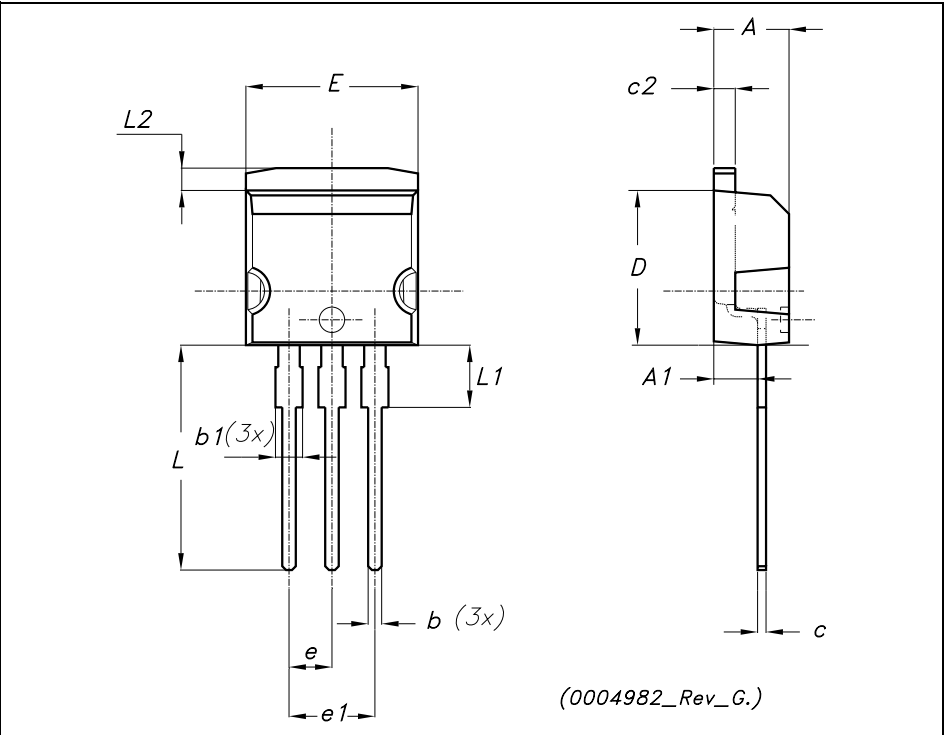


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

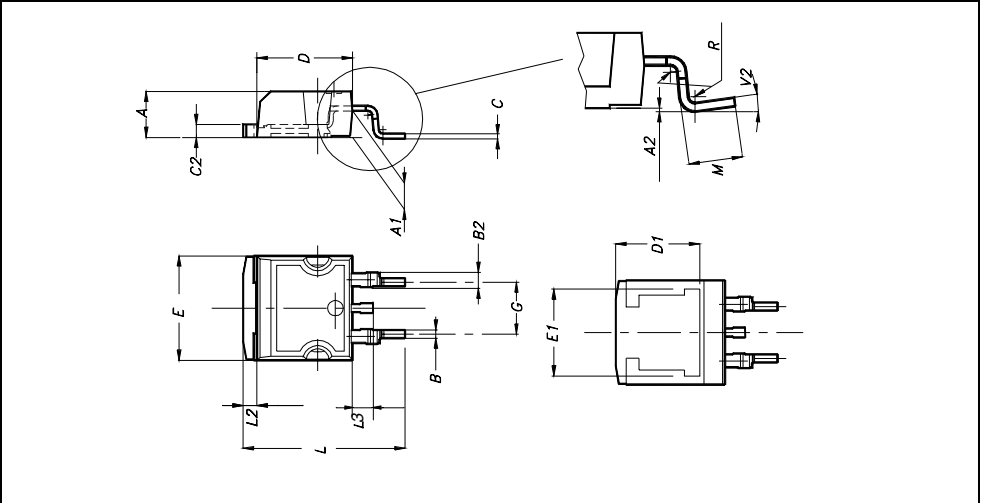
TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



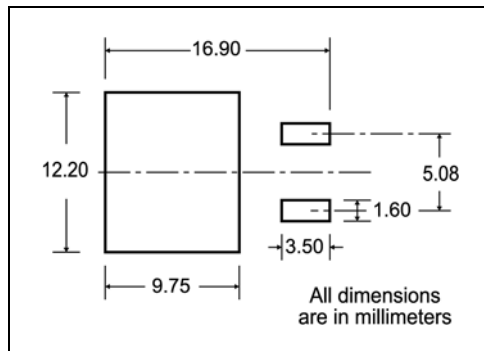
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

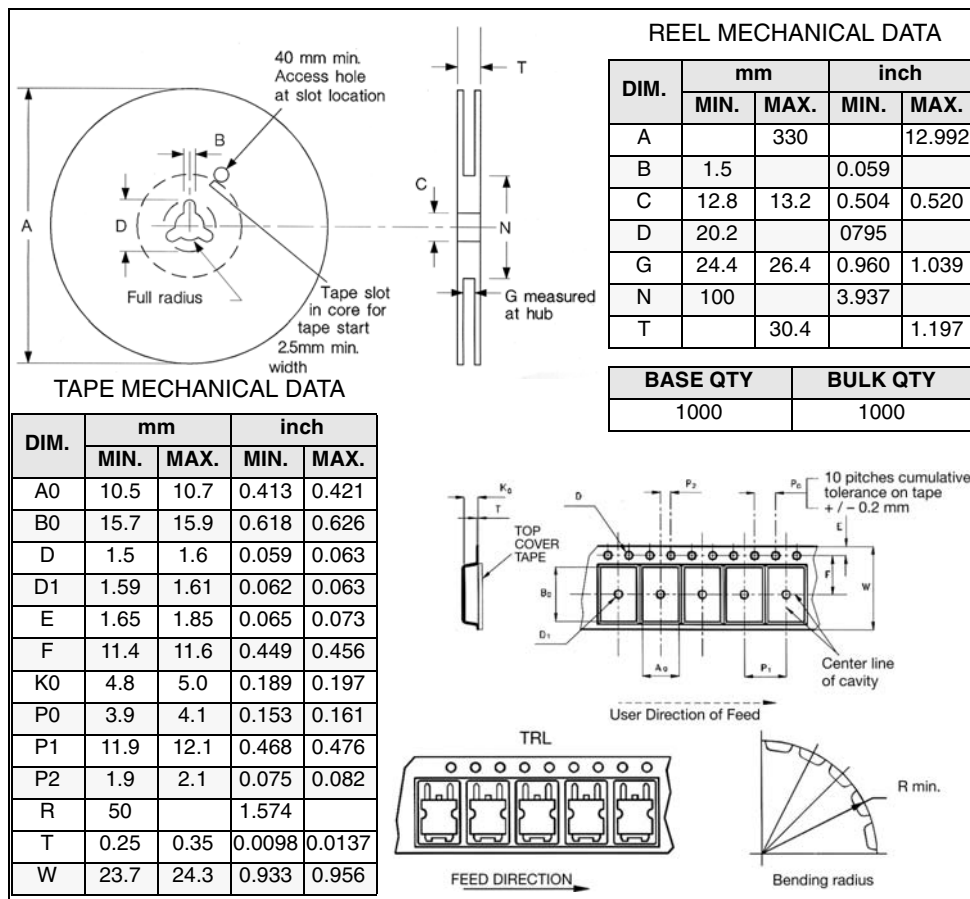


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 8. Revision history

Date	Revision	Changes
25-Sep-2006	1	First release

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