



# STB5600

## GPS RF FRONT-END IC

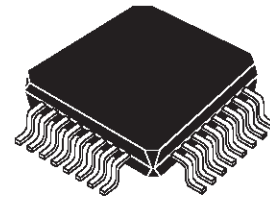
- ONE CHIP SYSTEM TO INTERFACE ACTIVE ANTENNA TO ST20GP1 MICROCONTROLLER
- COMPLETE RECEIVER USING NOVEL DUAL CONVERSION ARCHITECTURE WITH SINGLE IF FILTER
- MINIMUM EXTERNAL COMPONENTS
- COMPATIBLE WITH GPS L1 SPS SIGNAL
- INTERNALLY STABILISED POWER RAILS
- CMOS OUTPUT LEVELS
- FROM 3.3 TO 5.9V SUPPLY VOLTAGE
- TQFP32 PACKAGE

### DESCRIPTION

The STB5600, using STMicroelectronics HSB2, High Speed Bipolar technology, implements a Global Positioning System RF front-end.

The chip provides down conversion from the GPS (L1) signal at 1575 MHz via an IF of 20MHz to an output frequency of 4MHz suitable for ST20GP1 GPS processor.

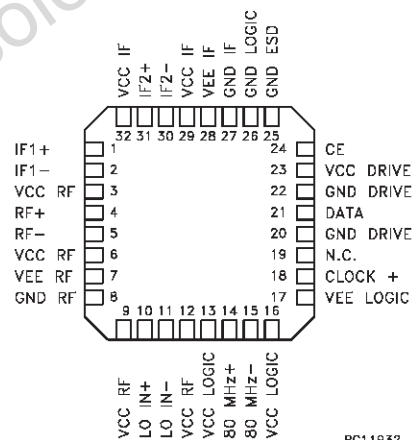
It uses a single external reference oscillator to generate both RF local oscillator signals and the processor reference clock.



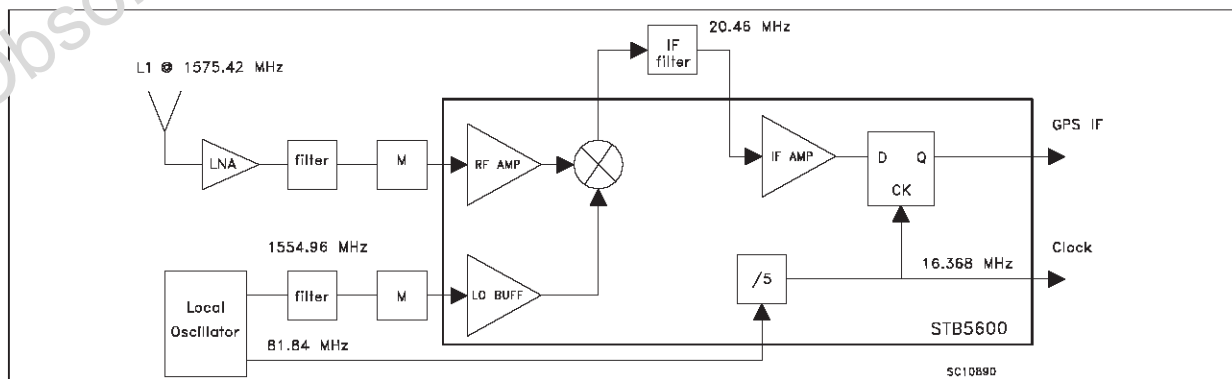
**TQFP32**

**MARKING:**  
STB5600  
TRACEABLE CODE  
ASSY CODE

### PIN CONNECTION (top view)



PC11932



**FUNCTIONAL DESCRIPTION**

The STB5600 GPS front-end is fed with the signal from an active antenna, via a ceramic RF filter. The gain between the antenna element and the STB5600 is expected to be between 10dB and 35dB overall, made up of the antenna LNA gain, the feeder loss, connector loss, and the ceramic filter loss.

In order to use an off-the-shelf ceramic filter, conventionally 50 Ohms single ended, a matching circuit is used. (see appendix A.1), which provides a 300 Ohm differential drive to the STB5600. A similar circuit can be used to feed the LO signal if using the recommended low-cost oscillator circuit (appendix A.3).

Note that the STB5600 radio architecture and the oscillator described here are covered by various patents held by SGS-Thomson and by others. The use of the circuits described in this data-sheet for any other purpose may infringe such patents.

**- RF SECTION**

The differential input signal is amplified by the RF-Amp and mixed with the oscillator signal amplified from the LO+,LO- inputs to generate a balanced 20.46MHz IF signal. The LO buffer amplifier may be fed differential or single ended signals, at levels between -60dBm and -20dBm .

**- IF SECTION**

The 20MHz differential signal from the mixer is fed through an external LC filter to suppress undesirable signals and mixer products. The multi-stage high-sensitivity limiting amplifier is connected to a D-type latch clocked by an internally derived 16MHz clock.. The effect of sampling the 20MHz signal at 16MHz is to create a sub-sampling alias at 4MHz. This is fed to the output level-converters.

**- DIVIDER SECTION**

The 80MHz oscillator signal may be provided single-ended or differentially to the high impedance 80MHz+, 80MHz- inputs. Any unused inputs should be connected to GNDLOGIC via a 1nF capacitor. The 80MHz signal is amplified, then divided by 5 to create the 16.368MHz clock required by the ST20GP1 processor, also used to clock the output latch of the STB5600.

**- OUTPUT SECTION**

The output latch samples the 20.46MHz intermediate frequency at a 16.368MHz rate, performing the dual function of second downconversion and latching. The downconversion occurs by sub-sampling aliasing, such that the digital output represents a 4.096MHz centre frequency

The output buffers perform level translation from the internal ECL levels to CMOS compatible outputs referred to external ground.

**ABSOLUTE MAXIMUM RATINGS**

| Symbol               | Parameter                           | Value      | Unit |
|----------------------|-------------------------------------|------------|------|
| V <sub>CC</sub>      | DC Supply Voltage                   | 5.9        | V    |
| RF+, RF-             | RF Input                            | 8          | dBm  |
| T <sub>j</sub>       | Junction Temperature                | 150        | °C   |
| T <sub>stg</sub>     | Storage Temperature Range           | -40 to 125 | °C   |
| R <sub>thj-amb</sub> | Thermal Resistance Junction-ambient | 80         | °C/W |

## PIN CONFIGURATION

Apply 5V at the CE, V<sub>CCRF</sub>, V<sub>CCIF</sub>, V<sub>CCLOGIC</sub> pins, apply 3 V at the V<sub>CCDRIVE</sub>

| Pin | Symbol               | Typ. DC Bias | Dexription               | External circuit               |
|-----|----------------------|--------------|--------------------------|--------------------------------|
| 1   | IF1+                 | 3.6 V        | Mixer Output 1           | see application circuit        |
| 2   | IF1-                 | 3.6 V        | Mixer Output 2           | see application circuit        |
| 3   | V <sub>CCRF</sub>    | 5 V          | RF Power Supply          | 100 nF to V <sub>EERF</sub>    |
| 4   | RF+                  | 3.5 V        | RF Input                 | AC Coupled                     |
| 5   | RF-                  | 3.5 V        | RF Input                 | AC Coupled                     |
| 6   | V <sub>CCRF</sub>    | 5 V          | RF Power Supply          | 100 nF to V <sub>EERF</sub>    |
| 7   | V <sub>EERF</sub>    | 2 V          | RF Voltage Reference     | 100 nF to V <sub>CCRF</sub>    |
| 8   | GND <sub>RF</sub>    | 0 V          | RF Ground                |                                |
| 9   | V <sub>CCRF</sub>    | 5 V          | RF Power Supply          | 100 nF to V <sub>EERF</sub>    |
| 10  | LO+                  | 3.5 V        | Local Oscillator Input   | AC Coupled                     |
| 11  | LO-                  | 3.5 V        | Local Oscillator Input   | AC Coupled                     |
| 12  | V <sub>CCRF</sub>    | 5 V          | RF Power Supply          | 100 nF to V <sub>EERF</sub>    |
| 13  | V <sub>CCLOGIC</sub> | 5 V          | Logic Power Supply       | 100 nF to V <sub>EELOGIC</sub> |
| 14  | 80 MHz+              | 4 V          | 80 MHz Clock Input       | AC Coupled                     |
| 15  | 80 MHz-              | 4 V          | 80 MHz Clock Input       | AC Coupled                     |
| 16  | V <sub>CCLOGIC</sub> | 5 V          | Logic Power Supply       | 100 nF to V <sub>EELOGIC</sub> |
| 17  | V <sub>EELOGIC</sub> | 2 V          | Logic Voltage Reference  | 100 nF to V <sub>CCLOGIC</sub> |
| 18  | CLOCK+               | 0.3 V or 3 V | 16 MHz Clock CMOS Output | 7 pF to GND <sub>DRIVE</sub>   |
| 19  | Not Connected        |              |                          |                                |
| 20  | GND <sub>DRIVE</sub> | 0 V          | CMOS Drive Ground        |                                |
| 21  | DATA                 | 0.3 V or 3 V | 4 MHz Data CMOS Output   | 7 pF to GND <sub>DRIVE</sub>   |
| 22  | GND <sub>DRIVE</sub> | 0 V          | CMOS Drive Ground        |                                |
| 23  | V <sub>CCDRIVE</sub> | 3 V          | CMOS Drive Power Supply  |                                |
| 24  | CE                   | 3 V          | Chip Enable              |                                |
| 25  | GND                  | 0 V          | Substrate Ground         |                                |
| 26  | GND <sub>LOGIC</sub> | 0 V          | Logic Ground             |                                |
| 27  | GND <sub>IF</sub>    | 0 V          | IF Ground                |                                |
| 28  | V <sub>EEIF</sub>    | 2 V          | IF Voltage Reference     | 100 nF to V <sub>CCIF</sub>    |
| 29  | V <sub>CCIF</sub>    | 5 V          | IF Power Supply          | 100 nF to V <sub>EEIF</sub>    |
| 30  | IF2-                 | 4 V          | Limiting Amplifier Input | see application circuit        |
| 31  | IF2+                 | 4 V          | Limiting Amplifier Input | see application circuit        |
| 32  | V <sub>CCIF</sub>    | 5 V          | IF Power Supply          | 100 nF to V <sub>EEIF</sub>    |

**ELECTRICAL SPECIFICATION** ( $V_{VCCRf} = 3.3\text{ V} \dots 5.9\text{ V}$ ;  $V_{VCCIF} = 3.3\text{ V} \dots 5.9\text{ V}$ ;  $V_{VCC\text{ LOGIC}} = 3.3\text{ V} \dots 5.9\text{ V}$   $V_{VCCDRIVE} = 3\text{ V}$ ;  $T_a = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

#### LNA MIXER

| Symbol      | Parameter                     | Note   | Min. | Typ.     | Max. | Unit           |
|-------------|-------------------------------|--|------|----------|------|----------------|
| $I_{VCCRf}$ | Supply Current                | $V_{VCCRf} = 5\text{ V}$   | 20   |          | 25   | mA             |
| $Z_{in}$    | Differential Input Impedance  | @ 1575 MHz AC Coupled at RF+ RF- inputs  |      | 300<br>1 |      | $\Omega$<br>pF |
| $Z_{out}$   | Differential Output Impedance | @ 20 MHz AC Coupled at IF1+ IF1- outputs   |      | 70<br>3  |      | $\Omega$<br>pF |
| $G_c$       | Voltage Conversion Gain       | $R_L > 3\text{ K}\Omega$ , $P_{IN} = -80\text{ dBm}$<br>( $V_{in} = 75\text{ }\mu\text{Vp}$ on $300\text{ }\Omega$ ) | 35   |          |      | dB             |
| IIP1        | Input Compression Point (1dB) | (see application circuit)  | -60  |          |      | dBm            |
| NF          | Noise figure                  |  |      | 5        |      | dB             |
| $f_{RF}$    | Input Signal Frequency (L1)   |  |      | 1575     |      | MHz            |
| $f_{IF}$    | Output Signal Frequency       |  |      | 20       |      | MHz            |

#### LO INPUT BUFFER

| Symbol   | Parameter                    | Note                                    | Min. | Typ.     | Max. | Unit           |
|----------|------------------------------|---|------|----------|------|----------------|
| $Z_{in}$ | Differential Input Impedance | @ 1555 MHz AC Coupled at LO+ LO- inputs |      | 300<br>1 |      | $\Omega$<br>pF |
|          | Input Signal Level           |   | -60  | -40      | -20  | dBm            |

#### LIMITING AMPLIFIER

| Symbol      | Parameter                    | Note                                    | Min. | Typ. | Max. | Unit             |
|-------------|------------------------------|---|------|------|------|------------------|
| $I_{VCCIF}$ | Supply Current               | $V_{VCCIF} = 5\text{ V}$                | 2.5  |      | 3.5  | mA               |
| $Z_{in}$    | Differential Input Impedance | @ 20 MHz AC Coupled at IF2+ IF2- inputs |      | 15   |      | $\text{K}\Omega$ |
| B           | Bandwidth 3dB                |   | 5    |      | 80   | MHz              |
| Sens        | Limiter sensitivity          | Input Signal @ 20 MHz AC Coupled        |      | 100  |      | $\mu\text{Vp}$   |
| $V_{INMAX}$ | Maximum Input Signal         | Input Signal @ 20 MHz AC Coupled        |      |      | 0.5  | Vp               |

#### CLOCK INPUT BUFFER

| Symbol         | Parameter                    | Note  | Min. | Typ.   | Max. | Unit                   |
|----------------|------------------------------|---|------|--------|------|------------------------|
| $I_{VCCLOGIC}$ | Supply Current               | $V_{VCC\text{ LOGIC}} = 5\text{ V}$           | 5    |        | 7    | mA                     |
| $Z_{in}$       | Differential Input Impedance | @ 80 MHz AC Coupled at 80 MHz+ 80 MHz- inputs |      | 8<br>2 |      | $\text{K}\Omega$<br>pF |
|                | Input Signal Level           | @ 80 MHz AC Coupled at 80 MHz+ 80 MHz- inputs | 5    |        | 100  | mVp                    |
| N              | Division Ratio               |   |      | 5      |      |                        |

## ELECTRICAL CHARACTERISTICS (Continued)

## OUTPUT SECTION

| Symbol         | Parameter           | Note                              | Min.        | Typ. | Max.        | Unit |
|----------------|---------------------|-----------------------------------|-------------|------|-------------|------|
| $I_{VCCDRIVE}$ | Supply Current      | $V_{VCCDRIVE} = 3\text{ V}$       |             | 8    |             | mA   |
| $V_{OH}$       | High output voltage | $V_p = V_{VCCDRIVE} = 3\text{ V}$ | $V_p - 0.4$ |      | $V_p$       | V    |
| $V_{OL}$       | Low output voltage  | $V_n = GND$                       | $V_n$       |      | $V_n + 0.4$ | V    |
| $t_r$          | Rise Time           | $C_{LOAD} = 7\text{ pF}$          |             | 6    |             | ns   |
| $t_f$          | Fall Time           | $C_{LOAD} = 7\text{ pF}$          |             | 2    |             | ns   |

## APPLICATION CIRCUIT

A typical application circuit is shown in figure 1. The RF input from the antenna download is fed via a ceramic filter and matching circuit to the RF+, RF- pins. The external LNA in the antenna should have between 10 and 35dB of amplifier gain, so the noise measured in a one MHz bandwidth should be

-114dBm for kTB in 1 MHz

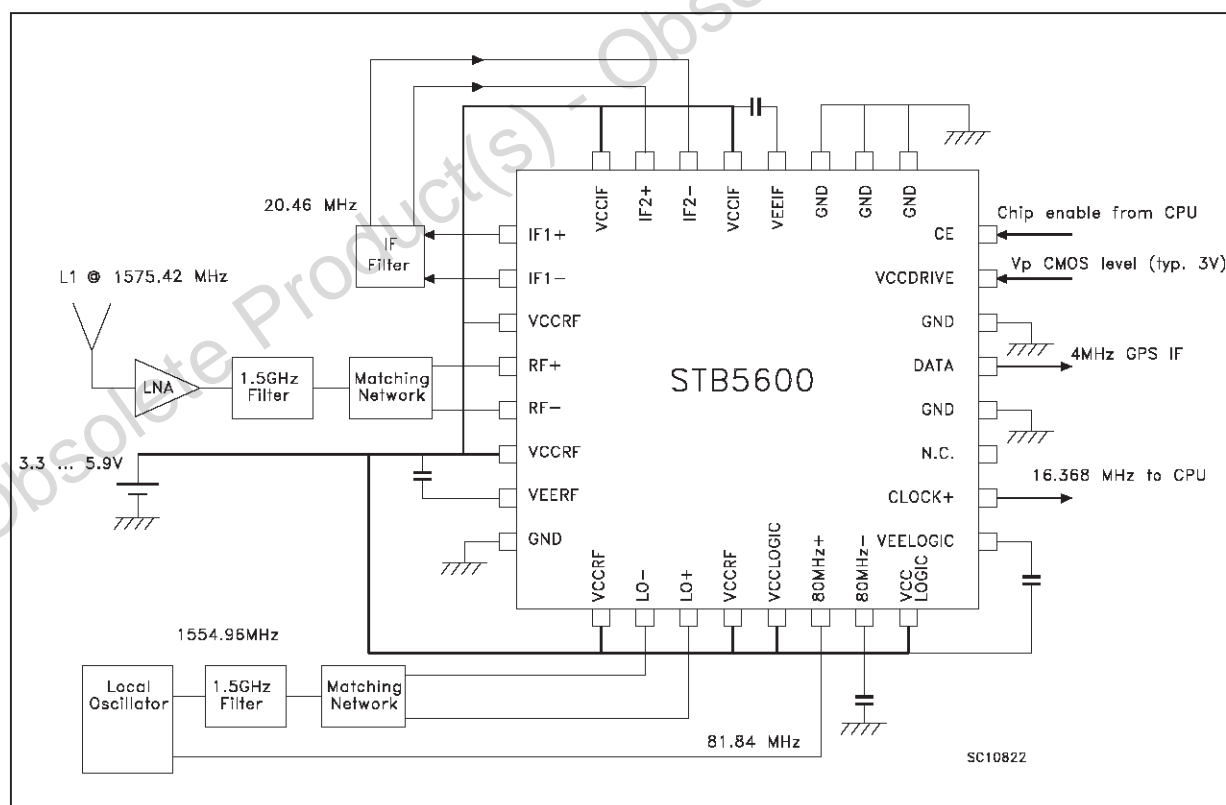
+ 2dB LNA noise figure

+10/35 dB LNA gain (net)

Total -102/77dBm at connector.

Allowing 2dB for filter loss, -104/-79 is available at the matching circuit.

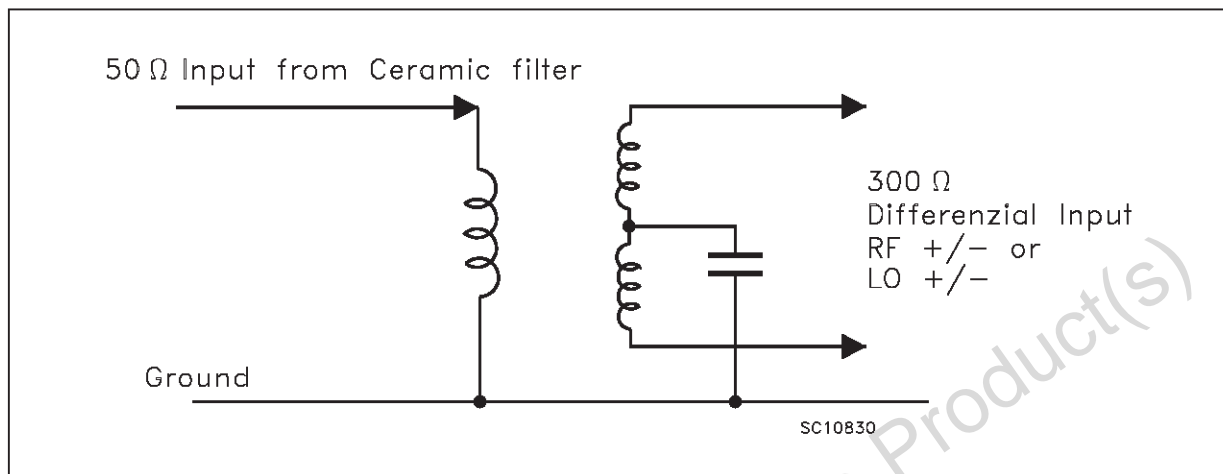
Fig. 1 Typical Application Circuit



### A.1 Matching Network

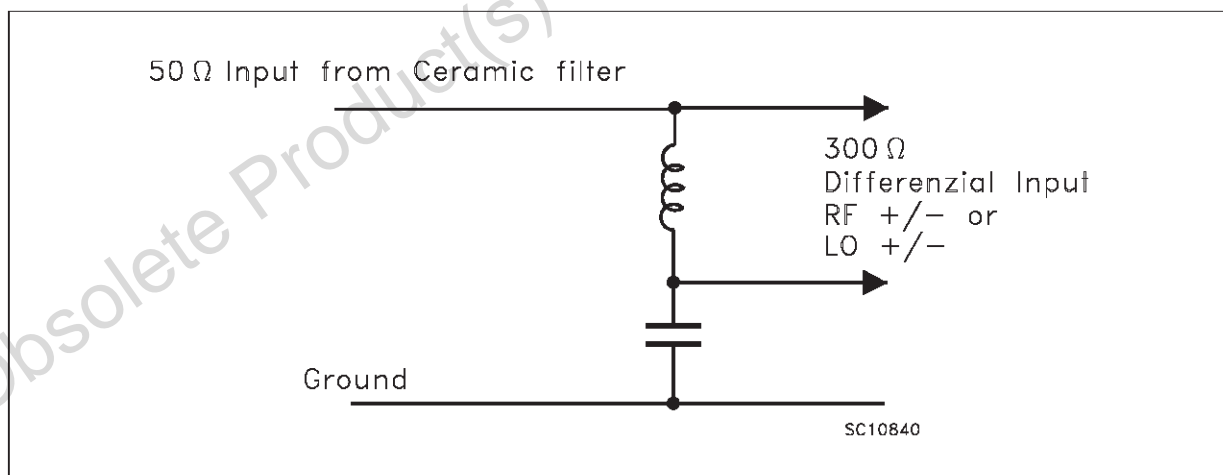
The **matching circuit** may be a 50 Ohm / 300 Ohm balun transformer (figure 2), but a more economical solution is a tuned match as shown below. A single 10nH inductor is optimal in cost, but may not meet the users tolerance requirements over spreads of silicon and pcb material, as it has only around 1pF tuning capacitance ( 2pF in series with 2pF inside the package).

Fig. 2 Matching Network with Balun



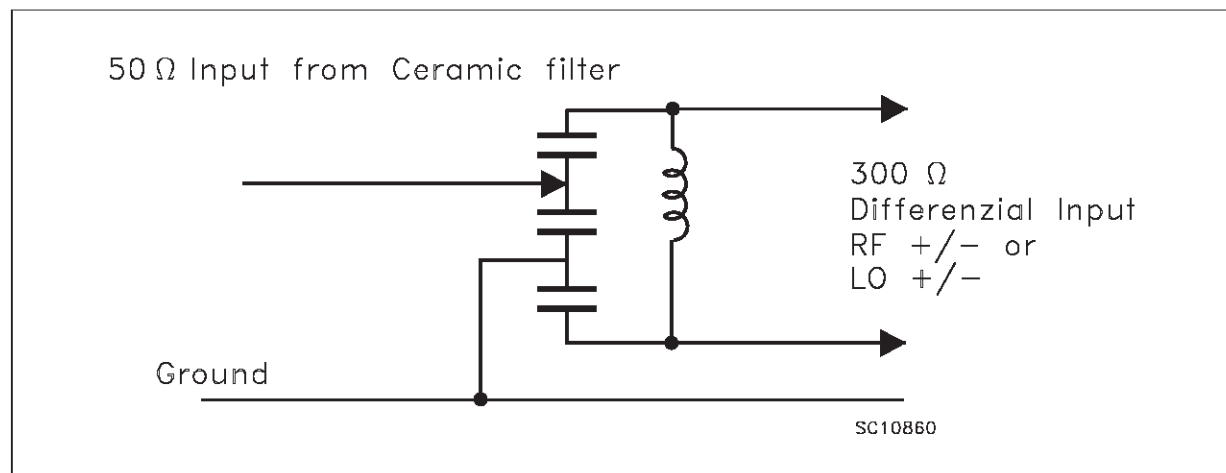
The first example (figure 3) increases the capacitance with a discrete capacitor, and uses a lower inductance value. Both examples assume that the ceramic filter is dc blocking, both input to output, and output to ground.

Fig. 3 Matching Network with two elements



The second (figure 4) example allows optimum matching by rationing the capacitors appropriately to achieve voltage gain commensurate with the impedance translation. While it has a higher component count, it is the version most tolerant of component variations and board capacitance.

Fig. 4 Matching Network with four elements



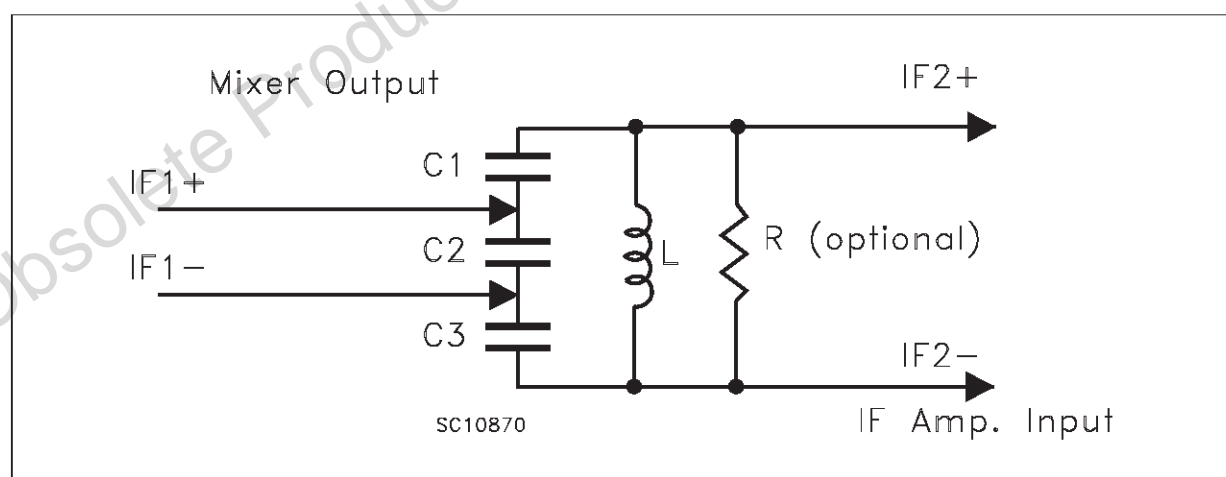
## A.2 IF Filter

The recommended **IF filter** is shown in figure 5. The stop band of the filter is to reject the alias images around 12MHz, and around 28MHz, where it should have at least 15dBc rejection.

Note that the mixer output is low impedance, (70 Ohms), and the IF input is high impedance (15kOhms), so considerable voltage gain is achieved in the impedance matching filter.

The filter also sets the bandwidth of the receiver, using the load impedance with the L/C ratio to set the filter Q. If desired, an external resistor may be added in parallel to reduce the Q. Note that the bandwidth must be much wider than the 2MHz needed to pass the power of the GPS signal... it must maintain linear phase across the 2MHz, even at the extremes of component tolerance.

Fig. 5 IF Filter



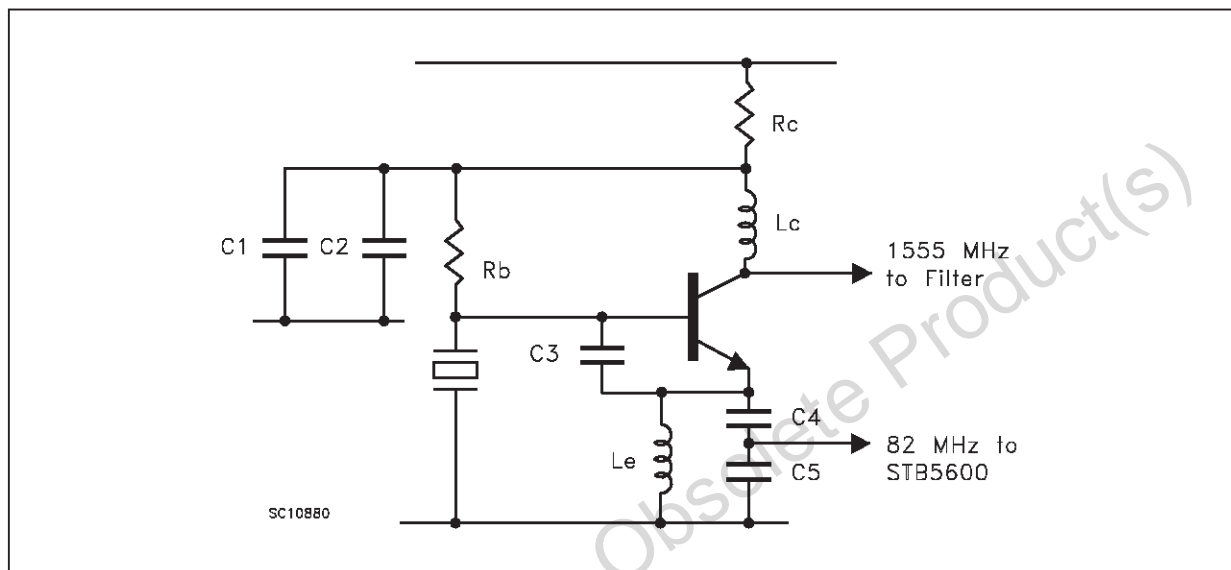
### A.3 Reference Oscillator

The recommended dual output oscillator shown in figure 6 generates both the 81.84MHz signal that is divided down for the CPU 16.368MHz clock, but also the low amplitude 1555MHz first local oscillator signal.

Note that some 2 volts of the 82MHz signal is available, and the capacitive tap on the tank circuit is used to reduce the amplitude to prevent excessive radiation.

Note that the transistor must be a high frequency type,  $F_t$  of 8 GHz or greater, and that the collector inductor must have a self resonant frequency of 2.5GHz or higher.

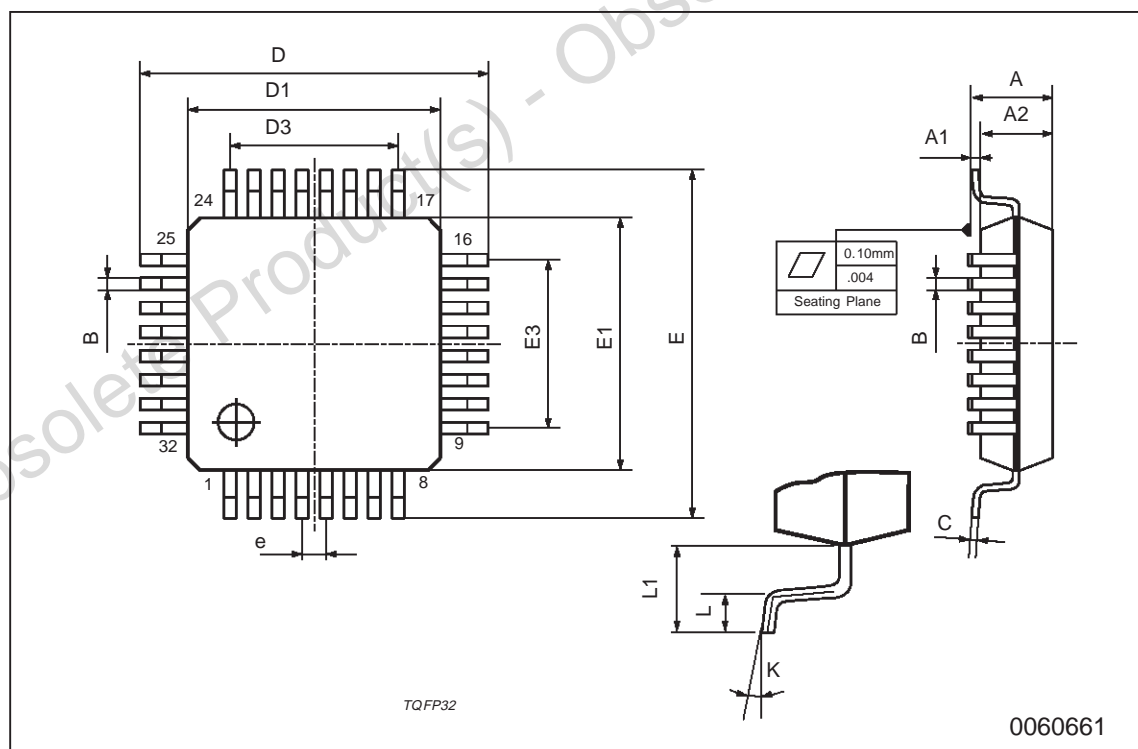
Fig. 6 Reference Oscillator





## TQFP32 MECHANICAL DATA

| DIM. | mm                 |      |      | inch  |       |       |
|------|--------------------|------|------|-------|-------|-------|
|      | MIN.               | TYP. | MAX. | MIN.  | TYP.  | MAX.  |
| A    |                    |      | 1.60 |       |       | 0.063 |
| A1   | 0.05               |      | 0.15 | 0.002 |       | 0.006 |
| A2   | 1.35               | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| B    | 0.30               | 0.37 | 0.45 | 0.012 | 0.015 | 0.018 |
| C    | 0.09               |      | 0.20 | 0.004 |       | 0.008 |
| D    |                    | 9.00 |      |       | 0.354 |       |
| D1   |                    | 7.00 |      |       | 0.276 |       |
| D3   |                    | 5.60 |      |       | 0.220 |       |
| e    |                    | 0.80 |      |       | 0.031 |       |
| E    |                    | 9.00 |      |       | 0.354 |       |
| E1   |                    | 7.00 |      |       | 0.276 |       |
| E3   |                    | 5.60 |      |       | 0.220 |       |
| L    | 0.45               | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1   |                    | 1.00 |      |       | 0.039 |       |
| K    | 0°(min.), 7°(max.) |      |      |       |       |       |



Obsolete Product(s) - Obsolete Product(s)

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

© 1998 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.