



STB50NE10

N-channel 100V - 0.021 Ω - 50A - D²PAK
STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STB50NE10	100V	<0.027 Ω	50A

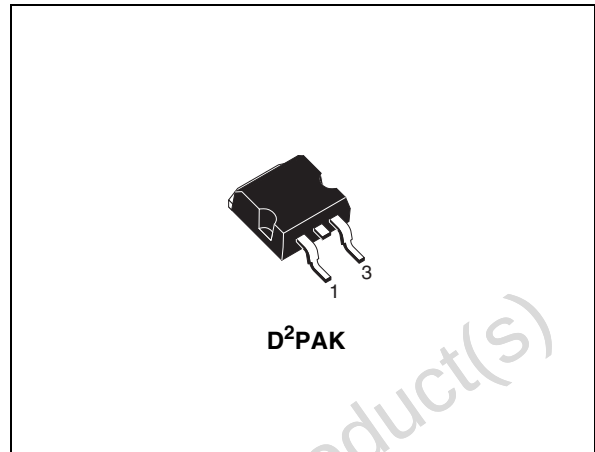
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge at 100 °C
- Application oriented characterization

Description

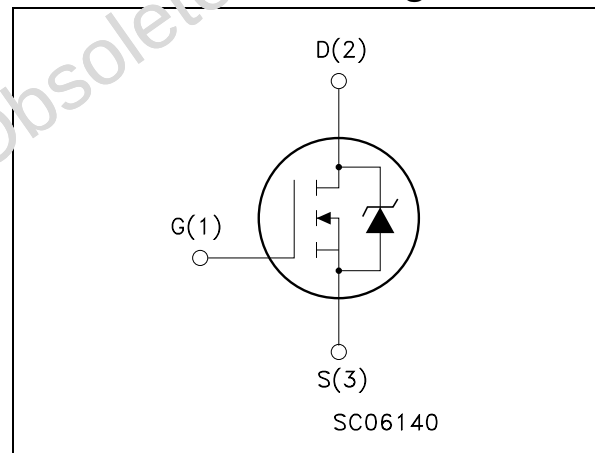
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB50NE10T4	B50NE10	D ² PAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	100	V
V_{GS}	Gate- source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	50	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	35	A
$I_{DM}^{(1)}$	Drain current (pulsed)	200	A
P_{tot}	Total dissipation at $T_C = 25^\circ\text{C}$	180	W
	Derating Factor	1.2	W/ $^\circ\text{C}$
dv/dt	Peak diode recovery voltage slope	6	V/ns
T_{stg}	Storage temperature	-65 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.

Table 2. Thermal data

$R_{thj-case}$	Thermal resistance junction-case max	0.83	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C/W}$
$R_{thj-sink}$	Thermal resistance case-sink max	0.5	$^\circ\text{C/W}$
T_J	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	50	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	300	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250μA, V _{GS} = 0	100			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 25A		0.021	0.027	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} =V _{DS} >I _{D(on)} ×R _{DS(on)} max, I _D = 20A	20	35		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1MHz, V _{GS} = 0		4350 500 175	6000	pF pF pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	V _{DD} = 50V, I _D = 25A R _G = 4.7Ω V _{GS} = 10V (see Figure 12)		25 100 45 35		ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 80V, I _D = 50A, V _{GS} = 10V, R _G = 4.7Ω (see Figure 13)		123 24 47	166	nC nC nC

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				50 200	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 50A$, $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 50A$, $di/dt = 100A/\mu s$, $V_{DD} = 30V$, $T_j = 150^\circ C$ (see Figure 14)		155 815 10.5		ns nC A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

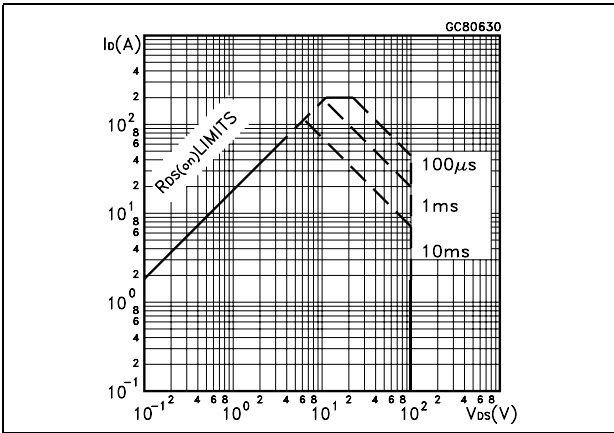


Figure 2. Thermal impedance

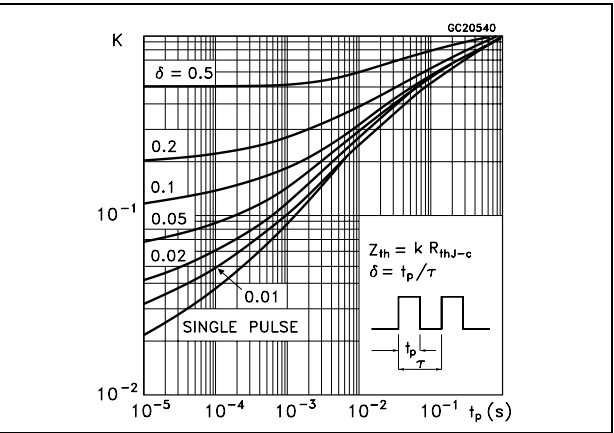


Figure 3. Output characteristics

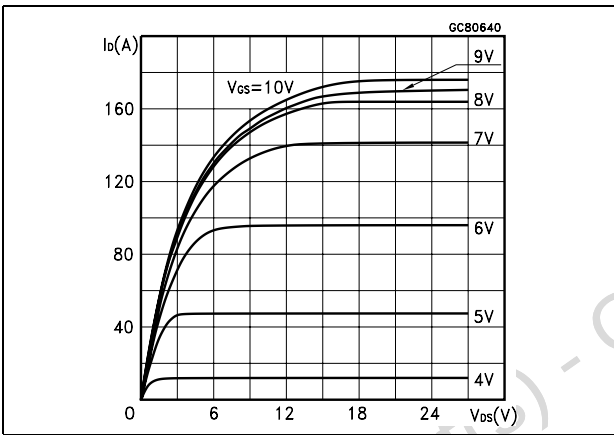


Figure 4. Transfer characteristics

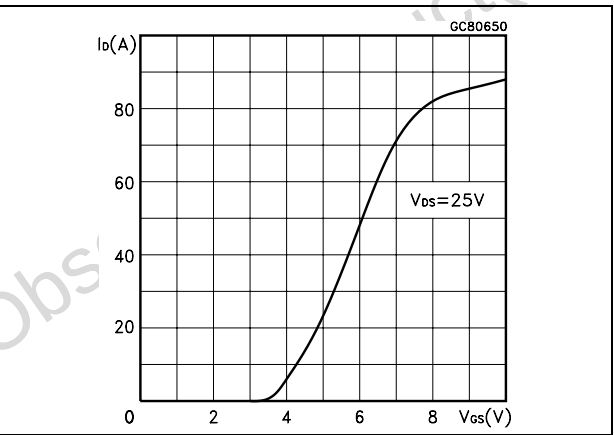


Figure 5. Transconductance

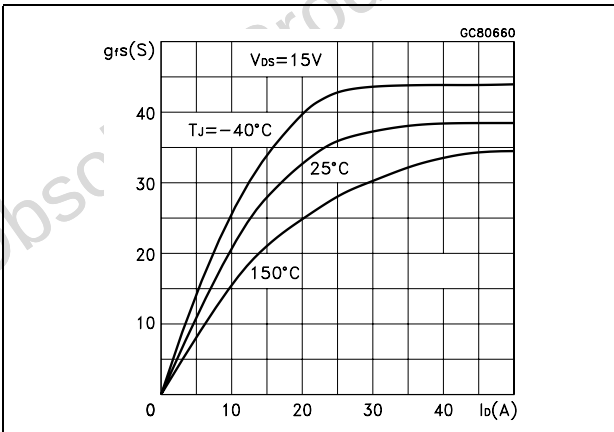


Figure 6. Static drain-source on resistance

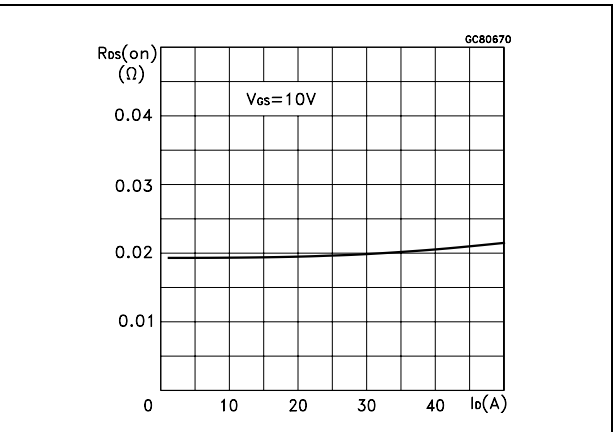


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

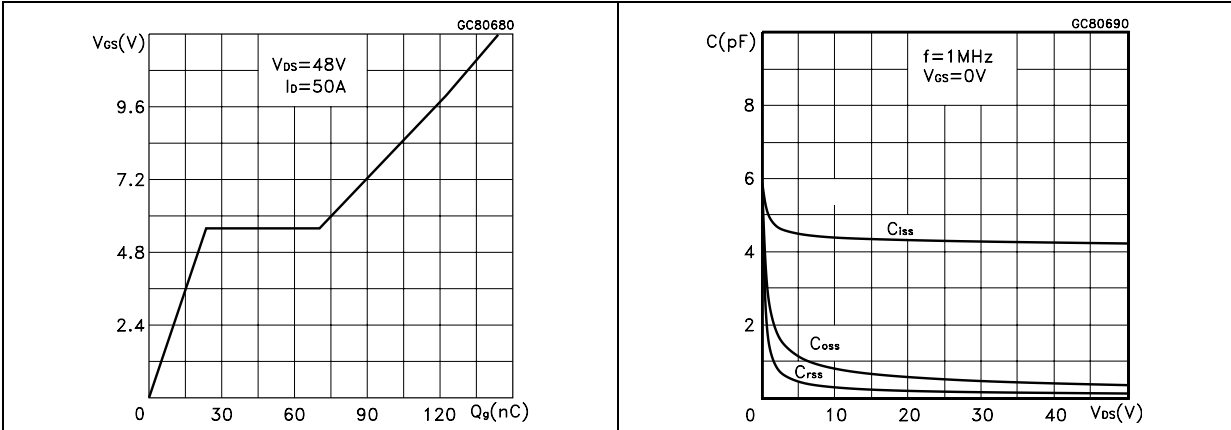


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

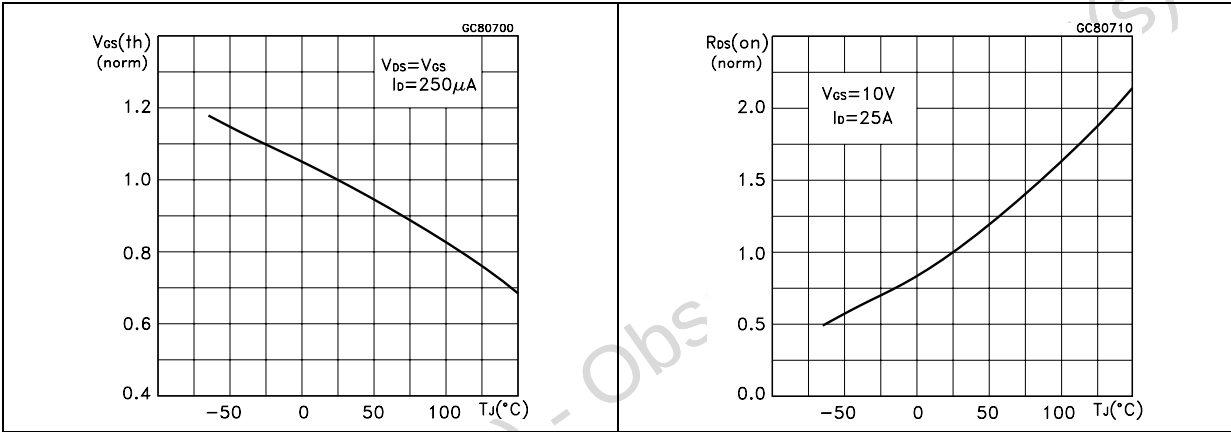
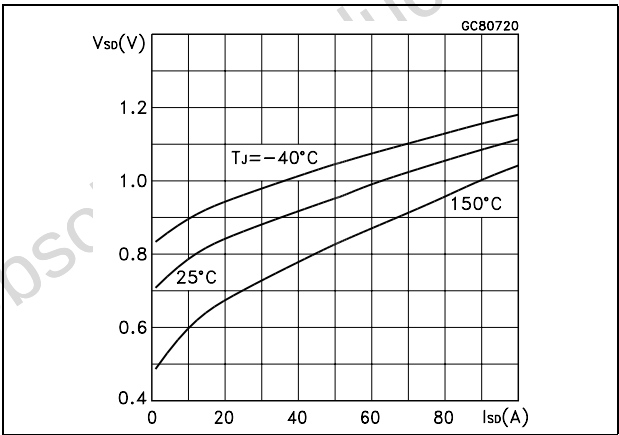


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

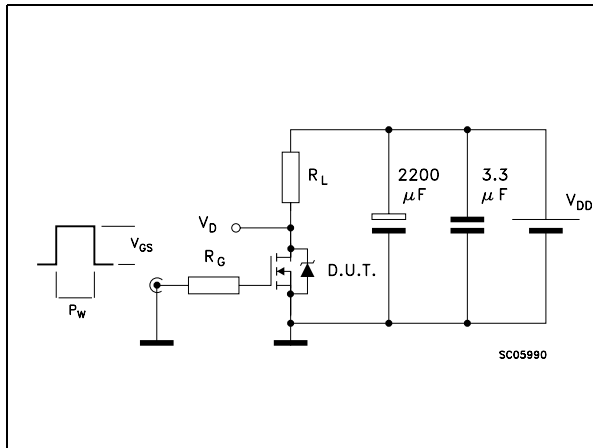


Figure 13. Gate charge test circuit

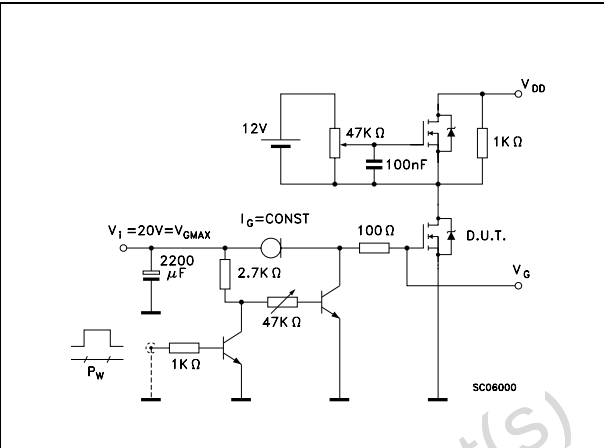


Figure 14. Test circuit for inductive load switching and diode recovery times

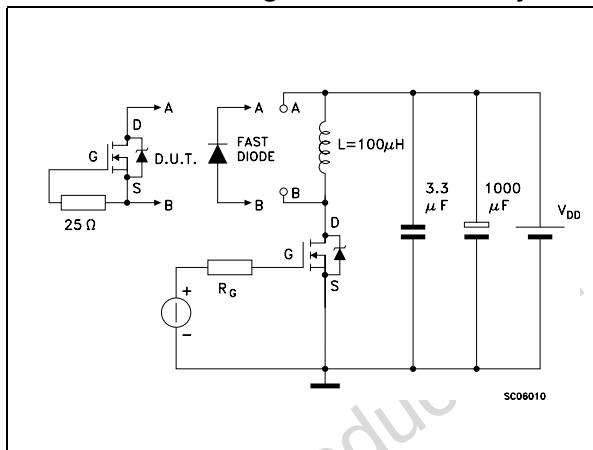


Figure 15. Unclamped Inductive load test circuit

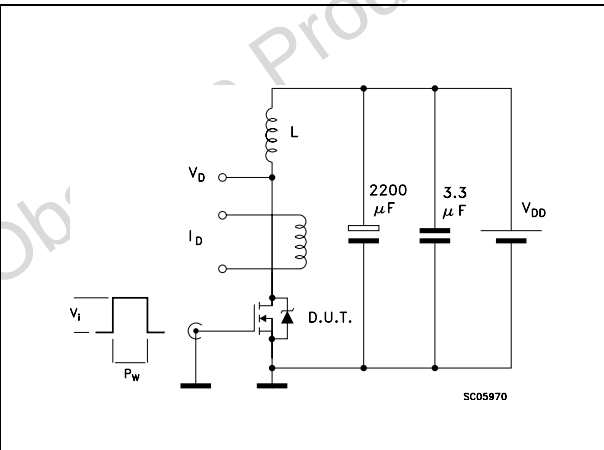


Figure 16. Unclamped inductive waveform

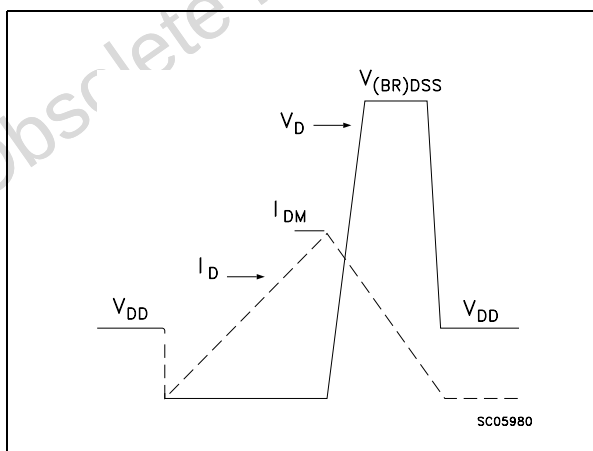
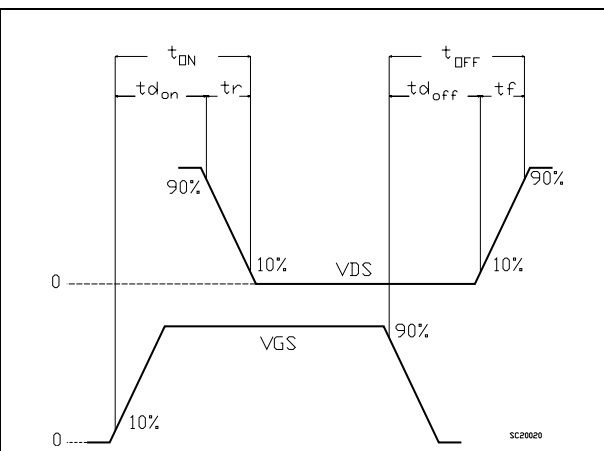


Figure 17. Switching time waveform



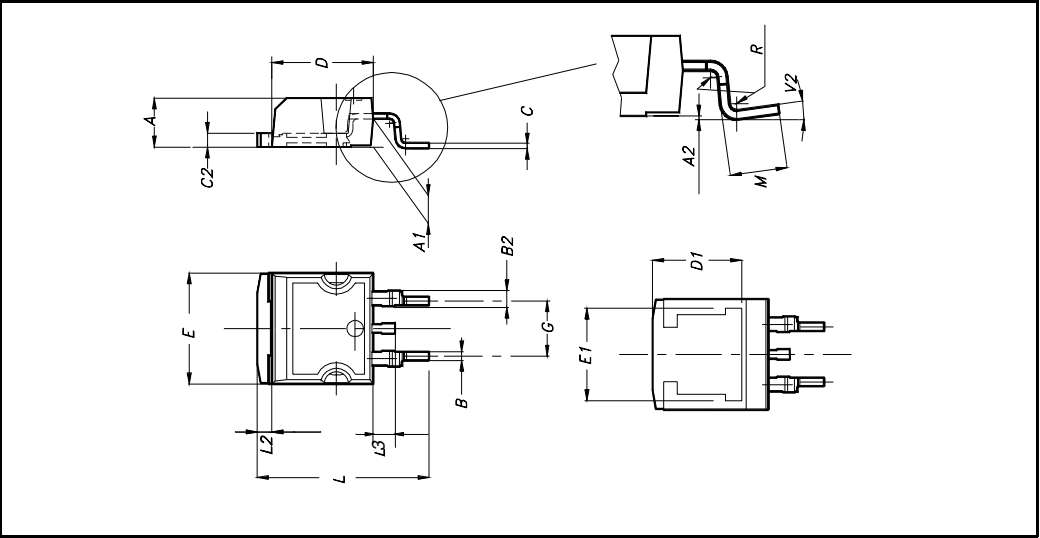
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) - Obsolete Product(s)

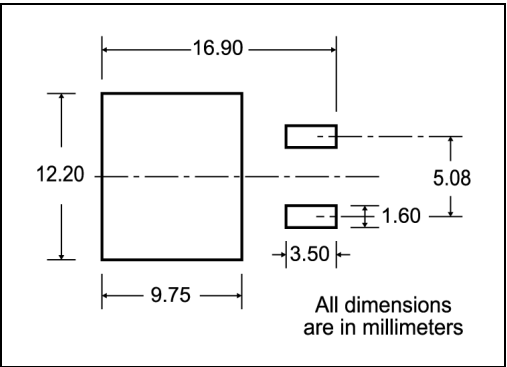
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

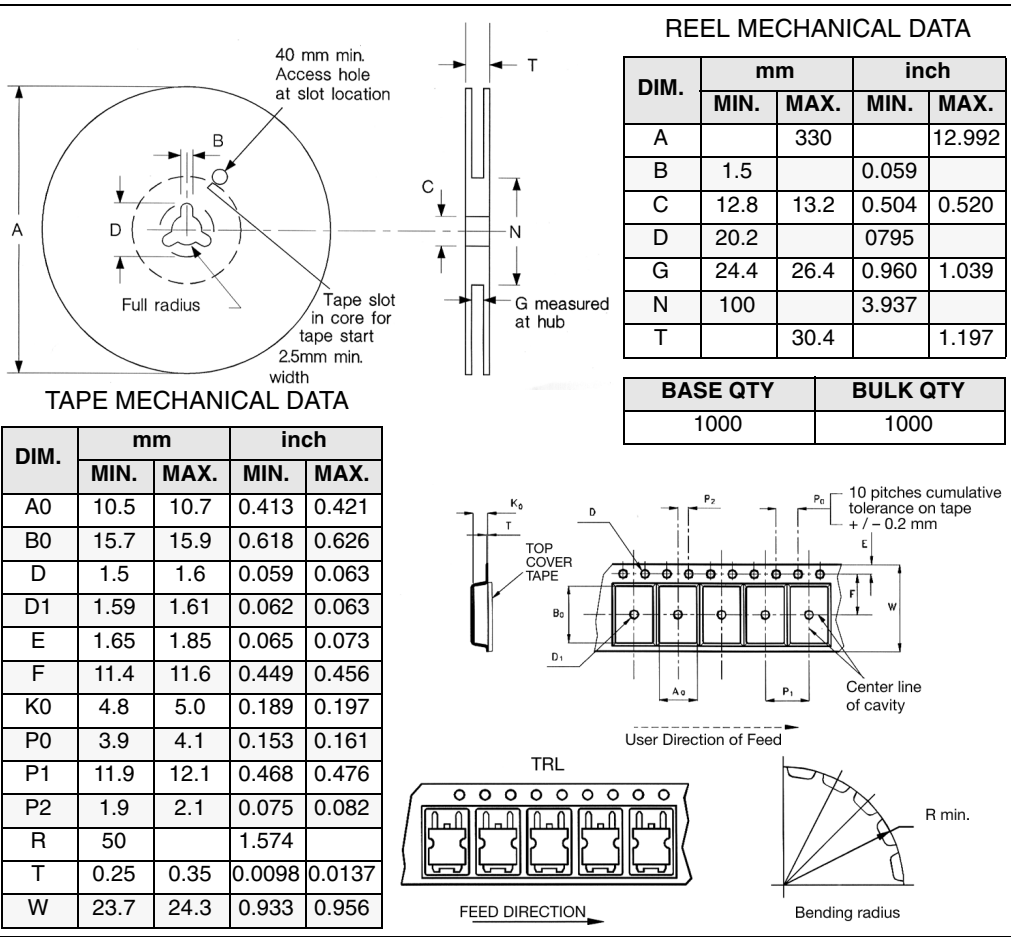


5 Packing mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jun-2004	4	Complete version
26-Jun-2006	5	New template, no content change

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