



STB20NM60D

N-channel 600V - 0.26Ω - 20A - D²PAK
FDmesh™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STB20NM60D	600V	<0.29Ω	20A	45W

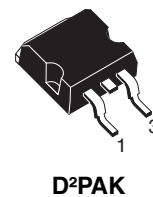
- High dv/dt and avalanche capabilities
- 100% Avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Tight process control and high manufacturing yields

Description

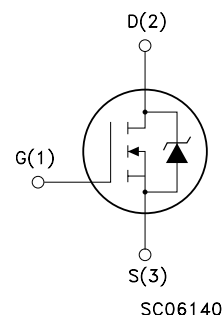
The FDmesh™ associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB20NM60D	B20NM60D	D ² PAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	600	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	600	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	20	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	12.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	80	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	192	W
	Derating factor	1.20	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	20	V/ns
T_j	Operating junction temperature	– 65 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature		$^\circ\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 20\text{A}$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DD} = 80\%V_{(BR)DSS}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	0.65	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	10	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 35\text{ V}$)	700	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 30\text{V}$			± 10 0	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 10\text{A}$		0.26	0.29	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 10\text{A}$		9		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		1300		pF
C_{oss}	Output capacitance			500		pF
C_{rss}	Reverse transfer capacitance			35		pF
$C_{oss\ eq.}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V to } 480\text{V}$		190		pF
R_G	Gate input resistance	$f=1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20mV open drain		2.7		Ω
Q_g	Total gate charge	$V_{DD} = 480\text{V}$, $I_D = 20\text{A}$, $V_{GS} = 10\text{V}$ (see Figure 13)		37	52	nC
Q_{gs}	Gate-source charge			10		nC
Q_{gd}	Gate-drain charge			17		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300V, I_D = 10A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 12)		25		ns
t_r	Rise time			12		ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD} = 480V, I_D = 20A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 12)		8		ns
t_f	Fall time			22		ns
t_c	Cross-over time			30		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				80	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20A, V_{GS} = 0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 20A, T_j = 25^\circ C$ $di/dt = 100A/\mu s, V_{DD} = 60V$ (see Figure 17)		240		ns
Q_{rr}	Reverse recovery charge			1800		nC
I_{RRM}	Reverse recovery current			16		A
t_{rr}	Reverse recovery time	$I_{SD} = 20A, T_j = 150^\circ C$ $di/dt = 100A/\mu s, V_{DD} = 60V$ (see Figure 17)		396		ns
Q_{rr}	Reverse recovery charge			2960		nC
I_{RRM}	Reverse recovery current			20		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

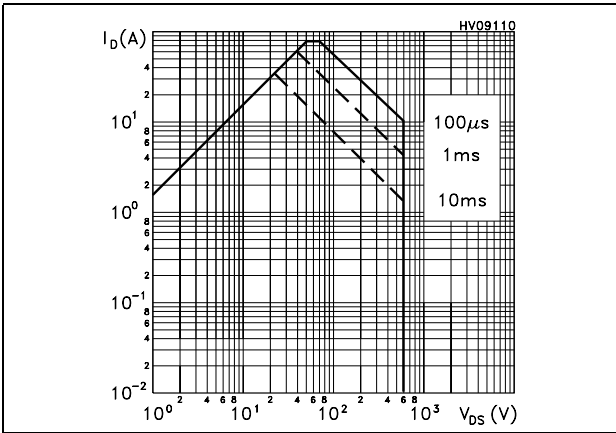


Figure 2. Thermal impedance

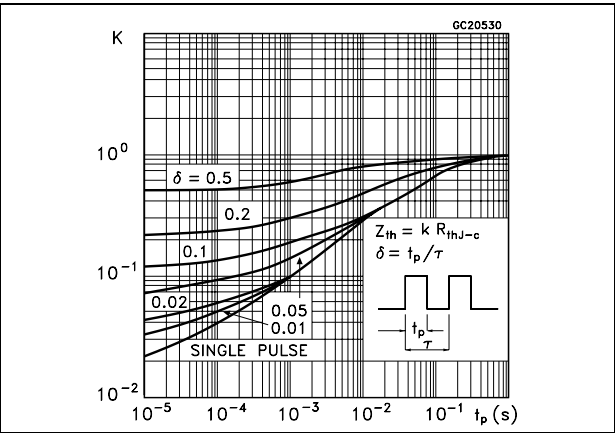


Figure 3. Output characteristics

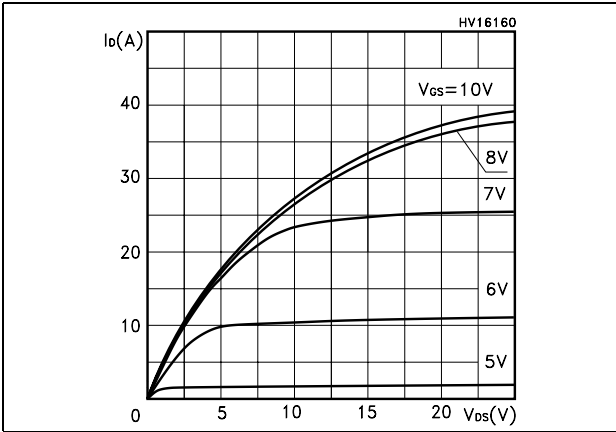


Figure 4. Transfer characteristics

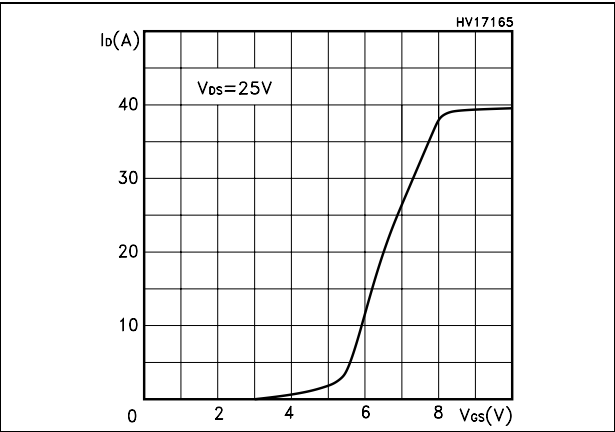


Figure 5. Transconductance

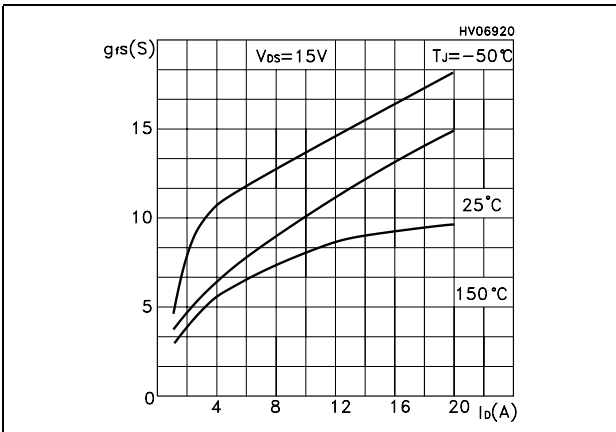


Figure 6. Static drain-source on resistance

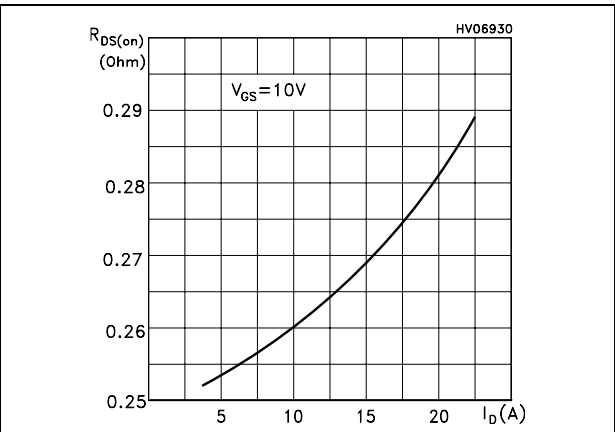


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

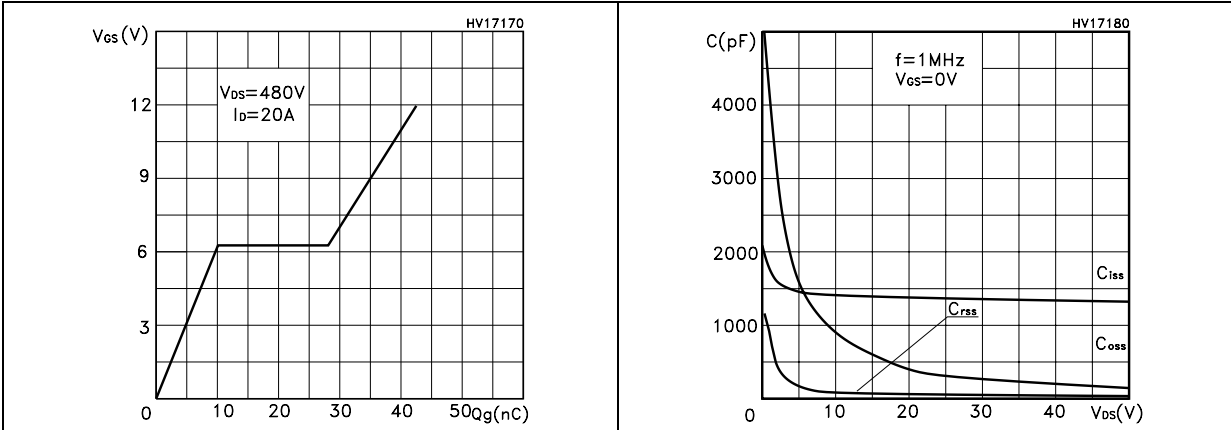


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

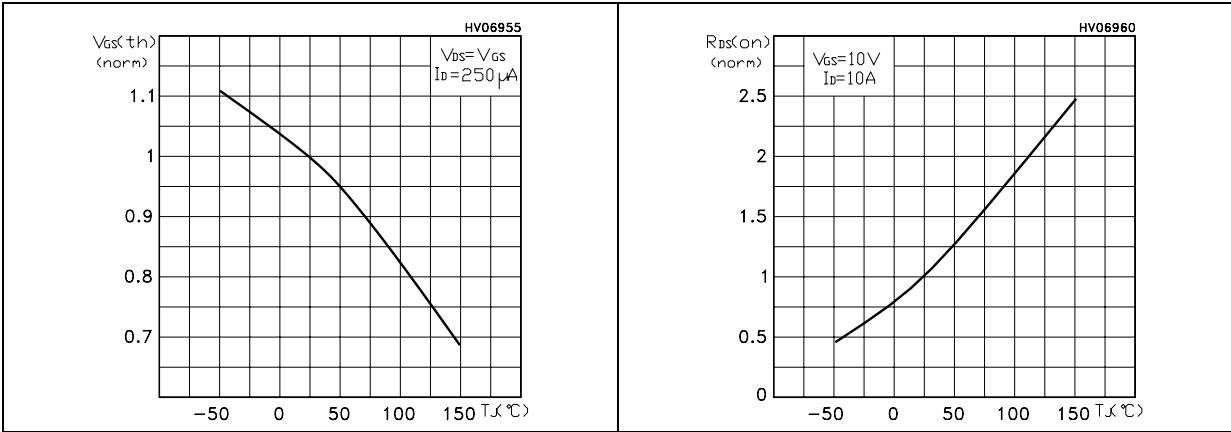
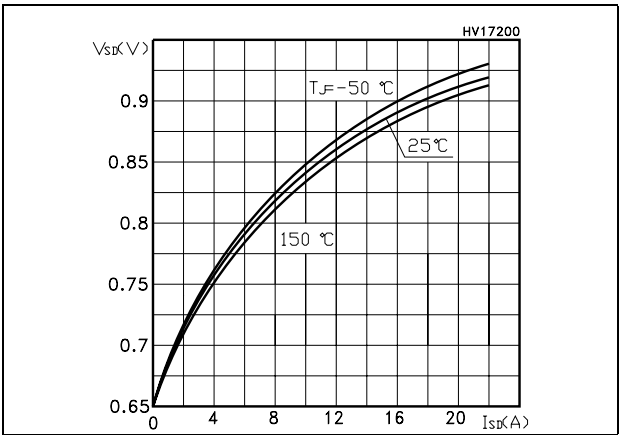


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load



Figure 13. Gate charge test circuit

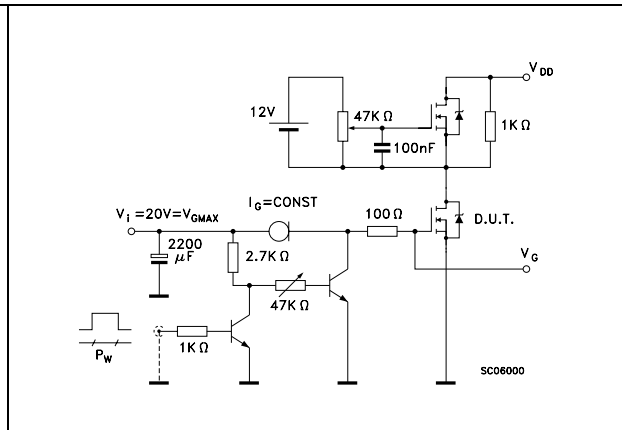


Figure 14. Test circuit for inductive load switching and diode recovery times

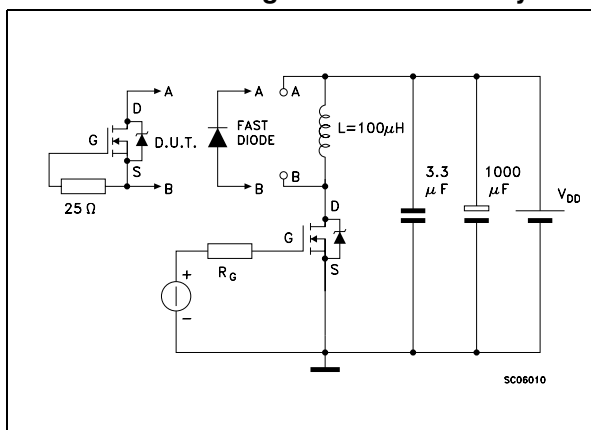


Figure 15. Unclamped inductive load test circuit

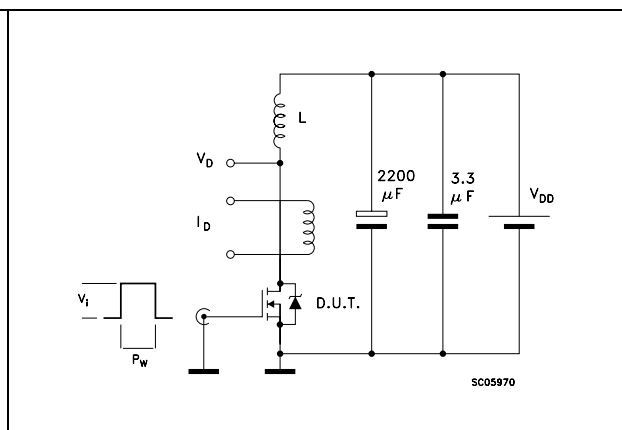


Figure 16. Unclamped inductive waveform

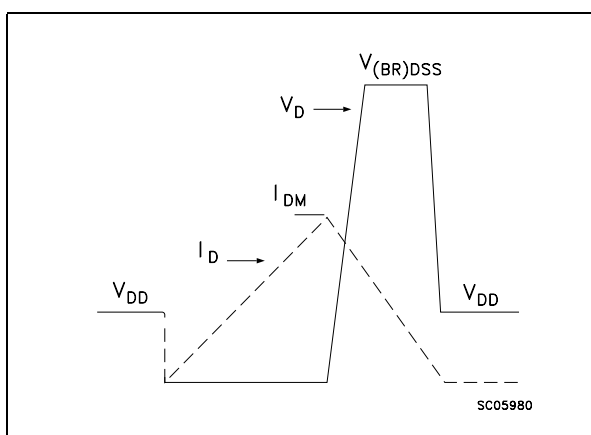
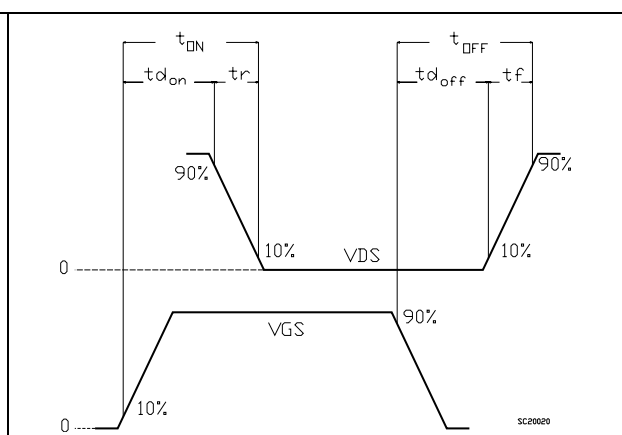


Figure 17. Switching time waveform

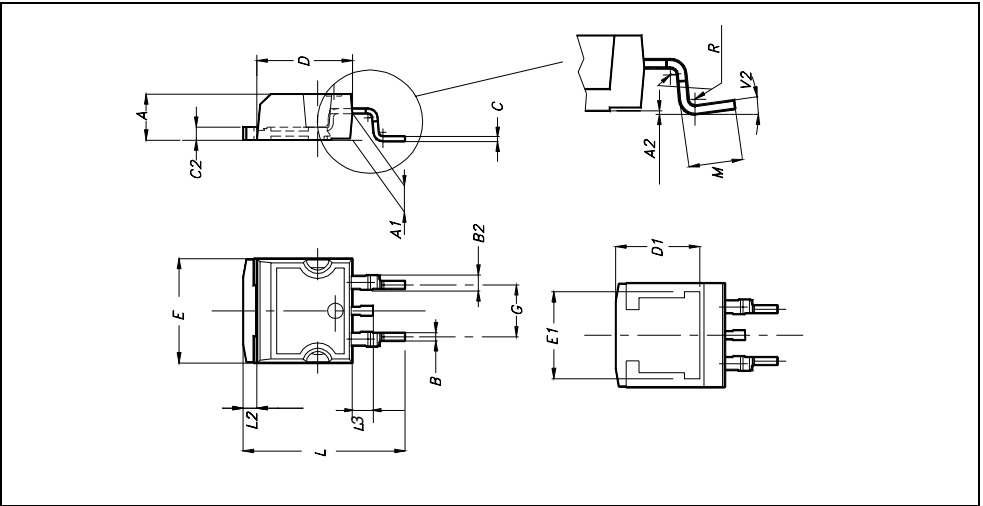


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

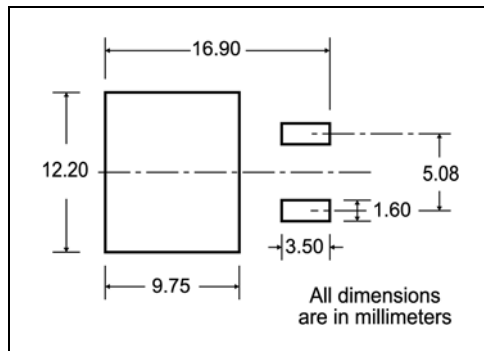
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

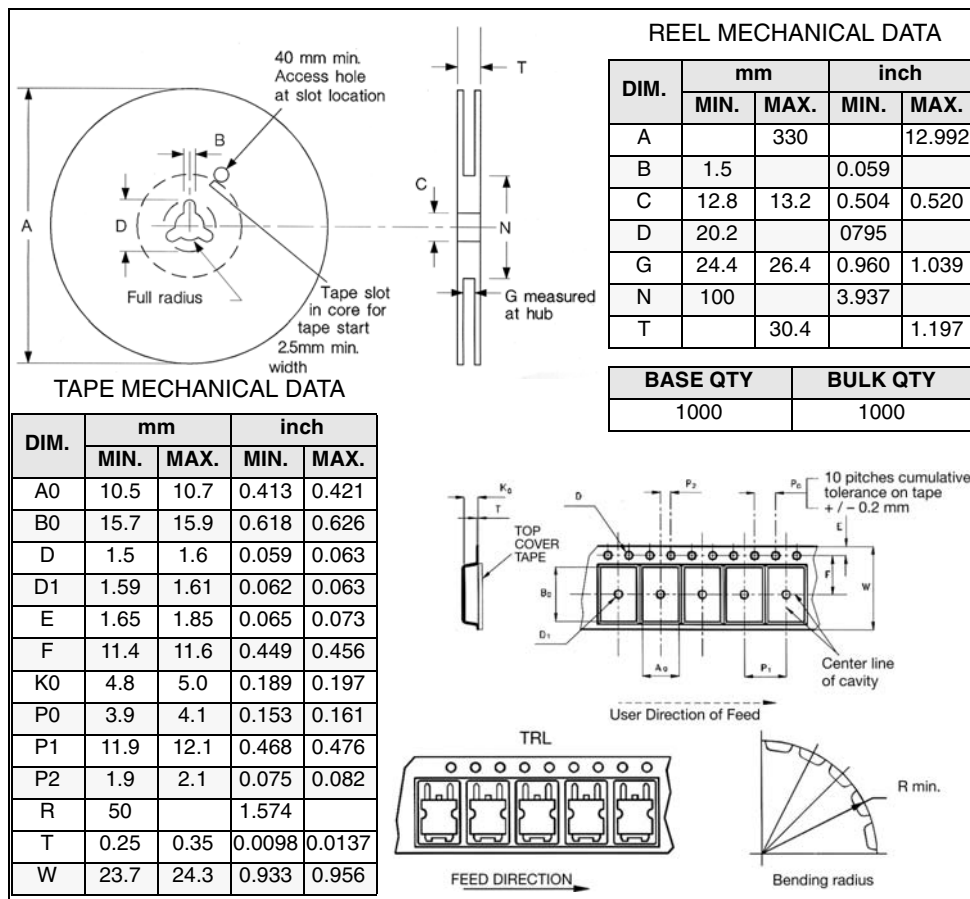


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 8. Revision history

Date	Revision	Changes
08-Jun-2006	1	First release

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