



STB16NF06L

N-channel 60V - 0.07 Ω - 16A - D²PAK
STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STB16NF06L	60V	<0.09 Ω	16A

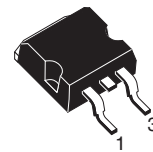
- Exceptional dv/dt capability
- Low gate charge at 100°C
- Logic level device
- Low threshold drive

Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

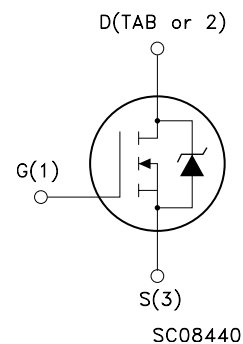
Applications

- Switching application



D²PAK

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB16NF06L	B16NF06L	D ² PAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	60	V
V_{GS}	Gate- source voltage	± 16	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	16	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	11	A
$I_{DM}^{(1)}$	Drain current (pulsed)	64	A
P_{tot}	Total dissipation at $T_C = 25^\circ\text{C}$	45	W
	Derating Factor	0.3	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery avalanche energy	23	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	127	mJ
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 6\text{A}$, $di/dt \leq 10\text{A}/\mu\text{s}$, $V_{DD} = V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
3. Starting $T_j = 25^\circ\text{C}$, $I_D = 8\text{A}$, $V_{DD} = 30\text{V}$

Table 2. Thermal data

$R_{thj-case}$	Thermal resistance junction-case max	3.33	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_J	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 5\text{V}$, $I_D = 8\text{A}$ $V_{GS} = 10\text{V}$, $I_D = 8\text{A}$		0.08 0.07	0.10 0.09	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 80\text{A}$		17		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		345 72 29		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 30\text{V}$, $I_D = 8\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{V}$ (see Figure 12)		10 37 20 12.5		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 48\text{V}$, $I_D = 16\text{A}$, $V_{GS} = 4.5\text{V}$, $R_G = 4.7\Omega$ (see Figure 13)		7.3 2.1 3.1	10	nC nC nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				16 64	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 16A$, $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 16A$, $di/dt = 100A/\mu s$, $V_{DD} = 16V$, $T_j = 150^\circ C$ (see Figure 14)		50 67.5 2.7		ns nC A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

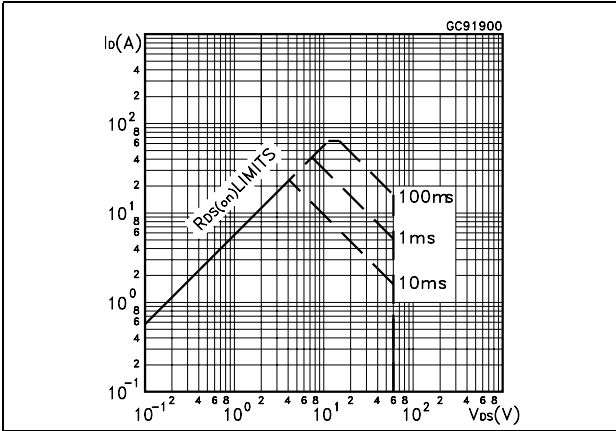


Figure 2. Thermal impedance

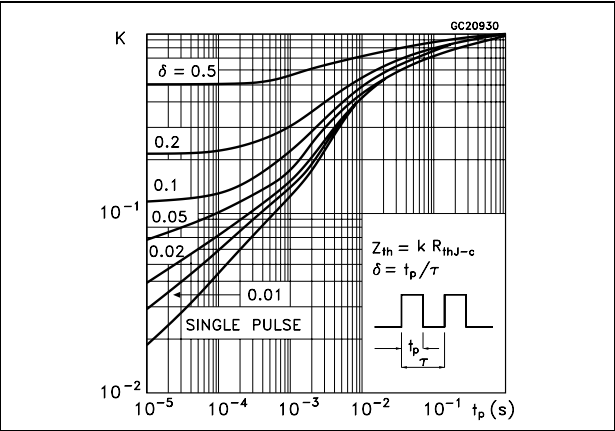


Figure 3. Output characteristics

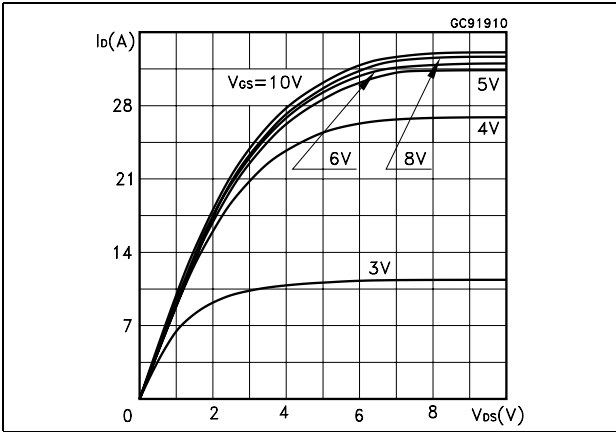


Figure 4. Transfer characteristics

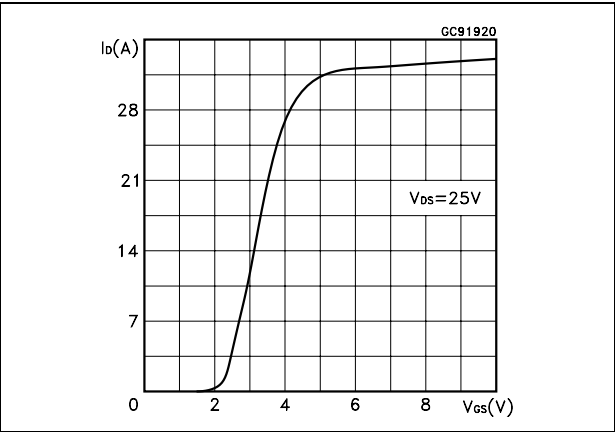


Figure 5. Transconductance

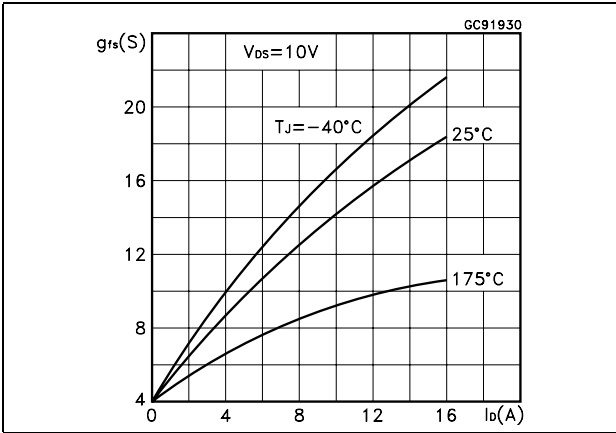


Figure 6. Static drain-source on resistance

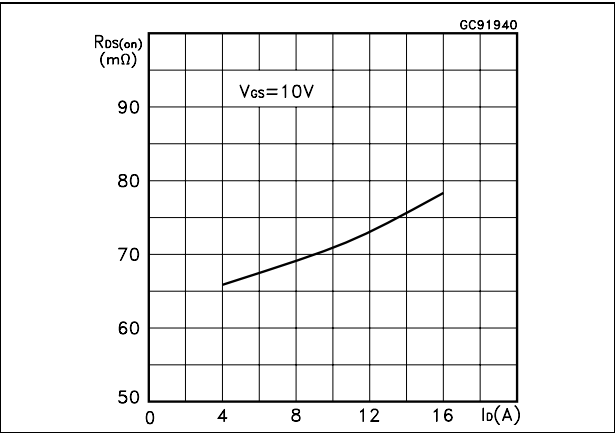


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

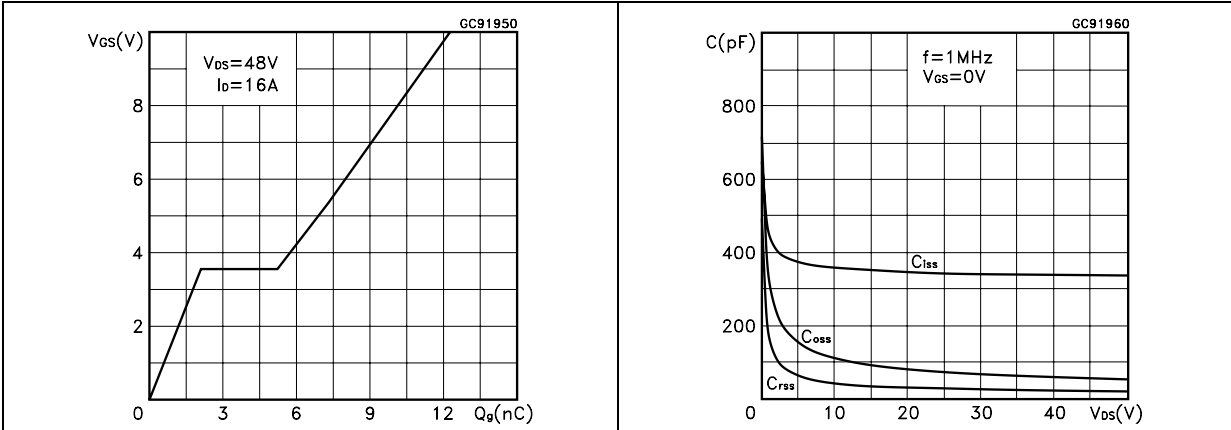


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

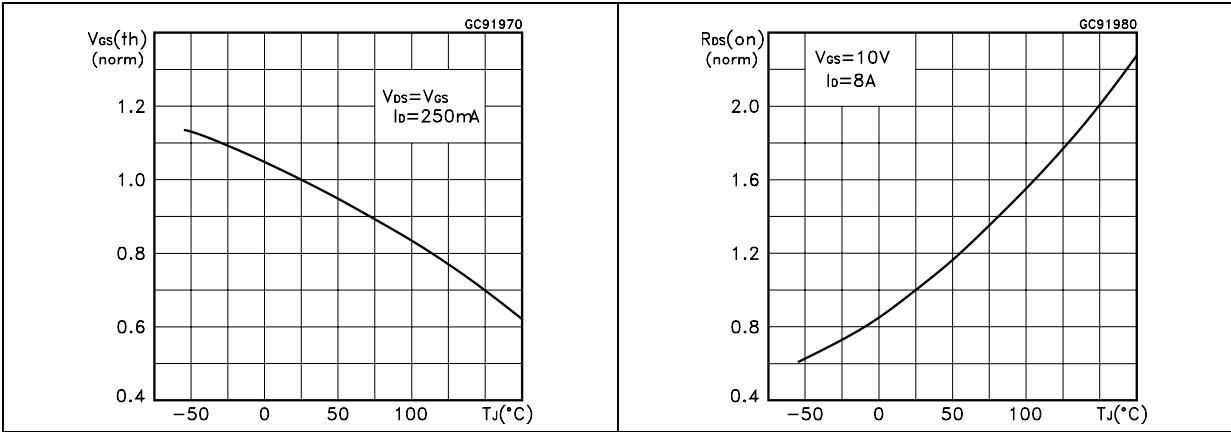
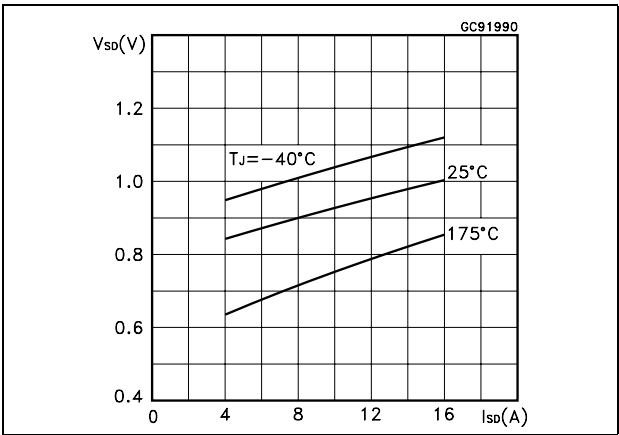


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load



Figure 13. Gate charge test circuit

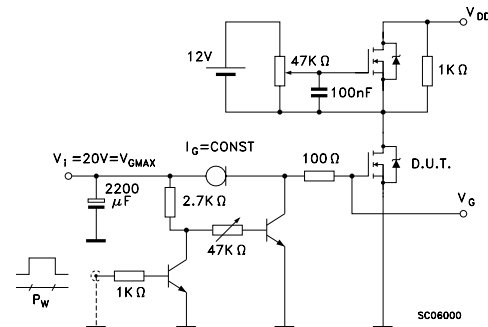


Figure 14. Test circuit for inductive load switching and diode recovery times

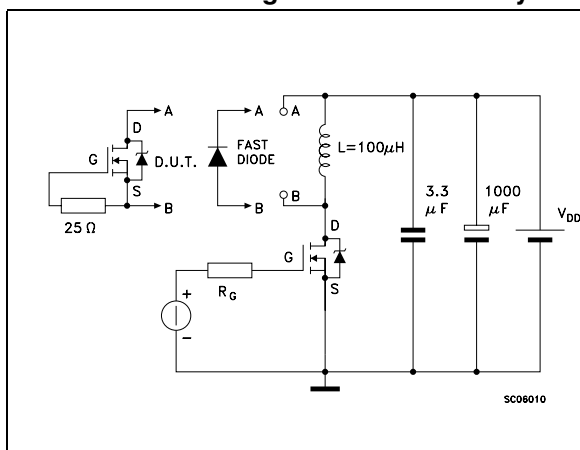


Figure 15. Unclamped Inductive load test circuit

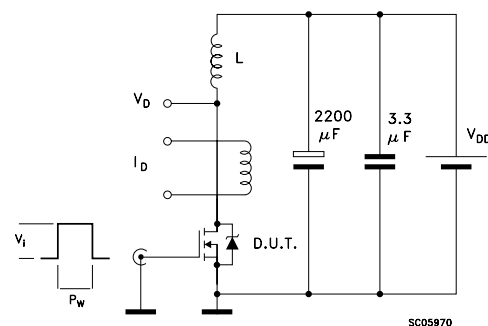
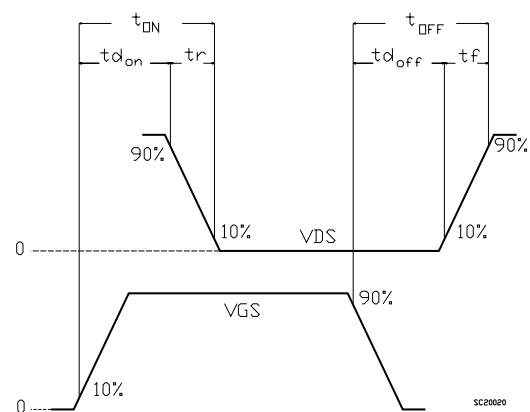


Figure 16. Unclamped inductive waveform



Figure 17. Switching time waveform

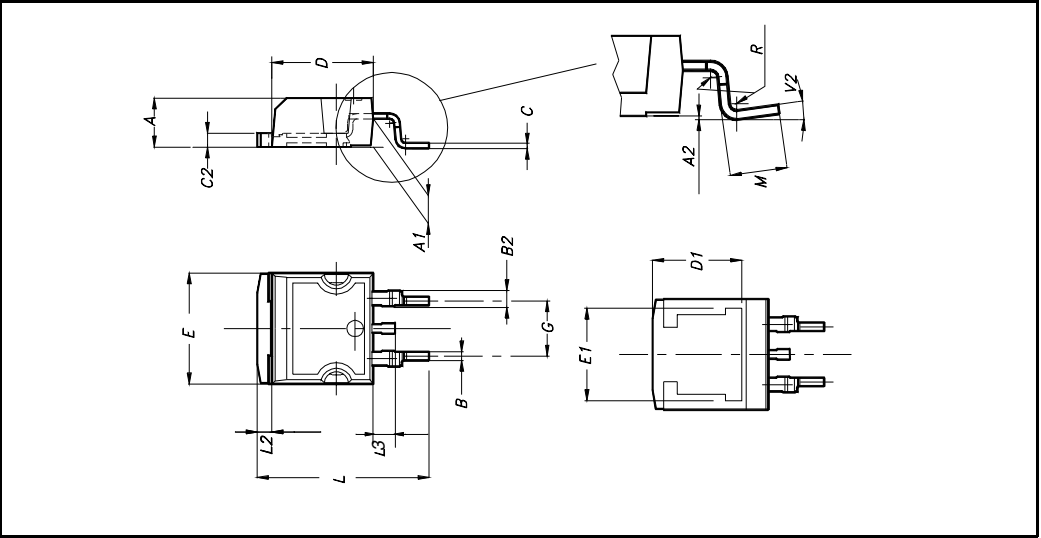


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

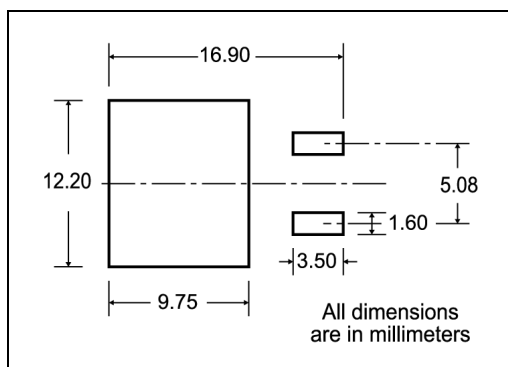
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

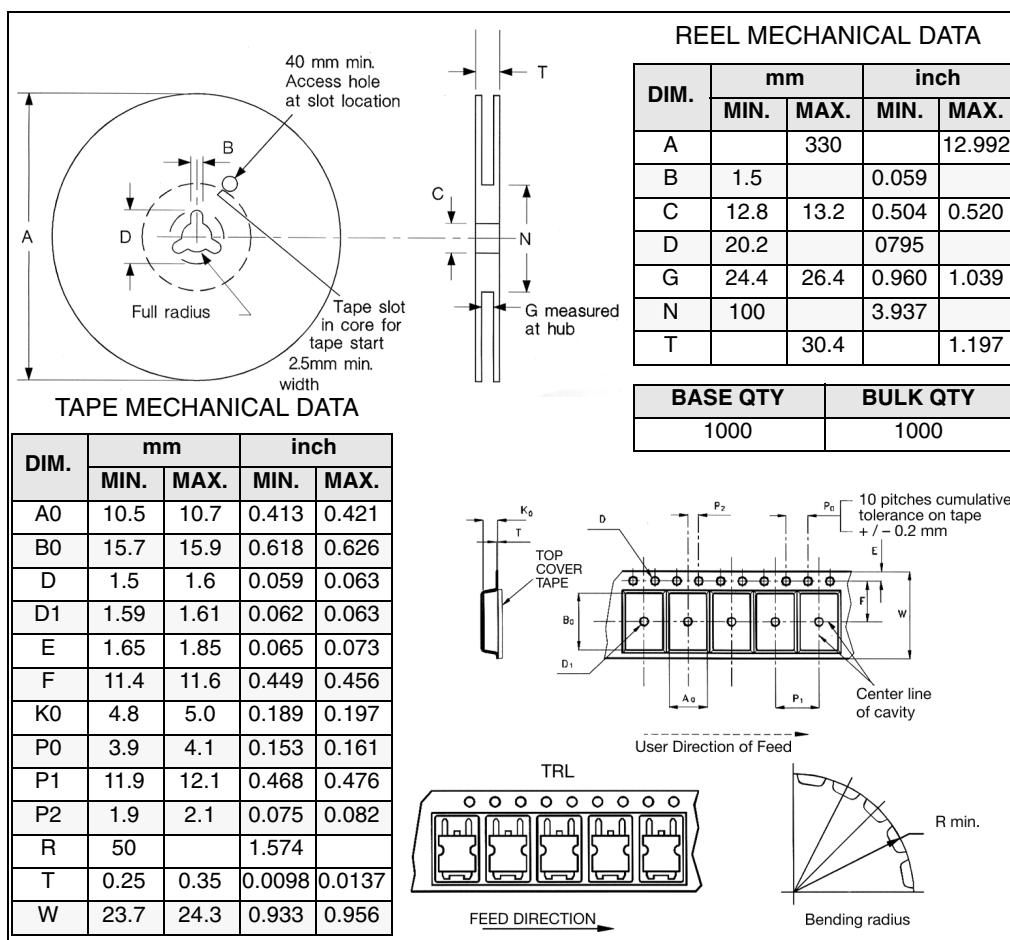


5 Packing mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 6. Revision history

Date	Revision	Changes
21-Jun-2004	1	First version
26-Jun-2006	2	New template, no content change

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