

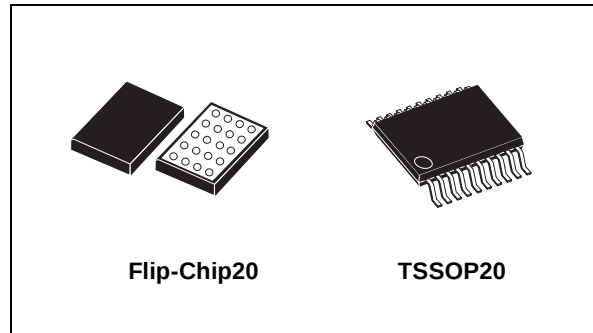


ST2378E

8-bit dual supply 1.71V to 5.5V level translator
with I/O $V_{CC} \pm 15KV$ ESD protection

General features

- High speed:
 - $t_{PD} = 15ns$ (Max.) at $T_A = 85^\circ C$
 - $V_L = 1.8V$
 - $V_{CC} = 5.5V$
- Guaranteed data rate:
 - 13Mbps ($1.8V \leq V_L \leq V_{CC} \leq 5.5V$)
- Low power dissipation:
 - $I_{TS-VL} = I_{TS-VCC} = 1\mu A$ (Max.) at $T_A = 85^\circ C$
 - $I_{QVL} = 100\mu A$ (Max.) at $T_A = 85^\circ C$
 - $I_{QCC} = 10\mu A$ (Max.) at $T_A = 85^\circ C$
- Output impedance:
 - $|I_{OHA}| = 20\mu A$ (Min.) at $V_L = 1.8V$; $V_{CC} = 5.5V$
 - $I_{OLA} = 1.0\mu A$ (Min.) at $V_L = 1.8V$ $V_{CC} = 5.5V$
- Bi-directional level translation
- Totem pole and open drain driving for I²C communications
- 5V tolerant on enable pin
- Wide operating voltage range:
 - $V_L(Opr) = 1.71V$ to V_{CC}
 - $V_{CC}(Opr) = 1.71V$ to $5.5V$
- ESD performance
- HBM > 15KV ESD protection on I/OV_{CC} lines
- Leadfree Flip-Chip and TSSOP packages



Description

The ST2378E is an 8-bit, dual supply, bi-directional level translator with $\pm 15kV$ ESD-protection on I/Os at V_{CC} side. It is designed to interface data transfer between low-voltage ASICs/PLDs and higher voltage systems. Externally applied voltage, V_{CC} and V_L , set logic levels at both sides with range specified as $1.71V \leq V_L \leq 5.5V$ and $V_L \leq V_{CC} \leq 5.5V$. For proper operation, V_{CC} should be set higher than V_L .

Utilizing a transmission-gate-based design, this device allows bi-directional asynchronous data transfer, which means each channel is allowed to have either V_{CC} to V_L or V_L to V_{CC} data transfer direction independently and no direction pin is required. ST2378E operates at guaranteed data rate of 13Mbps over the entire specified operating voltage range.

Among the other features is included the OE pin which allows disable-mode operation whereby current consumption is reduced to less than $1\mu A$.

Order codes

Part number	Temperature range	Package	Comments
ST2378EBJR	-40 to 85 °C	Flip-Chip20 (Tape and Reel)	3000 parts per reel
ST2378ETTR	-40 to 85 °C	TSSOP20 (Tape and Reel)	2500 parts per reel

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1 Block diagram

Figure 1. Block diagram

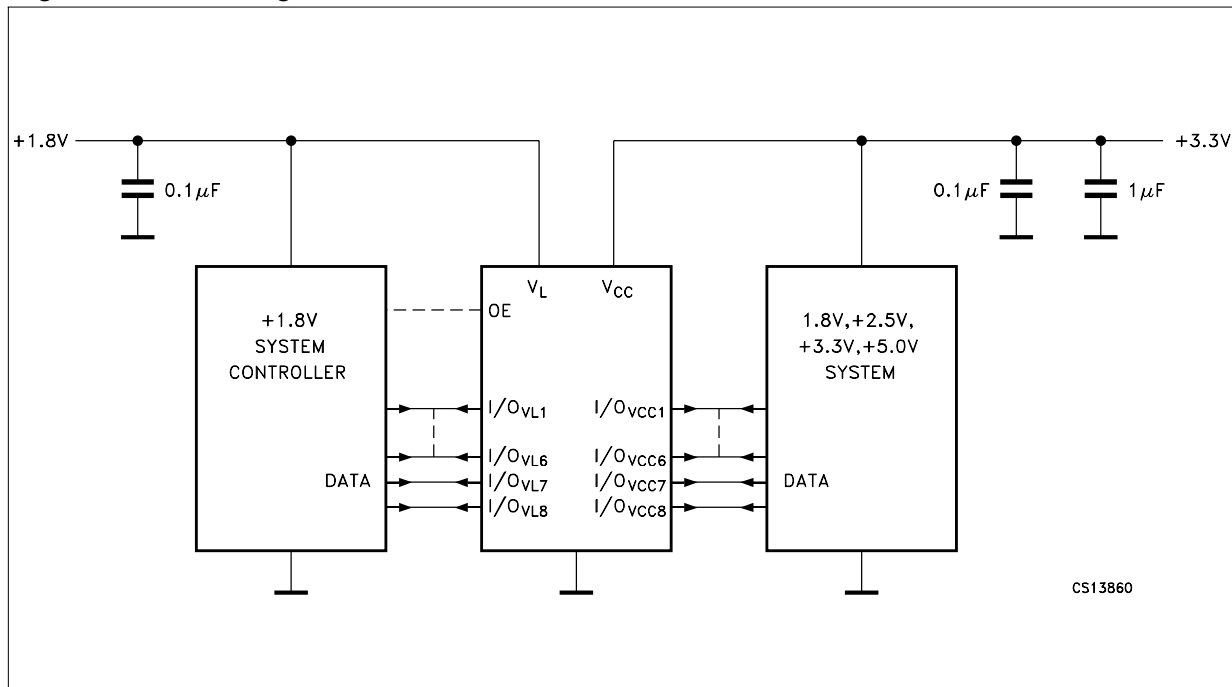
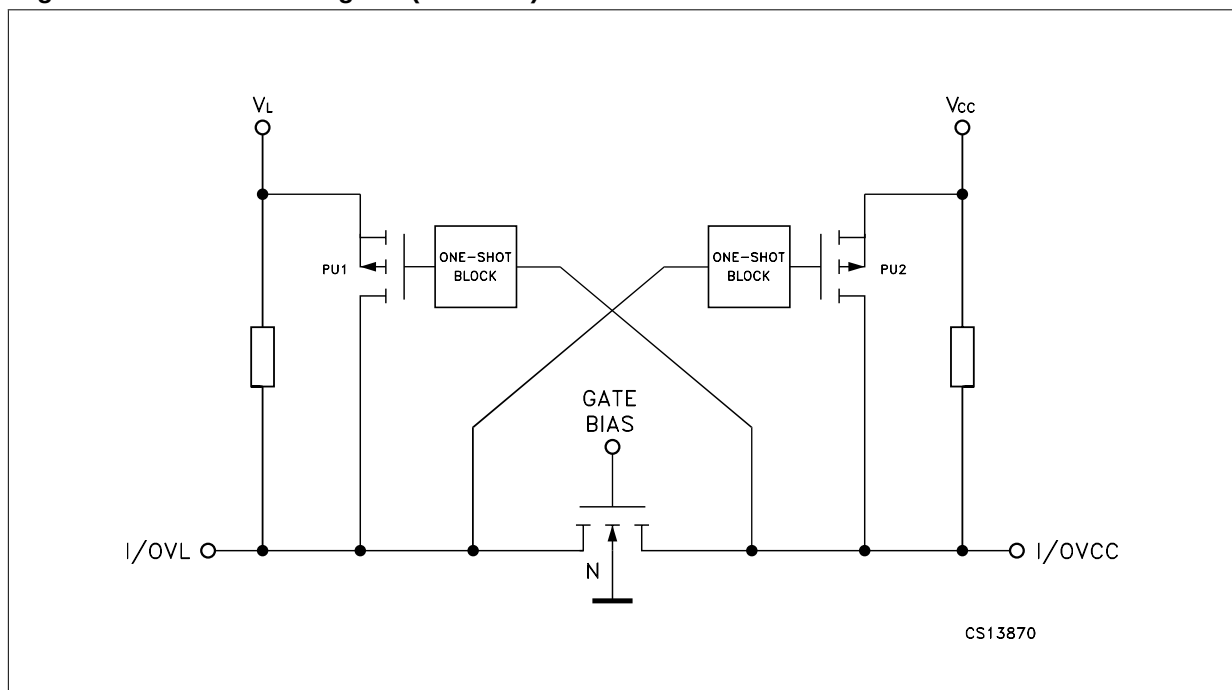


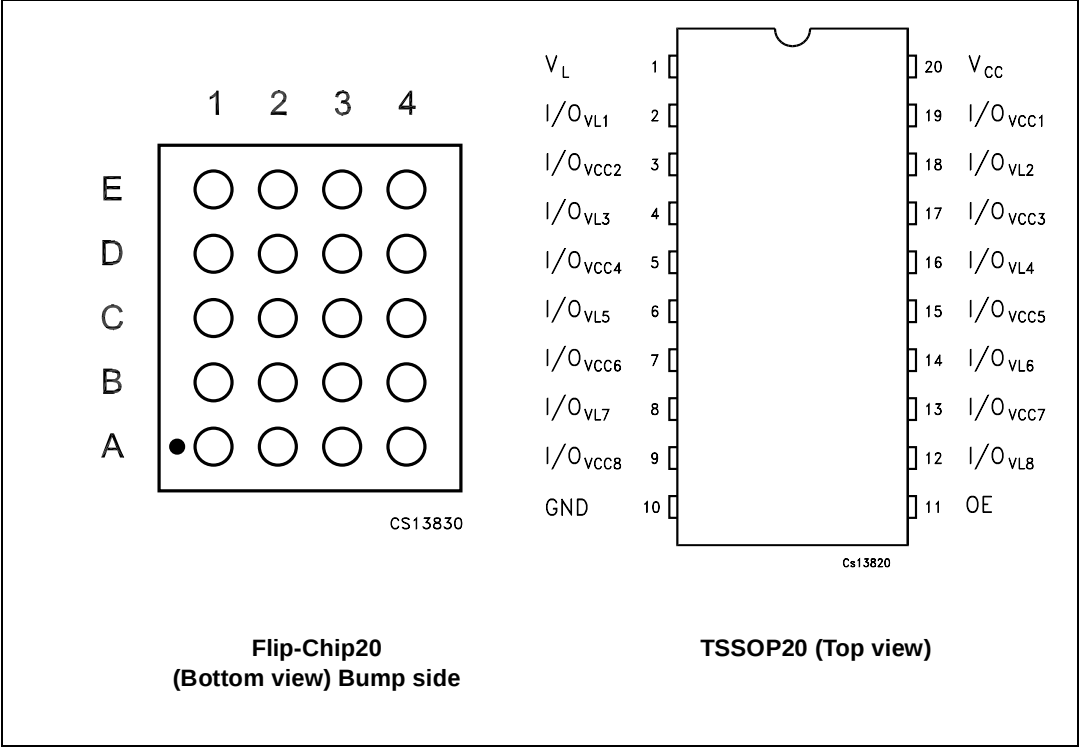
Figure 2. Functional diagram (1 I/O line)



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection



2.2 Pin description

Table 1. Pin description

Flip-Chip20 Pin N°	TSSOP20 Pin N°	Symbol	Name and function
E2, D1, D2, C1, C2, B1, B2, A1	2, 18, 4, 16, 6, 14, 8, 12	I/O_{VL1} to I/O_{VL8}	Data Inputs/Outputs
E3, D4, D3, C4, C3, B4, B3, A4	19, 3, 17, 5, 15, 7, 13, 9	I/O_{VCC1} to I/O_{VCC8}	Data Inputs/Outputs
A2	11	OE	Output Enable Inputs
A3	10	GND	Ground (0V)
E1	1	V_L	Positive Supply Voltage
E4	20	V_{CC}	Positive Supply Voltage

3 Electrical data

3.1 Maximum ratings

Table 2. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_L	Supply Voltage	-0.3 to V_{CC}	V
V_{CC}	Supply Voltage	-0.3 to +7.0	V
V_{OE}	DC Control Input Voltage	-0.3 to +7.0	V
$V_{I/OVL}$	DC I/O_{VL} Input Voltage (OE = Gnd or V_L)	-0.3 to $V_L + 0.3$	V
$V_{I/OVCC}$	DC I/O_{VCC} Input Voltage (OE = Gnd or V_L)	-0.3 to $V_{CC} + 0.3$	V
I_{IK}	DC Input Diode Current (OE Control Pin)	- 20	mA
I_{IOVL}	DC Output Current	± 25	mA
I_{IOVCC}	DC Output Current	± 25	mA
I_{SCTOUT}	Short Circuit Duration I/O_{VL} , I/O_{VCC} Driven from 40mA Source	Continuous	mA
I_{CCB}	DC V_{CC} or Ground Current	± 100	mA
P_d	Power Dissipation ⁽¹⁾	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

1. 500mW: $\cong$ 65°C derated to 300mW by 10mW/°C: 65°C to 85°C

3.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_L	Supply Voltage		1.71 to V_{CC}	V
V_{CC}	Supply Voltage		1.71 to 5.5	V
V_I	Input Voltage (OE Output Enable Pin, V_L Power Supply referred)		0 to 5.5	V
$V_{I/OVL}$	I/O_{VL} Voltage		0 to V_L	V
$V_{I/OVCC}$	I/O_{VCC} Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to 85	°C
dt/dv	Input Rise and Fall Time (OE Control Pin) ⁽¹⁾		0 to 10	ns/V
dt/dv	Input Rise and Fall Time ⁽²⁾	$1.71 < V_L < V_{CC} < 5V$	0 to 10	ns/V
		$V_{CC} = V_L = 5V$	0 to 3	ns/V

1. V_{OE} from 10% V_L to 90% V_L

2. $V_{I/OVL}$ from 10% V_L to 90% V_L ; $V_{I/OVCC}$ from 10% V_{CC} to 90% V_{CC}

4 Electrical characteristics

Table 4. DC Specification

Symbol	Parameter	Test Condition			Value					Unit
		V _L (*) (V)	V _{CC} (*) (V)		T _A = 25 °C			-40 to 85 °C		
					Min.	Typ	Max.	Min.	Max.	
V _{IHL}	High Level Input Voltage (I/O _{VL})	1.8	V _L to 5.5		V _L -0.2			V _L -0.2		V
		2.5	V _L to 5.5		0.75V _L			0.75V _L		
		3.3	V _L to 5.5		0.75V _L			0.75V _L		
		5.0	V _L to 5.5		0.75V _L			0.75V _L		
V _{ILL}	Low Level Input Voltage (I/O _{VL})	1.8	V _L to 5.5				0.15		0.15	V
		2.5	V _L to 5.5				0.30		0.30	
		3.3	V _L to 5.5				0.30		0.30	
		5.0	V _L to 5.5				0.30		0.30	
V _{IHC}	High Level Input Voltage (I/O _{VCC})	1.8	V _L to 5.5		V _L -0.2			V _L -0.2		V
		2.5	V _L to 5.5		0.75V _{CC}			0.75V _{CC}		
		3.3	V _L to 5.5		0.75V _{CC}			0.75V _{CC}		
		5.0	V _L to 5.5		0.75V _{CC}			0.75V _{CC}		
V _{ILC}	Low Level Input Voltage (I/O _{VCC})	1.8	V _L to 5.5				0.15		0.15	V
		2.5	V _L to 5.5				0.30		0.30	
		3.3	V _L to 5.5				0.30		0.30	
		5.0	V _L to 5.5				0.30		0.30	

Table 4. DC Specification

Symbol	Parameter	Test Condition			Value					Unit
		V _L (*) (V)	V _{CC} (*) (V)		T _A = 25 °C			-40 to 85 °C		
					Min.	Typ	Max.	Min.	Max.	
V _{IH-TS}	High Level Input Voltage (OE)	1.8	V _L to 5.5		V _L -0.2			V _L -0.2		V
		2.5	V _L to 5.5		0.75V _L			0.75V _L		
		3.3	V _L to 5.5		0.75V _L			0.75V _L		
		5.0	V _L to 5.5		0.75V _L			0.75V _L		
V _{IL-TS}	Low Level Input Voltage (OE)	1.8	V _L to 5.5				0.15		0.15	V
		2.5	V _L to 5.5				0.25V _L		0.25V _L	
		3.3	V _L to 5.5				0.25V _L		0.25V _L	
		5.0	V _L to 5.5				0.25V _L		0.25V _L	
V _{OHL}	High Level Output Voltage I/O _{VL}	1.8 to 5.5	V _L to 5.5	I _O =-20 μA I/O _{VCC} ≥V _{CC} -0.2	0.67V _L			0.67V _L		V
V _{OLL}	Low Level Output Voltage I/O _{VL}			I _O =1.0 mA I/O _{VCC} ≤0.15V			0.40		0.40	
V _{OHC}	High Level Output Voltage I/O _{VCC}	1.8 to 5.5	V _L to 5.5	I _O =-20 μA I/O _{VL} ≥V _L -0.2	0.67V _{CC}			0.67V _{CC}		V
V _{OLC}	Low Level Output Voltage I/O _{VCC}			I _O =1.0 mA I/O _{VL} ≤0.15V			0.40		0.40	
I _{TSL}	Control Input Leakage Current (OE)	1.8 to 5.5	V _L to 5.5	V _I =GNDor5.5			1		1	μA
I _{TS-LKG}	High Impedance Input Leakage Current (I/O _{VL} , I/O _{VCC})	1.8 to 5.5	V _L to 5.5	OE = GND			1		1	μA
I _{QVCC}	Quiescent Supply Current V _{CC}	1.8 to 5.5	V _L to 5.5	I/O _{VL} , I/O _{VCC} unconnected		0.1	1		10	μA

Table 4. DC Specification

Symbol	Parameter	Test Condition			Value					Unit
		V _L (*) (V)	V _{CC} (*) (V)		T _A = 25 °C			-40 to 85 °C		
					Min.	Typ	Max.	Min.	Max.	
I _{QVL}	Quiescent Supply Current V _L	1.8 to 5.5	V _L to 5.5	I/O _{VL} , I/O _{VCC} unconnected		13	20		100	μA
I _{TS-VCC}	High Impedance Mode Quiescent Supply Current V _{CC}	1.8 to 5.5	V _L to 5.5	OE= GND			1		1	μA
I _{TS-VL}	High Impedance Mode Quiescent Supply Current V _L	1.8 to 5.5	V _L to 5.5	OE= GND I/O _{VL} =GND to V _L I/O _{VCC} = GND to V _{CC}			1		1	μA

- Note:
- 1 Typical values are referred to $T_A = 25\text{ °C}$
 - 2 Power Supply Range: V_L , V_{CC} $1.8\text{V} \pm 5\%$, $2.5 \pm 0.2\text{V}$, $3.3 \pm 0.3\text{V}$, $5.0 \pm 0.5\text{V}$
 - 3 For normal operation, ensure $V_L < (V_{CC} + 0.3\text{V})$. During power-up, $V_L > (V_{CC} + 0.3\text{V})$ will not damage the device

Table 5. AC Electrical characteristics (totem pole driving)

Symbol	Parameter		Test Condition ⁽¹⁾		Value			Unit	
			C _L =15pF t _r =t _f ≤ 6ns Driver output R _T ≤ 50Ω ⁽²⁾		-40 to +85 °C				
			V _L (V) ⁽³⁾	V _{CC} (V) ⁽³⁾	Min.	Typ. ⁽⁴⁾	Max.		
t _{RVCC}	Rise Time I/O _{VCC} ⁽³⁾⁽⁸⁾		1.8	1.8		11	15	ns	
			1.8	2.5		11	15		
			1.8	3.3		10	15		
			1.8	5.0		9	15		
			2.5	3.3		8	15		
t _{FCC}	Fall Time I/O _{VCC} ⁽³⁾⁽⁸⁾		1.8	1.8		6	15	ns	
			1.8	2.5		7	15		
			1.8	3.3		8	15		
			1.8	5.0		10	15		
			2.5	3.3		6	15		
t _{RVL}	Rise Time I/O _{VL} ⁽³⁾⁽⁸⁾		1.8	1.8		12	15	ns	
			1.8	2.5		10	15		
			1.8	3.3		9	15		
			1.8	5.0		10	15		
			2.5	3.3		7	15		
t _{FVL}	Fall Time I/O _{VL} ⁽³⁾⁽⁸⁾		1.8	1.8		7	15	ns	
			1.8	2.5		6	15		
			1.8	3.3		6	15		
			1.8	5.0		7	15		
			2.5	3.3		4	15		
t _{IOVL-VCC}	Propagation Delay Time(4) I/O _{VL} -LH to I/O _{VCC} -LH I/O _{VL} -HL to I/O _{VCC} -HL		t _{PLH}	1.8	1.8		6	15	ns
				1.8	2.5		7	15	
				1.8	3.3		7	15	
				1.8	5.0		7	15	
				2.5	3.3		4	15	
			t _{PHL}	1.8	1.8		5	15	
				1.8	2.5		5	15	
				1.8	3.3		6	15	
				1.8	5.0		8	15	
				2.5	3.3		4	15	

Table 5. AC Electrical characteristics (totem pole driving)

Symbol	Parameter		Test Condition		Value			Unit
			C _L =15pF t _r =t _f ≤ 6ns Driver output R _T ≤ 50Ω		-40 to +85 °C			
			V _L (V)	V _{CC} (V)	Min.	Typ.	Max.	
t _{IOVCC-VL}	Propagation Delay Time(4) I/O _{VCC-LH} to I/O _{VL-LH} I/O _{VCC-HL} to I/O _{VL-HL}	t _{PLH}	1.8	1.8		2	15	ns
			1.8	2.5		2	15	
			1.8	3.3		2	15	
			1.8	5.0		2	15	
			2.5	3.3		2	15	
		t _{PHL}	1.8	1.8		5	15	
			1.8	2.5		5	15	
			1.8	3.3		5	15	
			1.8	5.0		6	15	
			2.5	3.3		4	15	
t _{PZL} t _{PZH} t _{PLZ} t _{PZL}	Output Enable and Disable Time	1.8	1.8		60	80	ns	
		1.8	5.0		150	200		
t _{OSLH} t _{OSHL}	Channel to channel Skew Time (6)(7)	1.8	1.8		0.1	1	ns	
		1.8	5.0		0.5	1		
DR	Maximum Data Rate	1.8 to 5.0	V _L to 5.0	13			Mbps	

- For normal operation, ensure $V_L < (V_{CC} + 0.3V)$. During power-up, $V_L > (V_{CC} + 0.3V)$ will not damage the device
- For $V_{CC} = V_L = 1.8V$, $t_r = t_f \leq 4\text{ns}$
- Power Supply Range: V_L , V_{CC} $1.8V \pm 5\%$, $2.5 \pm 0.2V$, $3.3 \pm 0.3V$, $5.0 \pm 0.5V$.
- Typical values are referred to $T_A=25^\circ\text{C}$ Typical values are referred to $T_A=25^\circ\text{C}$
- Rise Time:10% to 90%, Fall Time 90% to 10%
- tpd: 50% to 50%
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)
- Each translator equally loaded; parameter guaranteed by design

Table 6. AC characteristic (open drain driving)

Symbol	Parameter		Test Condition ⁽¹⁾		Value			Unit
			C _L =15pF t _r =t _f ≤ 6ns Driver output R _T ≤ 50Ω ⁽²⁾		-40 to +85 °C			
			V _L (V) ⁽³⁾	V _{CC} (V) ⁽³⁾	Min.	Typ. ⁽⁴⁾	Max.	
t _{RVCC}	Rise Time I/O _{VCC} ⁽³⁾⁽⁸⁾		1.8	1.8		210	300	ns
			1.8	5.0		59	150	
t _{FCC}	Fall Time I/O _{VCC} ⁽³⁾⁽⁸⁾		1.8	1.8		12	30	ns
			1.8	5.0		20	30	
t _{RVL}	Rise Time I/O _{VL} ⁽³⁾⁽⁸⁾		1.8	1.8		210	300	ns
			1.8	5.0		96	150	
t _{FVL}	Fall Time I/O _{VL} ⁽³⁾⁽⁸⁾		1.8	1.8		11	30	ns
			1.8	5.0		11	30	
t _{IOVL-VCC}	Propagation Delay Time(4) I/O _{VL-LH} to I/O _{VCC-LH} I/O _{VL-HL} to I/O _{VCC-HL}	t _{PLH}	1.8	1.8		210	300	ns
			1.8	5.0		100	150	
		t _{PHL}	1.8	1.8		7	20	
			1.8	5.0		14	20	
t _{IOVCC-VL}	Propagation Delay Time(4) I/O _{VCC-LH} to I/O _{VL-LH} I/O _{VCC-HL} to I/O _{VL-HL}	t _{PLH}	1.8	1.8		210	300	ns
			1.8	5.0		57	150	
		t _{PHL}	1.8	1.8		7	20	
			1.8	5.0		8	20	
t _{PZL} t _{PZH} t _{PLZ} t _{PZL}	Output Enable and Disable Time		1.8	1.8		60	80	ns
			1.8	5.0		150	200	
t _{OSLH} t _{OSHL}	Channel to channel Skew Time (6)(7)		1.8	1.8		10	20	ns
			1.8	5.0		2	10	
DR	Maximum Data Rate		1.8 to 5.0	V _L to 5.0	800			kbps

- For normal operation, ensure $V_L < (V_{CC} + 0.3V)$. During power-up, $V_L > (V_{CC} + 0.3V)$ will not damage the device
- For $V_{CC} = V_L = 1.8V$, $t_r = t_f \leq 4ns$
- Power Supply Range: V_L , V_{CC} $1.8V \pm 5\%$, $2.5 \pm 0.2V$, $3.3 \pm 0.3V$, $5.0 \pm 0.5V$.
- Typical values are referred to $T_A=25^\circ C$
- Rise Time:10% to 90%, Fall Time 90% to 10%
- t_{pd} : 50% to 50%
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)
- Each translator equally loaded; parameter guaranteed by design

5 Test circuit

Figure 4. Test circuit

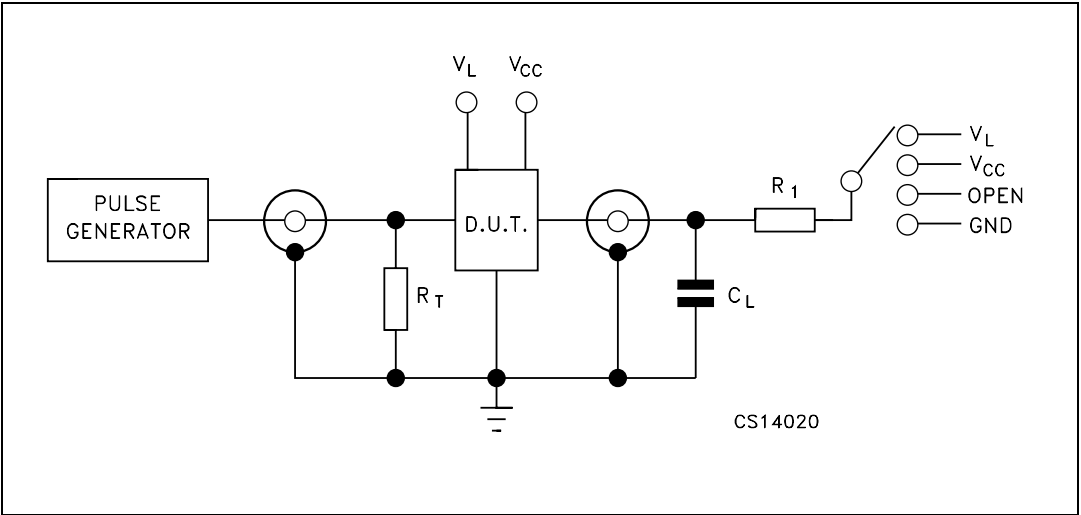


Table 7. Test circuit switches

Test	Switch		
	Driving I/O _{V_L}	Driving I/O _{V_{CC}}	Open Drain Driving
t_{PLH} , t_{PHL}	Open	Open	Open
t_{PZL} , t_{PLZ}	V _{CC}	V _L	-
t_{PZH} , t_{PHZ}	Gnd	Gnd	-

Note: $C_L = 15/50pF$ or equivalent (includes jig and probe capacitance)
 $R_1 = 1K\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Table 8. Truth table

Control Pin	Bidirectional Input/Outputs	
OE	I/O _{V_L}	I/O _{V_{CC}}
H ⁽¹⁾	H ⁽¹⁾	H ⁽²⁾
H ⁽¹⁾	L	L
L	Z	Z

1. High Level V_L Power Supply referred
2. High Level V_{CC} Power Supply referred

Note: X= Do not care; Z = High Impedance;

6 Waveforms

Table 9. Waveform symbol value

Symbol	Driving I/O _{VL}		Driving I/O _{VCC}	
	$1.8V \leq V_L \leq V_{CC} \leq 2.5V$	$3.3V \leq V_L \leq V_{CC} \leq 5.0V$	$1.8V \leq V_L \leq V_{CC} \leq 2.5V$	$3.3V \leq V_L \leq V_{CC} \leq 5.0V$
V _{IH}	V _L	V _L	V _{CC}	V _{CC}
V _{IM}	50% V _L	50% V _L	50% V _{CC}	50% V _{CC}
V _{OM}	50% V _{CC}	50% V _{CC}	50% V _{CC}	50% V _{CC}
V _X	V _{OL} +0.15V	V _{OL} +0.3V	V _{OL} +0.15V	V _{OL} +0.3V
V _Y	V _{OH} -0.15V	V _{OH} -0.3V	V _{OH} -0.15V	V _{OH} -0.3V

Figure 5. Waveform - propagation delay (f = 1MHz; 50% duty cycle)

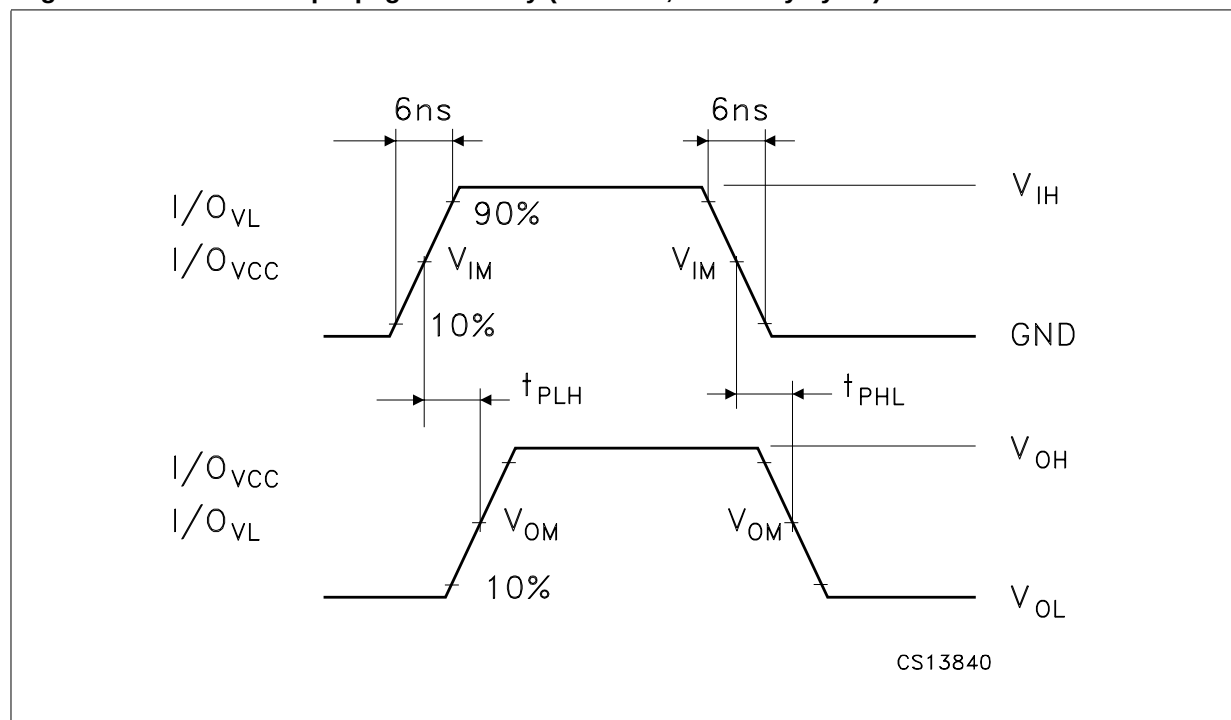
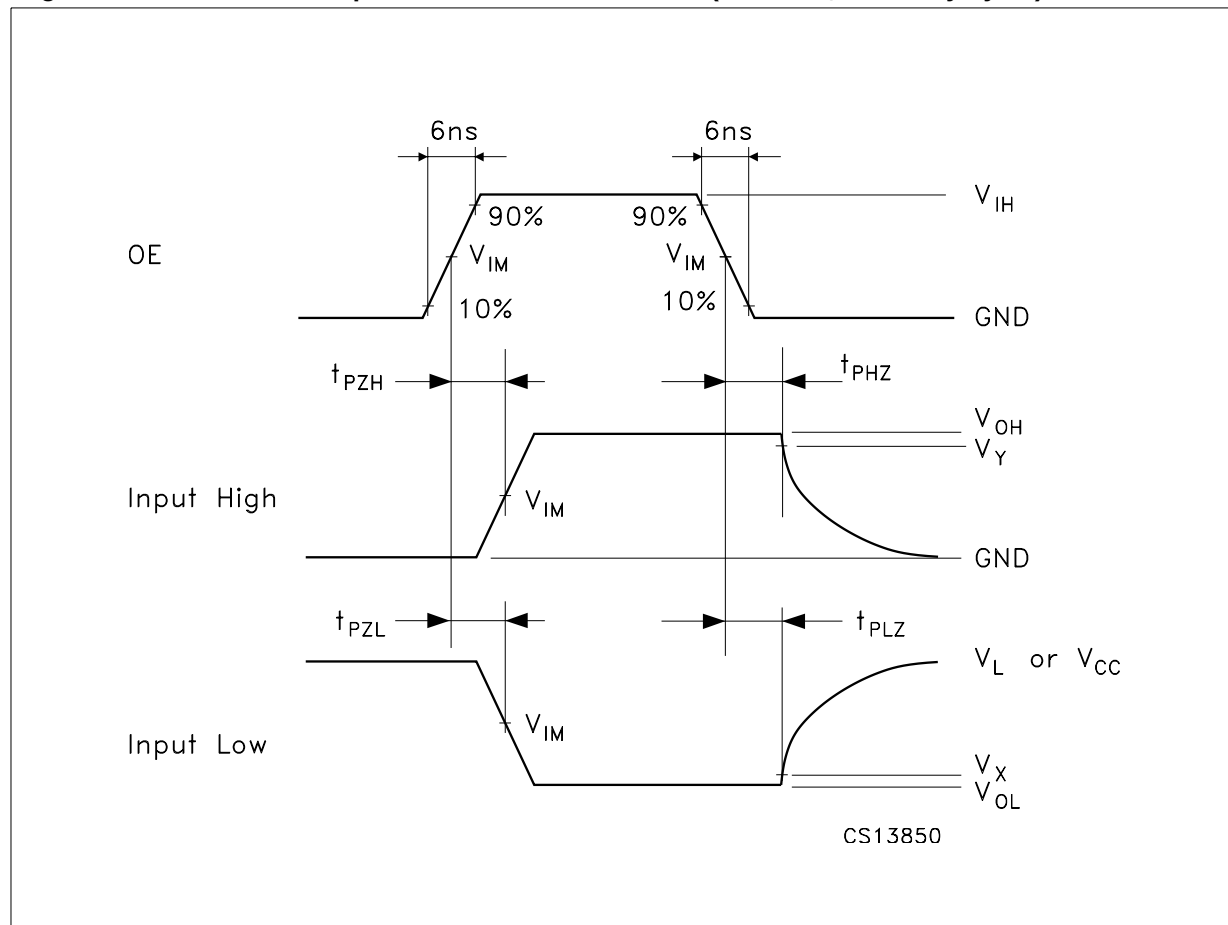


Figure 6. Waveform - output enable and disable time ($f = 1\text{MHz}$; 50% duty cycle)

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Figure 7. TSSOP20 Mechanical data

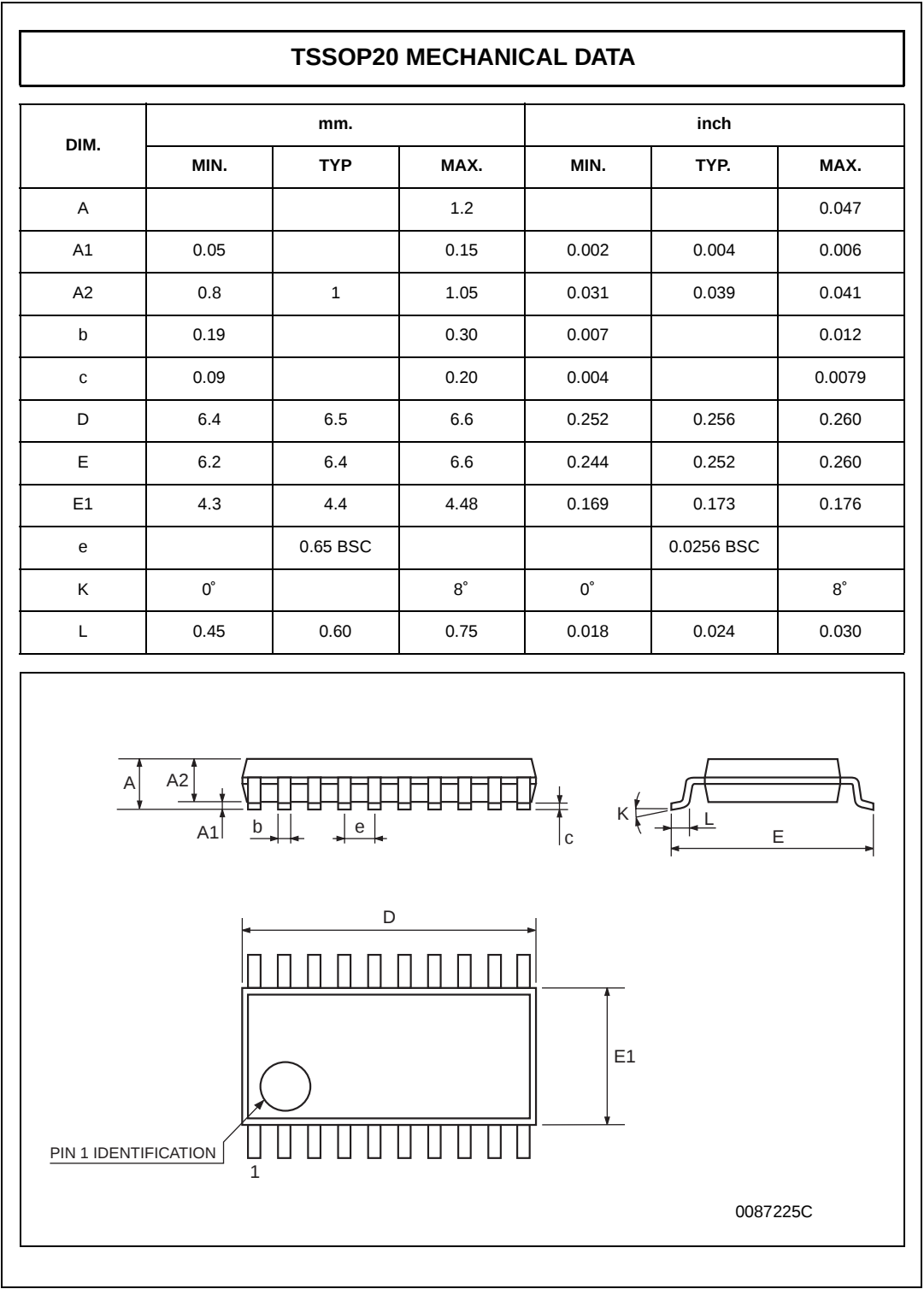


Figure 8. Flip-Chip20 Mechanical data

Flip-Chip20 MECHANICAL DATA						
DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.81	0.89	1.00	31.9	35.0	39.4
A1	0.15	0.24	0.35	5.9	9.4	13.8
A2		0.65			25.6	
b	0.25	0.30	0.35	9.8	11.8	13.8
D	2.41	2.46	2.51	94.9	96.9	98.8
D1		2.00			78.7	
E	1.93	1.98	2.03	76.0	78.0	79.9
E1		1.5			59.1	
e		0.50			19.7	
SE		0.25			9.8	

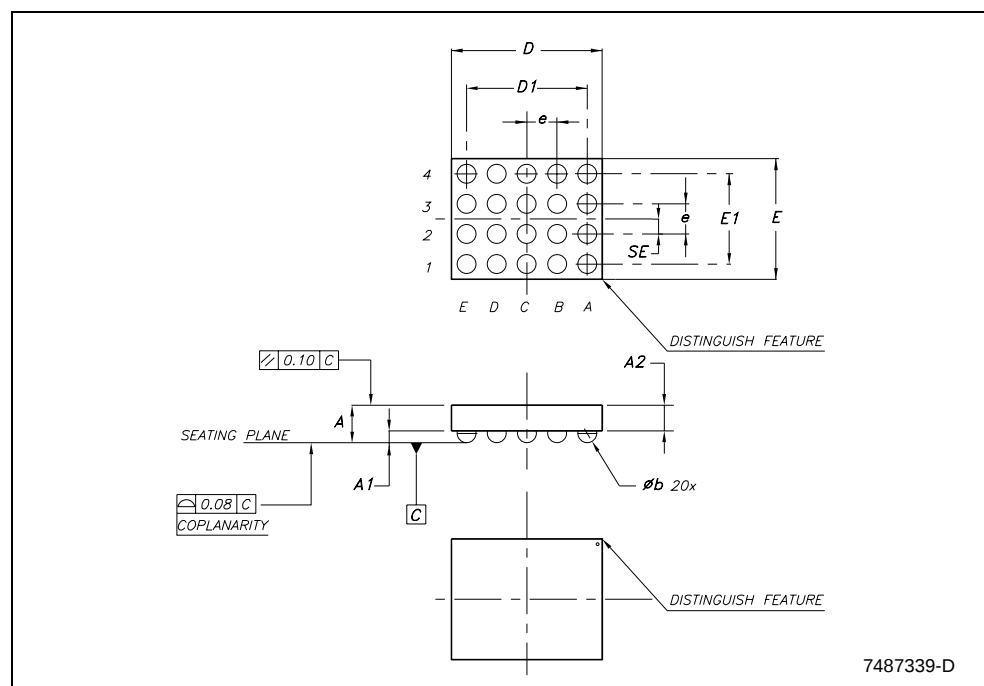


Figure 9. TSSOP20 Tape and reel

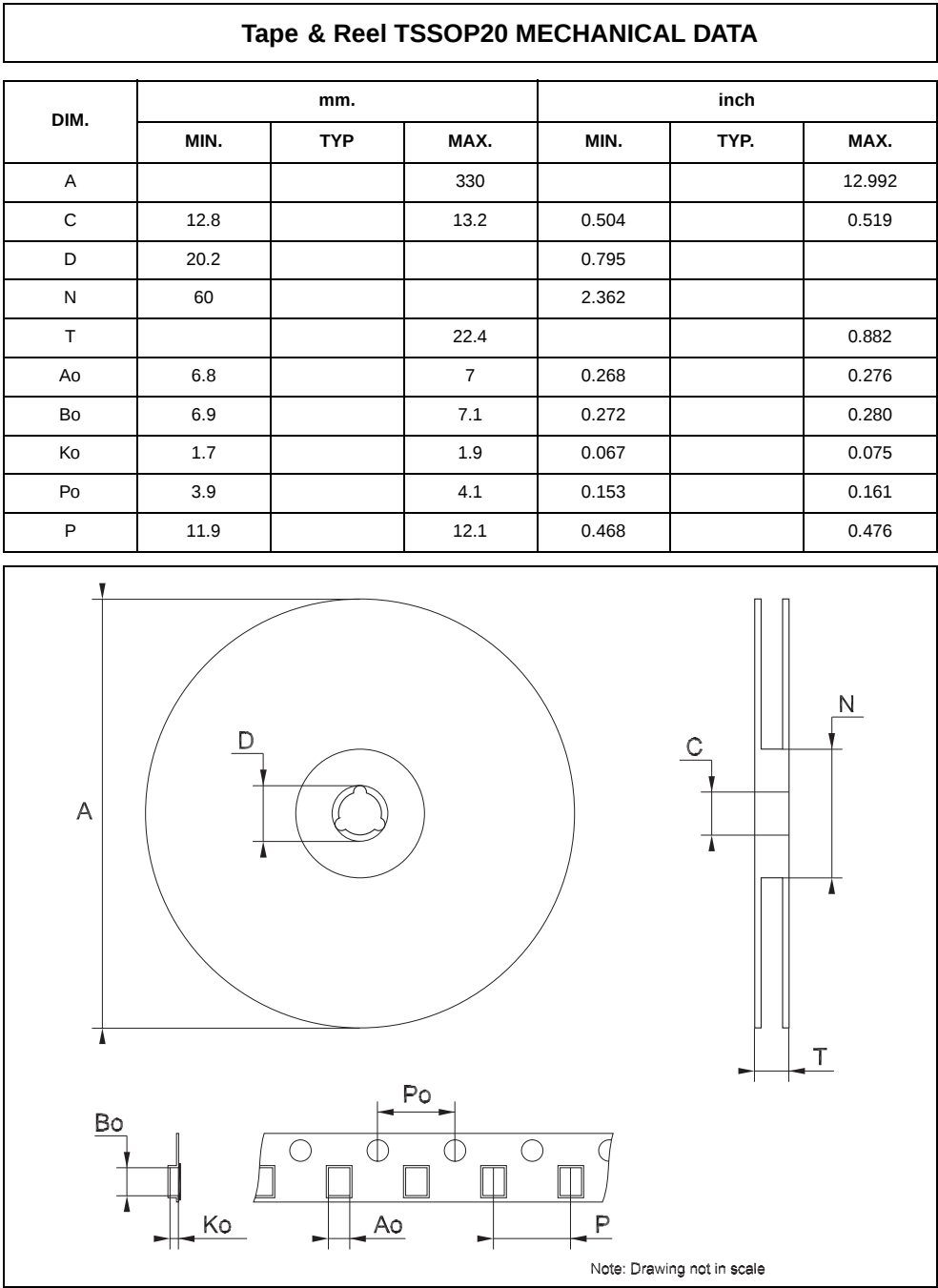
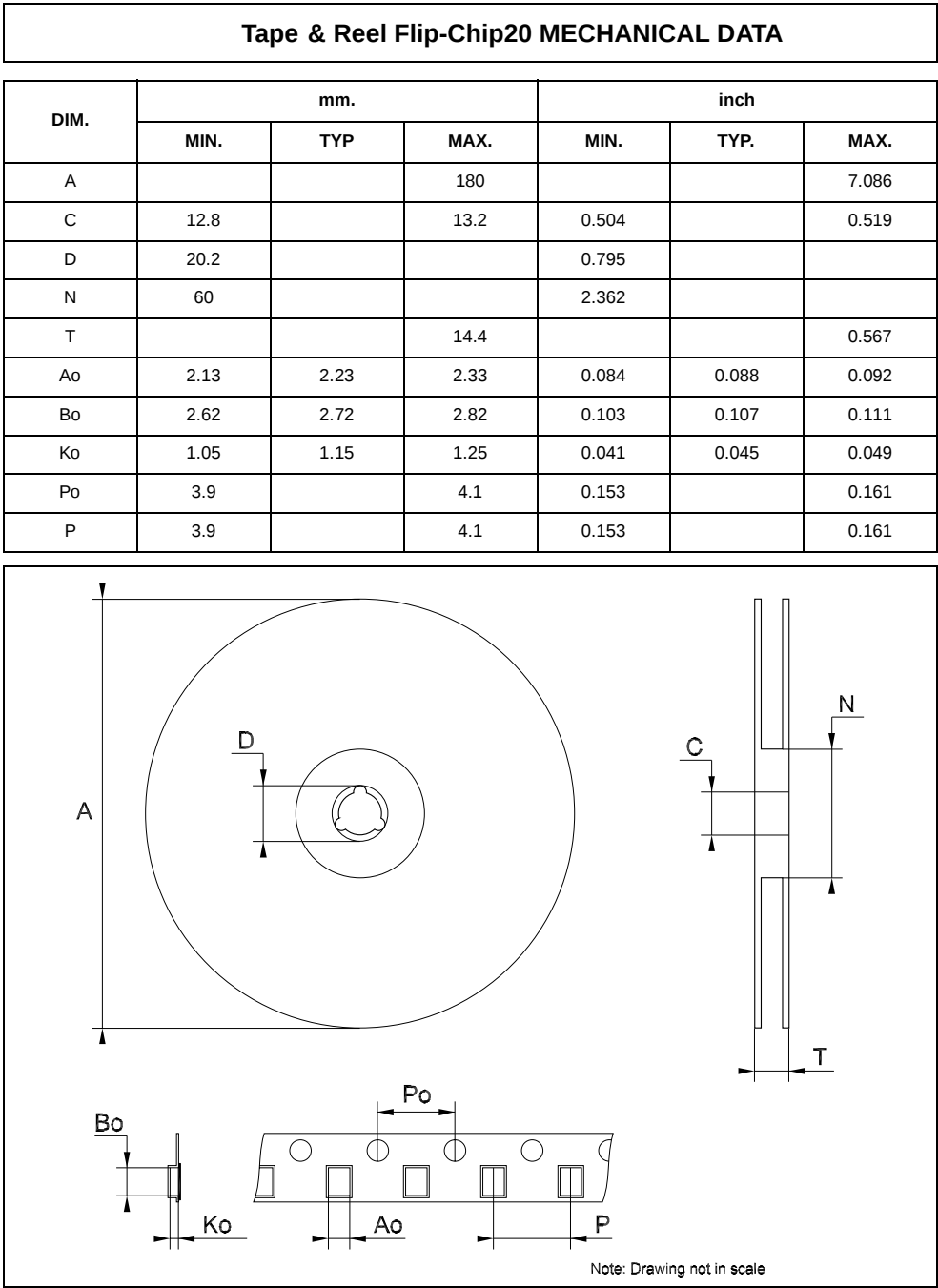


Figure 10. Flip-Chip20 Tape and reel



8 Revision history

Table 10. Revision history

Date	Revision	Changes
10-Apr-2006	1	Initial release.

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