

N-Channel Reduced Q_g , Fast Switching MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
30	0.007 at $V_{GS} = 10$ V	19	11.5
	0.0095 at $V_{GS} = 4.5$ V	17	

FEATURES

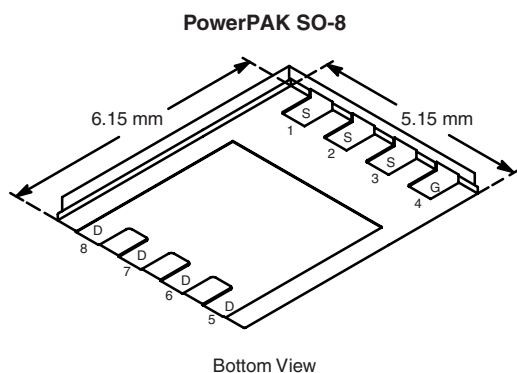
- Halogen-free available
- TrenchFET® Gen II Power MOSFET
- PWM Optimized for High Efficiency
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 % R_g Tested



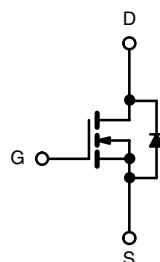
RoHS
COMPLIANT

APPLICATIONS

- DC/DC Conversion for PC



Ordering Information: Si7386DP-T1-E3 (Lead (Pb)-free)
Si7386DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

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Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	19	12	A
	T _A = 70 °C		16	9	
Pulsed Drain Current		I _{DM}	± 50		
Continuous Source Current (Diode Conduction) ^a		I _S	4.1	1.5	
Avalanche Current	L = 0.1 mH	I _{AS}	25		
Single Pulse Avalanche Energy		E _{AS}	32		
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	5	1.8	W
	T _A = 70 °C		3.2	1.1	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) ^a	R_{thJA}	21	25	$^\circ\text{C/W}$
		56	70	
Maximum Junction-to-Case (Drain)	R_{thJC}	2.4	3.0	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

MOSFET SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1.5	2.0	2.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 70^\circ\text{C}$			15	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	40			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 19\ \text{A}$		0.0058	0.007	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 17\ \text{A}$		0.0078	0.0095	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 19\ \text{A}$		50		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 4.1\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.78	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 19\ \text{A}$		11.5	18	nC
Gate-Source Charge	Q_{gs}			5.8		
Gate-Drain Charge	Q_{gd}			3.0		
Gate Resistance	R_g		0.8	1.7	2.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_g = 6\ \Omega$		12	18	ns
Rise Time	t_r			9	14	
Turn-Off Delay Time	$t_{d(off)}$			35	53	
Fall Time	t_f			10	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.8\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		25	50	

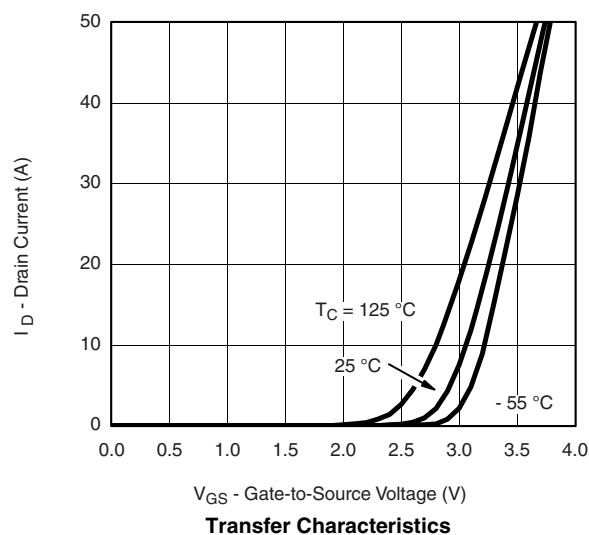
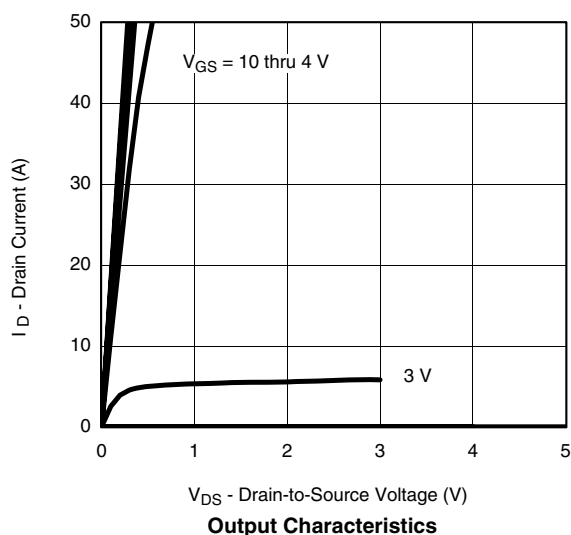
Notes:

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

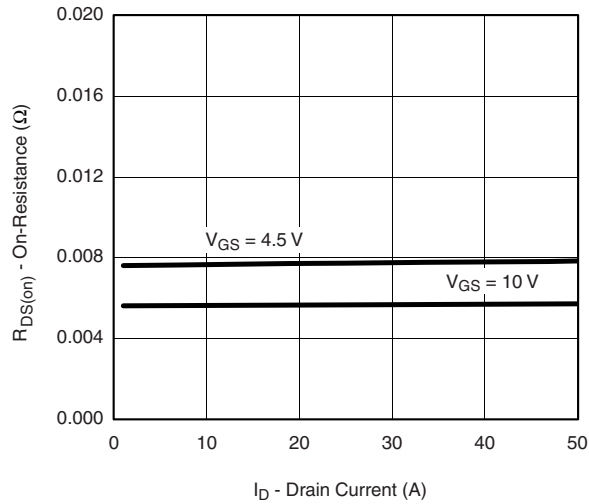
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

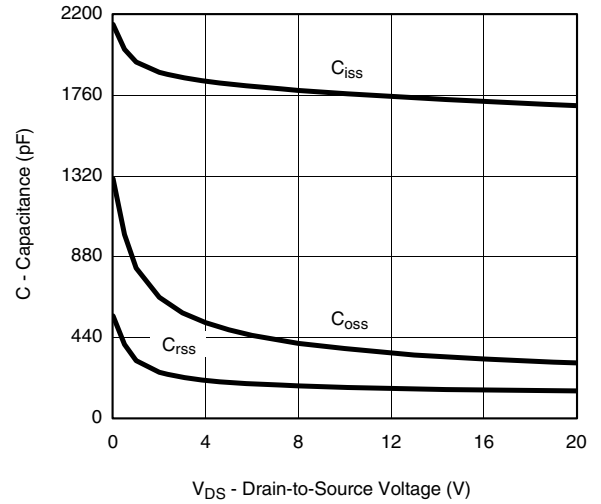
TYPICAL CHARACTERISTICS 25°C , unless otherwise noted



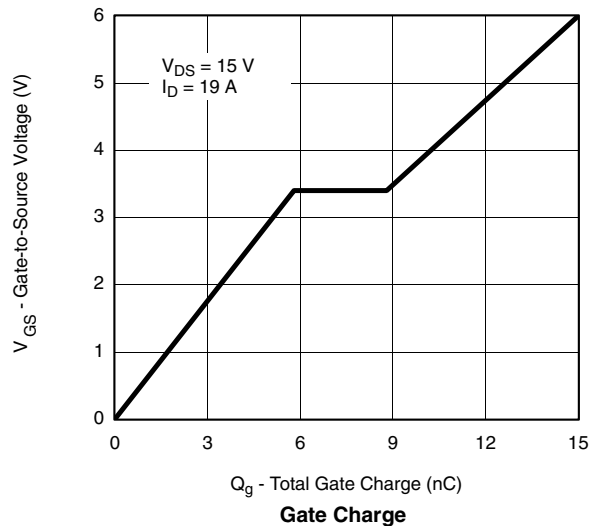
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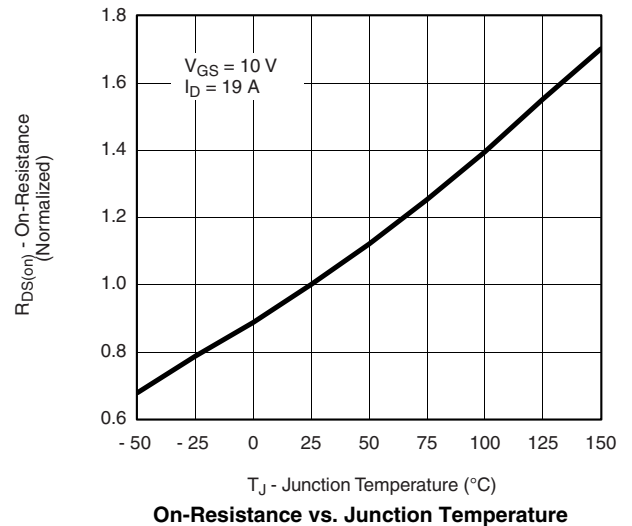
On-Resistance vs. Drain Current



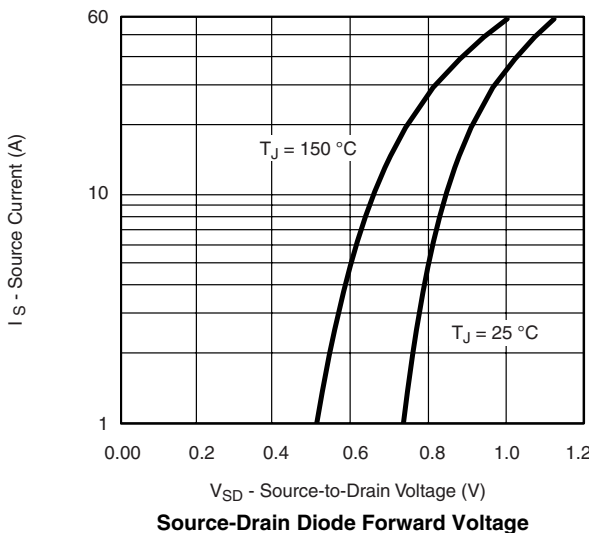
Capacitance



Gate Charge



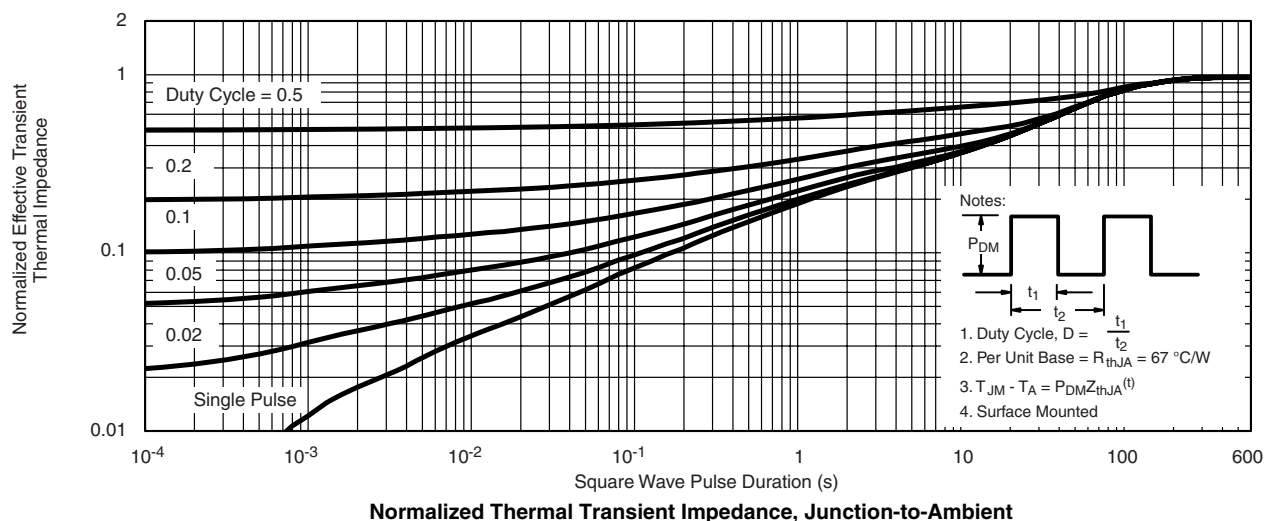
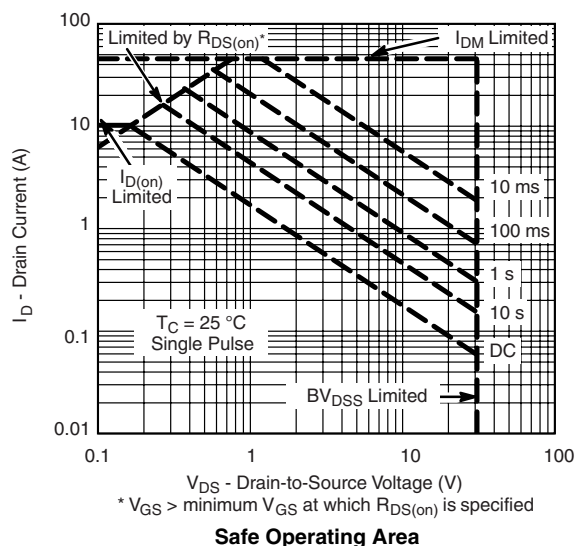
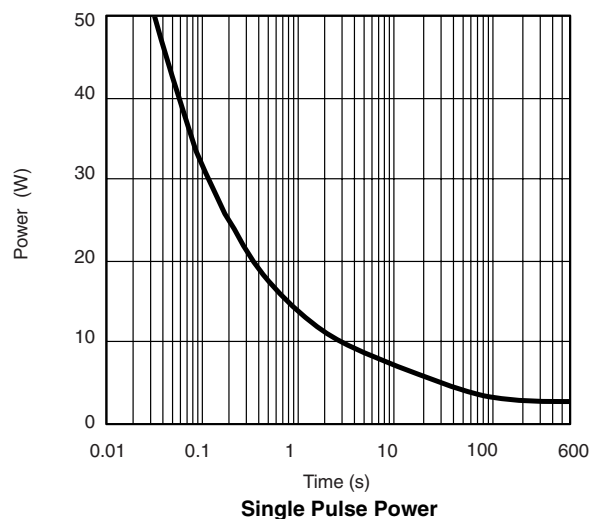
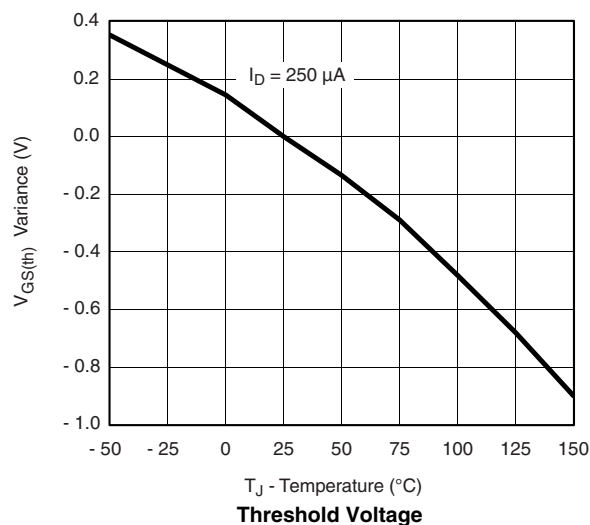
On-Resistance vs. Junction Temperature



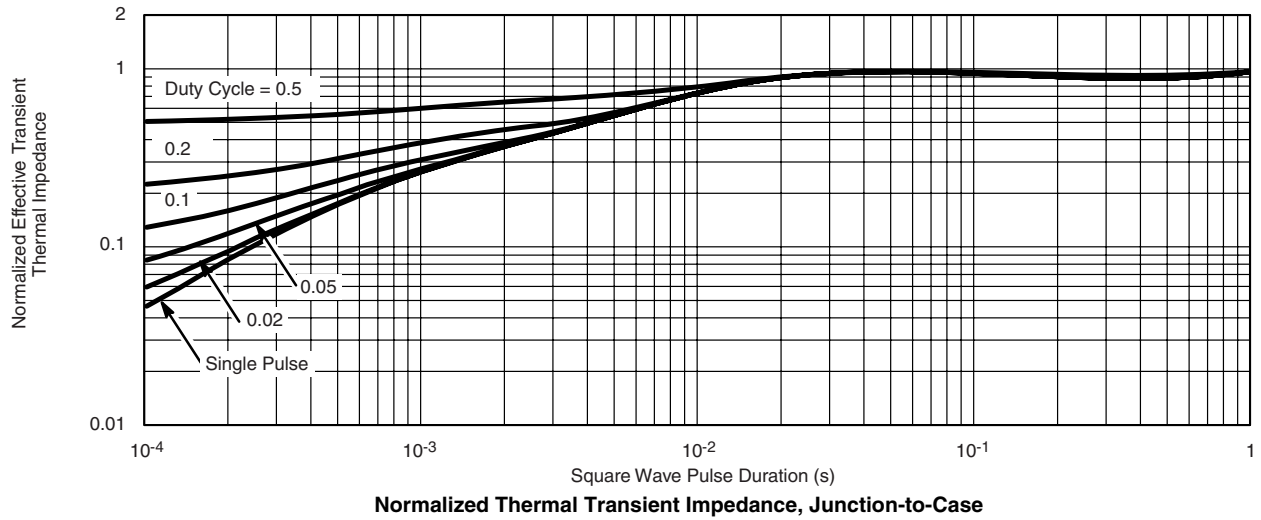
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

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