



P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

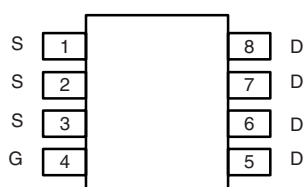
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
- 40	0.014 at $V_{GS} = - 10$ V	- 10.5	40
	0.021 at $V_{GS} = - 4.5$ V	- 8.7	

FEATURES

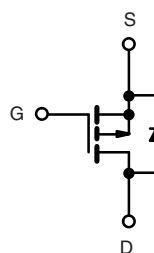
- TrenchFET® Power MOSFET
- 100 % R_g Tested

RoHS
COMPLIANT

SO-8



Top View



P-Channel MOSFET

Ordering Information: Si4401BDY-T1-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	10 sec	Steady State	Unit
Drain-Source Voltage	V_{DS}	- 40		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	- 10.5	- 8.7	A
		- 8.3	- 5.9	
Pulsed Drain Current	I_{DM}	- 50		
Continuous Source Current (Diode Conduction) ^a	I_S	- 2.6	- 1.36	
Avalanche Current	I_{AS}	30		mJ
Single Pulse Avalanche Energy	E_{AS}	45		
Maximum Power Dissipation ^a	P_D	2.9	1.5	W
		1.85	0.95	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	36	43	$^\circ\text{C/W}$
		70	84	
Maximum Junction-to-Foot (Drain)	R_{thJF}	16	21	

Notes:

a. Surface Mounted on 1" x 1" FR4 Board.

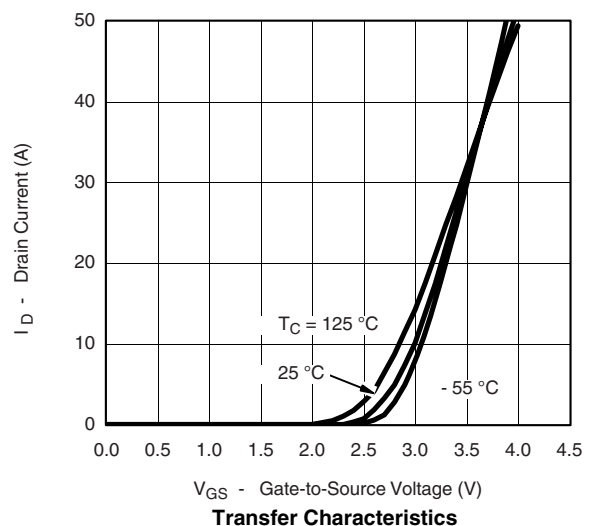
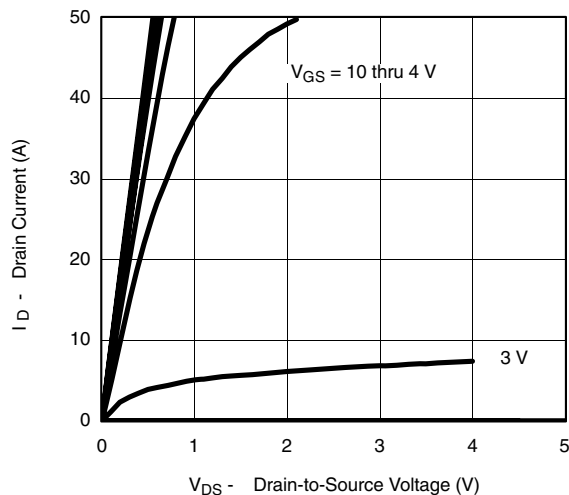
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	- 1.0		- 3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40\text{ V}$, $V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 70\text{ }^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\text{ V}$, $V_{GS} = -10\text{ V}$	- 30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\text{ V}$, $I_D = -10.5\text{ A}$		0.011	0.014	Ω
		$V_{GS} = -4.5\text{ V}$, $I_D = -8.7\text{ A}$		0.0165	0.021	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}$, $I_D = -10.5\text{ A}$		26		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.7\text{ A}$, $V_{GS} = 0\text{ V}$		- 0.74	- 1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15\text{ V}$, $V_{GS} = -5\text{ V}$, $I_D = -10.5\text{ A}$		40	55	nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			14		
Gate Resistance	R_g		1.4	2.8	4.2	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}$, $R_L = 15\text{ }\Omega$ $I_D = -1\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 6\text{ }\Omega$		16	25	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			97	150	
Fall Time	t_f			47	75	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		35	55	

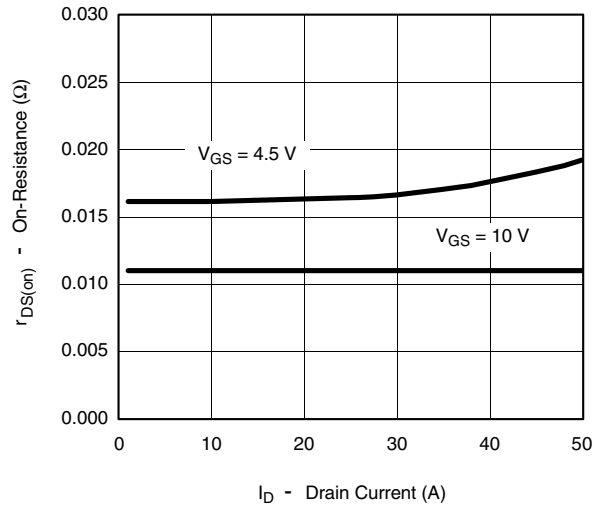
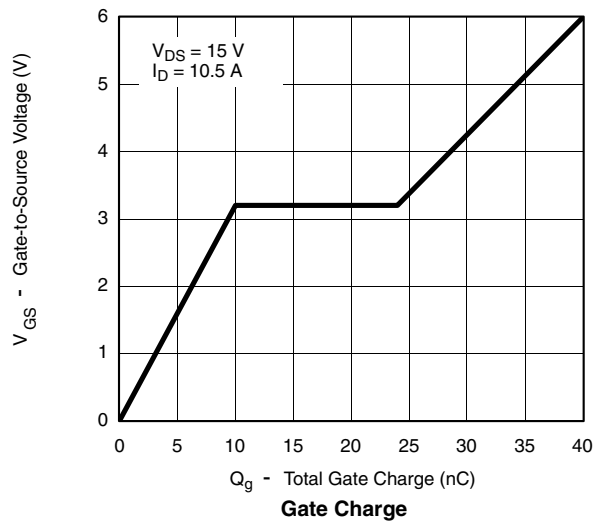
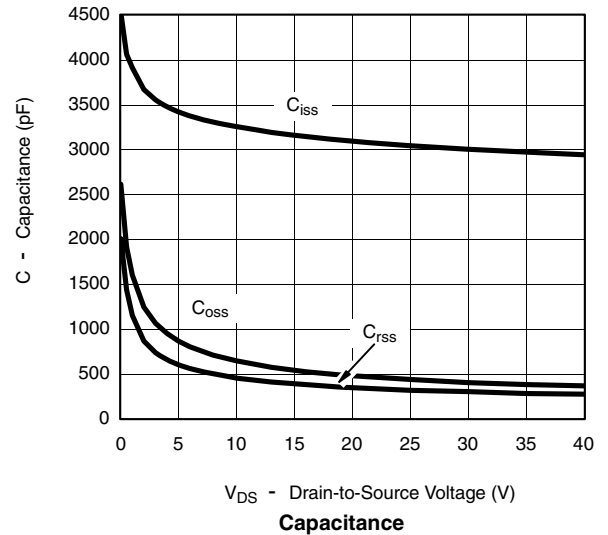
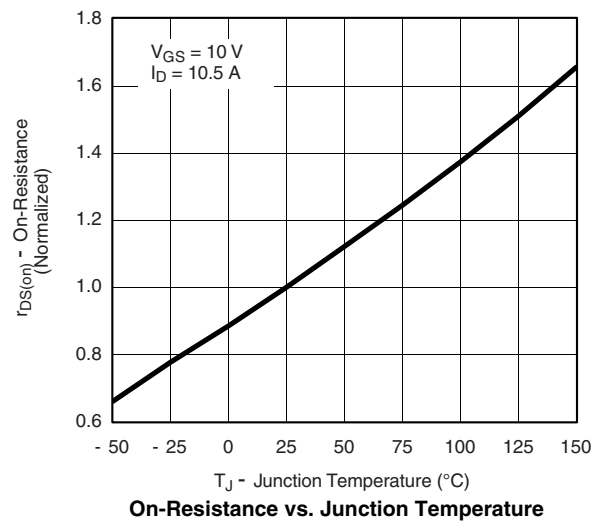
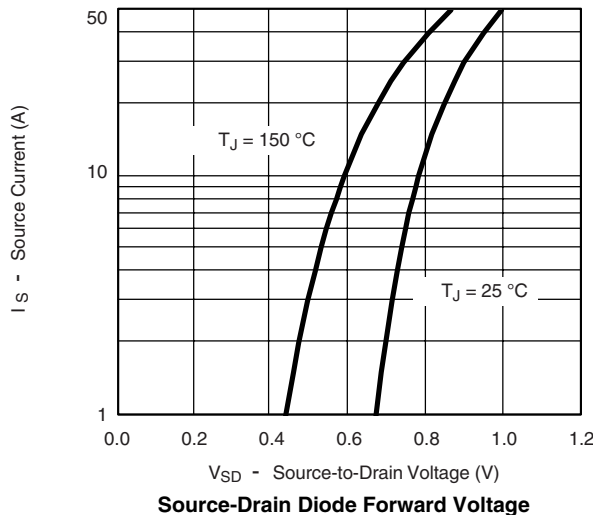
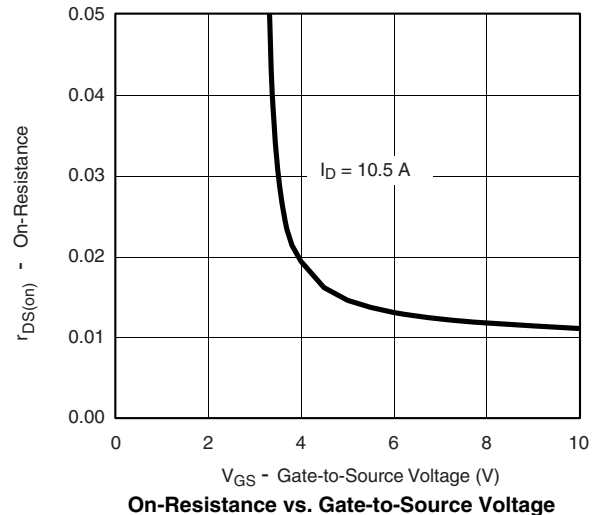
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

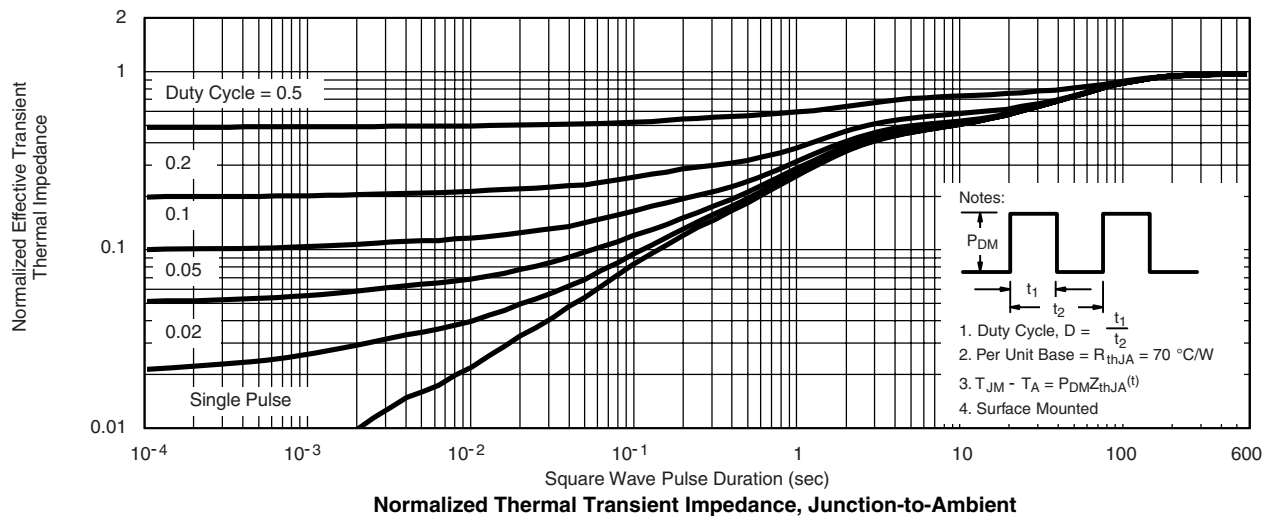
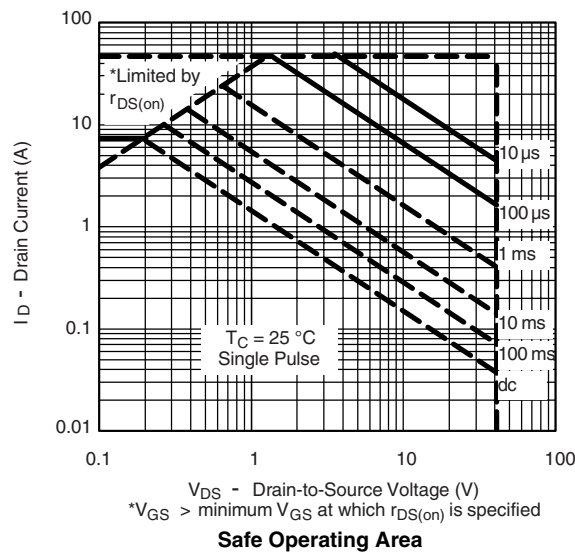
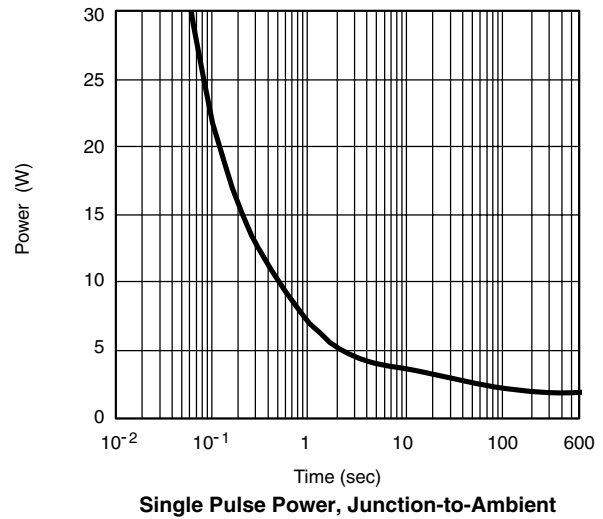
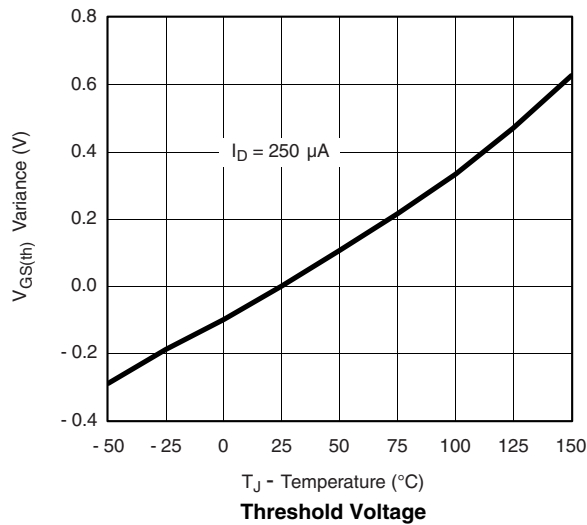
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**On-Resistance vs. Drain Current****Gate Charge****On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage**

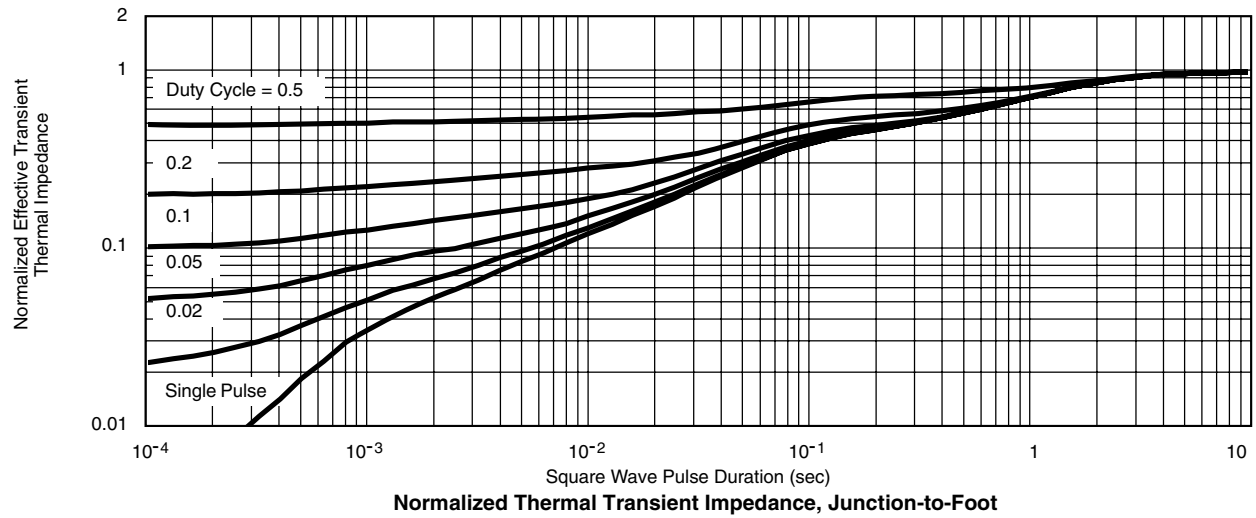
Si4401BDY

Vishay Siliconix

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73140>.



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