EPSON

S1S65000

Network Camera Controller with JPEG Encoder

■ DESCRIPTIONS

S1S65000 is an optimum network camera controller IC for configuring Internet cameras. In addition to the network/protocol processing function, it has camera interface and JPEG encoder function. Connecting a camera module, PHY for the Ethernet and a Flash EEPROM stored with a firmware to the S1S65000 enables simple configuration of the Internet camera.

Image captures and JPEG encoding can be set to work continuously or be triggered by software. While operating the S1S65000 on the LAN as the HTTP server, image files can be sent to the client on request. Image can be captured in a constant cycle by using the internal timer or in conjunction with an external sensor through its interrupt pin, and be sent to a specified client. E-mail attached format is possible.

GPIO pins and I^2C bus is useful to configure the camera and control external devices such as the motor over the network.

Network device drivers are attached for this product.

■ FEATURES

- Realize the function of the Internet camera without the PC
- Supports various camera modules up to VGA size
- Compress image into JPEG format with internal JPEG encoder
- Rewritable JPEG encoder table (quantization, AC/DC table)
- Peripheral devices control over the network using the GPIO pins and I^2C bus interface
- Various control setting over the network
- Image transfer by e-mail
- Power saving by periodic suspension/restart with timers, etc.
- Access restriction with password setting
- Wireless LAN interface support through CompactFlash card interface

■ BUILT-IN FUNCTIONS

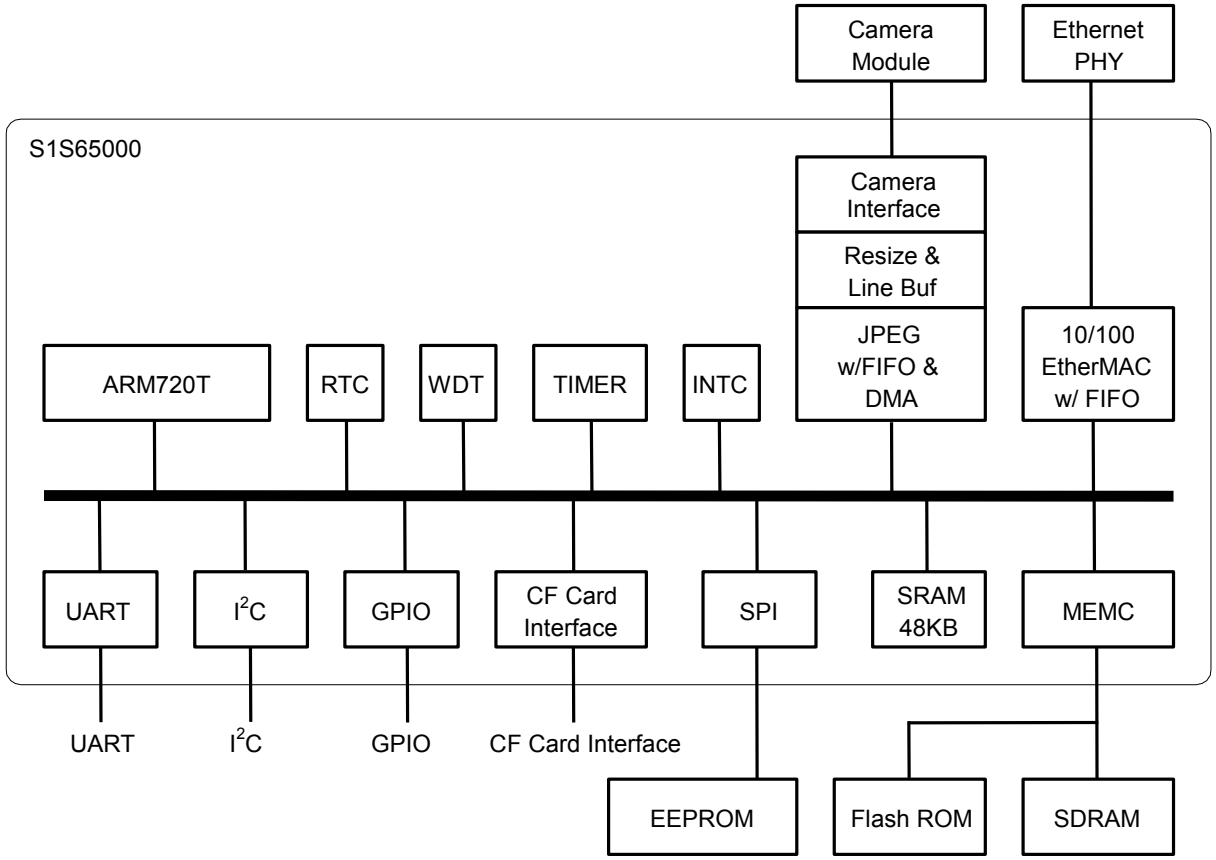
- **CPU:**
  - 32Bit RISC ARM720T (50MHz)
  - 32Bit-long codes and efficient 16bit-long codes (Thumb Code) can be selected for use
  - 31 general-purpose 32 bit registers
  - A multiplier is included in the CPU.
- **RAM:**
  - 48KB Embedded RAM for CPU/JPEG/Ethernet Work
- **Camera input/JPEG encoder:**
  - YUV4-2-2 (8bit input) (Progressive type)
  - Resolution: VGA, QVGA, CIF, QCIF
  - Supports ITU-R BT656 format
  - Hardware JPEG encoder
  - Max. 7.5 fps @VGA, 15 fps @CIF
- **JPEG:**
  - Hardware JPEG encoder
  - Resize function
  - Dedicated Line Buffer
  - FIFO for JPEG encode output
  - An enhanced DMA
- **Network:**
  - Ethernet Mac controller supporting 10/100 BASE Full duplex and Half duplex mode
  - Media Independent Interface (IEEE 802.3 Clause 22 compliant)
  - An enhanced DMA
- **External Memory Controller:**
  - 16Bit Data Bus
  - Supports 2 to 128MB SDRAM
  - Supports static memory (Flash ROM/SRAM). (Maximum capacity: 4MB)
  - 3 Chip Select pins (typically for SDRAM, Flash EEPROM and another chip).
- **CF Card Interface:**
  - CF+ Specification Rev.1.4 compliant.
  - Can be used as the interface of wireless LAN, Memory card, etc.
  - Supports True IDE interface
- **Standby function:**
  - The HALT function to stop the CPU clock when CPU operation is not required.
  - Programmable I/O clock stop function for major I/O block clocks.
- **Timer, Watchdog Timer:**
  - 16-Bit timer × 3 channels
  - Re-load/Cyclic or One Shot Operation Mode
  - Supports toggle outputs from timer underflow.
  - Interrupt output or re-settable watchdog timer.
- **Serial Interface:**
  - UART: 16550 Software compatible × 1 channel
  - SPI: Clock synchronous type × 3 channels
  - I^2C master interface (camera Interface and multipurpose use)
- **Interrupt Controller:**
  - Supports 32 IRQs and 2 FIQs.

- **Real Time Clock:**
  - Supports day, hour, minute and second.
  - The internal timer tap from 1/128 to 1/2 can be used as the interrupt source
  - Supports alarm function and interrupt.
- **GPIO:**
  - General-purpose I/O port (up to 57 ports)
  - Directions programmable for all ports.
  - Some ports are shared with other I/O functions.
- **Power Supply:**
  - 3.3V (I/O power supply)
  - 1.8V (Core power supply)
  - 1.8V (Analog power supply for PLL)
  - 2.4V – 3.6V (Camera I/O power supply)
- **Package:**
  - TQFP 144 Pin (TQFP24): 16 × 16 × 1mm, 0.4mm Pin pitch

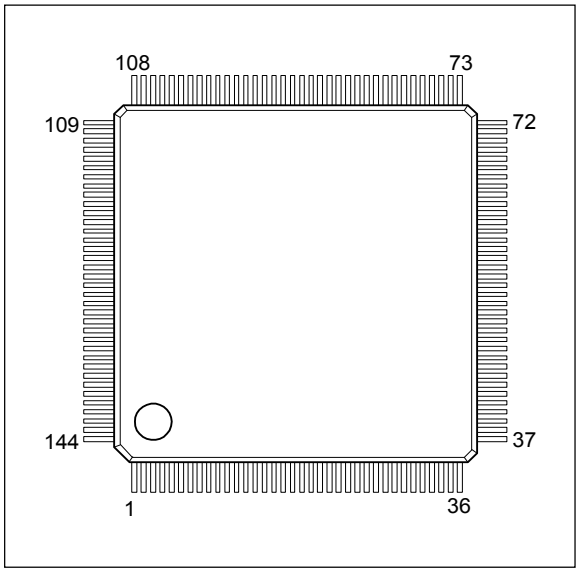
■ SUPPORTING PROTOCOLS

ARP, ICMP, IP, TCP, UDP, HTTPd, SMTP, DHCP*, FTP*, DNS resolver*, telnet*
Necessary protocols can be added or updated by rewriting Flash ROM.
*: Sample code.

■ BLOCK DIAGRAM



■ PIN ASSIGNMENT



Pin No.	Pin Name	Pin No.	Pin Name
1	MA14	37	MD12
2	MA15	38	MD13
3	MA16	39	MD14
4	MA17	40	MD15
5	MA18	41	MDQML
6	VSS	42	MDQMH
7	MA19	43	HVDD1
8	MCS2#	44	VSS
9	MCS1#	45	MII_CRS
10	MCS0#	46	MII_COL
11	LVDD	47	MII_TXD3
12	MOE#	48	MII_TXD2
13	MWE0#	49	MII_TXD1
14	MWE1#	50	LVDD
15	HVDD1	51	MII_TXD0
16	MCLKEN	52	MII_TXEN
17	MCLK	53	MII_TXCLK
18	VSS	54	MII_RXER
19	MRAS#	55	VSS
20	MCAS#	56	HVDD1
21	MD0	57	MII_RXCLK
22	MD1	58	MII_RXDV
23	MD2	59	MII_RXD0
24	MD3	60	MII_RXD1
25	VSS	61	LVDD
26	LVDD	62	MII_RXD2
27	MD4	63	MII_RXD3
28	MD5	64	MII_MDC
29	MD6	65	MII_MDIO
30	MD7	66	VSS
31	HVDD1	67	CLKI
32	MD8	68	PLLVSS
33	MD9	69	VCP
34	MD10	70	PLLVDD
35	MD11	71	RESET#
36	VSS	72	TESTEN

Pin No.	Pin Name	Pin No.	Pin Name
73	TRST#	109	CMDATA5
74	TCK	110	CMDATA6
75	TMS	111	CMDATA7
76	TDI	112	VSS
77	TDO	113	LVDD
78	VSS	114	GPIOD0
79	GPIOA0	115	GPIOD1
80	GPIOA1	116	CFCE2#
81	GPIOA2	117	CFCE1#
82	GPIOA3	118	CFIORD#
83	GPIOA4	119	CFIOWR#
84	GPIOA5	120	CFIREQ
85	GPIOA6	121	CFRST
86	GPIOA7	122	VSS
87	HVDD1	123	HVDD1
88	VSS	124	CFWAIT#
89	GPIOB0	125	CFSTSCHG#
90	GPIOB1	126	CFDEN#
91	GPIOB2	127	CFDDIR
92	GPIOB3	128	MA0
93	LVDD	129	MA1
94	GPIOB4	130	MA2
95	GPIOB5	131	MA3
96	GPIOB6	132	VSS
97	GPIOB7	133	LVDD
98	VSS	134	MA4
99	CMHREF	135	MA5
100	CMVREF	136	MA6
101	CMCLKIN	137	MA7
102	CMCLKOUT	138	MA8
103	CMDATA0	139	HVDD1
104	CMDATA1	140	MA9
105	HVDD2	141	MA10
106	CMDATA2	142	MA11
107	CMDATA3	143	MA12
108	CMDATA4	144	MA13

Note: # at the right end of a pin name indicates a low active signal.

■ PIN DESCRIPTION

#: # at the right end of a pin name indicates a low active signal.
I: Input pin
O: Output pin
IO: Bi-directional pin
P: Power Supply

Cell Type Description

Cell Type	Description	Applicable pin example
ICS	LVCMOS Schmitt input	TCK, CLKI, RESET#
ICD1	LVCMOS input with pull down resistor (50kΩ@3.3V)	TESTEN
ICU1	LVCMOS input with pull up resistor (50kΩ@3.3V)	TMS, TDI
ICSU1	LVCMOS Schmitt input with pull up resistor	TRST#
BLNC4	Low noise LVCMOS IO buffer (±4mA)	MII
BLNC4U1	Low noise LVCMOS IO buffer with pull-up resistor (50kΩ@3.3V) (±4mA)	CF Interface
BLNC4D2	Low noise LVCMOS IO buffer with pull-down resistor (100kΩ@3.3V) (±4mA)	MD [15:0]
BLNS4	Low noise LVCMOS Schmitt IO buffer (±4mA)	GPIOA, GPIOB, GPIOD [1:0]
BLNS4D1	Low noise LVCMOS Schmitt IO buffer with pull-down resistor (50kΩ@3.0V) (±4mA)	Camera Interface
OLN4	Low noise output buffer (±4mA)	MIC Interface (excluding MD)
OTLN4	Low noise Tri-state output buffer (±4mA)	TDO
OLTR	Low Voltage Transparent Output	VCP

Pin Description

Pin Name	Type	Cell Type	Pin No.	Description
(MA [21:20])	(I/O)	(BLNS4)	(114-115)	See GPIOD [1:0] for more detail of these pins.
MA [19:12]	O	OLN4	7, 1-5, 143-144	**Address outputs [19:12]** Out of these, MA [15:14] become BA [1:0] as a bank address, when using SDRAM
MA 11	O	OLN4	142	This pin has the following functions: ・**MA11**: Address output 11 (Default pin function) ・**CFREG# output** During the CompactFlash (CF) cycles, this signal behaves as the REG# signal selecting attribute or I/O space of the CF card.
MA [10:0]	O	OLN4	128-131, 134-138, 140-141	These pins have the following functions: ・**MA [10:0]**: Address outputs [10:0] (Default pin function) ・**CFADDR [10:0] outputs** During the CF cycles, these signals become the CF interface address signal [10:0].
MD [15:0]	I/O	BLNC4D2	21-24, 27-30, 32-35, 37-40	These pins have the following functions: ・**16-bit Data bus for memory** (Default pin function) ・**Data Bus for CF Card.** ・**MODESEL [15:0]** At the power ON reset time (RESET# is changed from LOW to HIGH), these pins are sampled to determine the internal operation mode. See "SYSTEM CONFIGURATION by MODESEL PIN" for more details. To determine the operation mode, a pull-up resistance may be required externally. (Resistor value: 4.7kΩ to 10kΩ range)
MCS [2:0]#	O	OLN4	8-10	**Chip select signals for memory (SDRAM and static memories)** (Low active) Use MCS2# to support an SDRAM
MOE#	O	OLN4	12	This pin has the following functions (Low active) ・**MOE#**: Read strobe signal for memory read cycle. (Default pin function) ・**CFOE#**: Enable signal for CF read cycle During the CF cycle, this signal becomes output enable signal for CF common memory or attribute space access.

Pin Name	Type	Cell Type	Pin No.	Description
MWE0#	O	OLN4	13	This pin has the following functions (Low active): ・**MWE0#**: Write enable signal for memory (for static memory) (Default pin function) ・**CFWE# output** During the CF cycle, this signal becomes write enable signal for CF common memory or attribute space access.
MWE1#	O	OLN4	14	**Write Enable signal for memory** (for SDRAM) (Low active)
MCLK	O	OLN4	17	**Clock output signal for SDRAM** Outputs the same frequency as the Internal Operating Frequency (CPUCLK).
MCLKEN	O	OLN4	16	**Clock enable signal for SDRAM**
MRAS#	O	OLN4	19	**RAS signal for SDRAM** (Low active)
MCAS#	O	OLN4	20	**CAS signal for SDRAM** (Low active)
MDQML MDQMH	O	OLN4	41-42	These pins have the following functions: ・**Byte enable signal** (for static memory) ・**DQM signal for SDRAM** MDQML and MDQMH correspond to lower byte and higher byte respectively.
MII_TXCLK	I/O	BLNC4	53	This pin has the following functions: ・**MII_TXCLK**: Clock TXCLK input for transmit data from Media Independent Interface Ethernet PHY (hereafter referred to as MII PHY) (Default pin function, “Function 1”) ・**GPIOF7 input/output**
MII_TXEN	I/O	BLNC4	52	This pin has the following functions: ・**MII_TXEN**: Transmit output enable TXEN output to MII PHY (Default pin function, “Function 1”) ・**GPIOF6 input/output** ・**SPI2_SCLK**: Serial clock for SPI2 (Select “Function 2”)
MII_TXD3	I/O	BLNC4	47	This pin has the following functions: ・**MII_TXD3**: Transmit data TXD3 output to MII PHY (Default pin function, “Function 1”) ・**GPIOF2 input/output** ・**SPI1_SCLK**: Serial clock for SPI1 (Select “Function 2”)
MII_TXD2	I/O	BLNC4	48	This pin has the following functions: ・**MII_TXD2**: Transmit data TXD2 output to MII PHY (Default pin function, “Function 1”) ・**GPIOF3 input/output** ・**SPI1_MOSI**: Master Out/Slave In for SPI1 (Select “Function 2”)
MII_TXD1	I/O	BLNC4	49	This pin has the following functions: ・**MII_TXD1**: Transmit data TXD1 output to MII PHY (Default pin function, “Function 1”) ・**GPIOF4 input/output** ・**SPI2_SS**: Chip select signal for SPI2 (Select “Function 2”)
MII_TXD0	I/O	BLNC4	51	This pin has the following functions: ・**MII_TXD0**: Transmit data TXD0 output to MII PHY (Default pin function, “Function 1”) ・**GPIOF5 input/output** ・**SPI2_MOSI**: Master Out/Slave In for SPI2 (Select “Function 2”)
MII_RXCLK	I/O	BLNC4	57	This pin has the following functions: ・**MII_RXCLK**: Receive data clock RXCLK input from MII PHY (Default pin function, “Function 1”) ・**GPIOG1 input/output**
MII_COL	I/O	BLNC4	46	This pin has the following functions: ・**MII_COL**: Collision detection COL input from MII PHY (Default pin function, “Function 1”) ・**GPIOF1 input/output** ・**SPI1_MISO**: Master In/Slave Out for SPI1 (Select “Function 2”)
MII_CRS	I/O	BLNC4	45	This pin has the following functions: ・**MII_CRS**: Carrier sense CRS input from MII PHY (Default pin function, “Function 1”) ・**GPIOF0 input/output** ・**SPI1_SS**: Chip select signal for SPI1 (Select “Function 2”)
MII_RXDV	I/O	BLNC4	58	This pin has the following functions: ・**MII_RXDV**: Receive data valid RXDV input from MII PHY (Default pin function, “Function 1”) ・**GPIOG2 input/output**

Pin Name	Type	Cell Type	Pin No.	Description
MII_RXD [3:0]	I/O	BLNC4	59-60, 62-63	These pins have the following functions: ・**MII_RXD [3:0]**: Receive data RXD [3:0] input from MII PHY (Default pin function, "Function 1") ・**GPIOG [6:3] input/output**
MII_RXER	I/O	BLNC4	54	This pin has the following functions: ・**MII_RXER**: Receive error RXER for MII PHY (Default pin function, "Function 1") ・**GPIOG0 input/output**
MII_MDC	I/O	BLNC4	64	This pin has the following functions: ・**MII_MDC**: Management interface clock MDC for MII PHY (Default pin function, "Function 1") ・**GPIOG7 input/output**
MII_MDIO	I/O	BLNC4	65	This pin has the following functions: ・**MII_MDIO**: Management interface Data MDIO input/output for MII PHY (Default pin function, "Function 1") ・**GPIOH0 input/output** ・**SPI2_MISO**: Master In/Slave Out for SPI2 (Select "Function 2")
CMDATA [7:0]	I/O	BLNS4D1	103-104, 106-111	These pins have the following functions: ・**CMDATA [7:0]**: YUV data from camera (Select "Function 1") After reset, theses pins become GPIOC [7:0] input. To use as the CMDATA [7:0] pin, select "Function 1" in the Bit [15:0] of the GPIOC pin function register. ・**GPIOC [7:0] inputs/outputs** (Default pin function)
CMVREF	I/O	BLNS4D1	100	This pin has the following functions: ・**CMVREF**: Vertical sync input from camera (Select "Function 1") After reset, this pin becomes GPIOD4 input. To use as the CMVREF pin, select "Function 1" in the Bit [9:8] of the GPIOD pin function register. ・**GPIOD4 input/output** (Default pin function)
CMHREF	I/O	BLNS4D1	99	This pin has the following functions: ・**CMHREF**: Horizontal sync input from camera (Select "Function 1") After reset, this pin becomes GPIOD5 input. To use as the CMHREF pin, select "Function 1" in the Bit [11:10] of the GPIOD pin function register. ・**GPIOD5 input/output** (Default pin function)
CMCLKOUT	I/O	BLNS4D1	102	This pin has the following functions: ・**CMCLKOUT**: Basic clock output to camera (Select "Function 1") After reset, this pin becomes GPIOD6 input. To use as the CMCLKOUT pin, select "Function 1" in the Bit [13:12] of the GPIOD pin function register. ・**GPIOD6 input/output** (Default pin function)
CMCLKIN	I/O	BLNS4D1	101	This pin has the following functions: ・**CMCLKIN**: Pixel clock input from camera (Select "Function 1") After reset, this pin becomes GPIOD7 input. To use as the CMCLKIN pin, select "Function 1" in the Bit [15:14] of the GPIOD pin function register. ・**GPIOD7 input/output** (Default pin function)
CFCE2#	I/O	BLNC4U1	116	This pin has the following functions: ・**CFCE2#**: Card Enable 2 CE2# for CompactFlash card Interface (hereafter referred to as CF) (Low active; Select "Function 1") After reset, this pin becomes GPIOD2 input. To use as the CFCE2# pin, select "Function 1" in the Bit [5:4] of the GPIOD pin function register. ・**GPIOD2 input/output** (Default pin function)
CFCE1#	I/O	BLNC4U1	117	This pin has the following functions: ・**CFCE1#**: Card Enable 1 CE1# for CF (Low active; Select "Function 1"). After reset, this pin becomes GPIOD3 input. To use as the CFCE1# pin, select "Function1" in the Bit [7:6] of the GPIOD pin function register. ・**GPIOD3 input/output** (Default pin function)
CFIORD#	I/O	BLNC4U1	118	This pin has the following functions: ・**CFIORD#**: IO Read strove signal for CF (Low active; Select "Function 1") After reset, this pin becomes GPIOE0 input. To use as the CFIORD# pin, select "Function 1" in the Bit [1:0] of the GPIOE pin function register. ・**GPIOE0 input/output** (Default pin function)
CFIOWR#	I/O	BLNC4U1	119	This pin has the following functions: ・**CFIOWR#**: IO Write strove signal for CF (Low active; Select "Function 1") After reset, this pin becomes GPIOE1 input. To use as the CFIOWR# pin, select "Function 1" in the Bit [3:2] of the GPIOE pin function register. ・**GPIOE1 input/output** (Default pin function)

Pin Name	Type	Cell Type	Pin No.	Description
CFWAIT#	I/O	BLNC4U1	124	This pin has the following functions: ・**CFWAIT#**: Wait request input from CF (Low active; Select "Function 1") After reset, this pin becomes GPIOE2 input. To use as the CFWAIT# pin, select "Function 1" in the Bit [5:4] of the GPIOE pin function register. ・**GPIOE2 input/output** (Default pin function)
CFRST	I/O	BLNC4U1	121	This pin has the following functions: ・**CFRST**: Reset signal to CF card (Select "Function 1") The signal is HIGH when the card is reset and LOW when the card is under normal operation. After reset, this pin becomes GPIOE3 input. To use as the CFRST pin, select "Function 1" in the Bit [7:6] of the GPIOE pin function register. ・**GPIOE3 input/output** (Default pin function)
CFIREQ	I/O	BLNC4U1	120	This pin has the following functions: ・**CFIREQ**: Interrupt request signal from CF card (Select "Function 1") After reset, this pin becomes GPIOE4 input. To use as the CFIREQ pin, select "Function 1" in the Bit [9:8] of the GPIOE pin function register. ・**GPIOE4 input/output** (Default pin function)
CFSTSCHG#	I/O	BLNC4U1	125	This pin has the following functions: ・**CFSTSCHG#**: Status change signal from CF card (Low active; Select "Function 1") After reset, this pin becomes GPIOE5 input. To use as the CFSTSCHG# pin, select "Function 1" in the Bit [11:10] of the GPIOE pin function register. ・**GPIOE5 input/output** (Default pin function)
CFDEN#	I/O	BLNC4U1	126	This pin has the following functions: ・**CFDEN#**: CF Data Bus enable signal of CF card for external buffer (Low active; Select "Function 1") After reset, this pin becomes GPIOE6 input. To use as the CFDEN# pin, select "Function 1" in the Bit [13:12] of the GPIOE pin function register. ・**GPIOE6 input/output** (Default pin function)
CFDDIR	I/O	BLNC4U1	127	This pin has the following functions: ・**CFDDIR**: Data Bus Direction signal for CF. (Select "Function 1") When CF data is read, this pin becomes low. After reset, this pin becomes GPIOE7 input. To use as the CFDDIR pin, select "Function 1" in the Bit [15:14] of the GPIOE pin function register. ・**GPIOE7 input/output** (Default pin function)
GPIOA0	I/O	BLNS4	79	This pin has the following functions: ・**GPIOA0 input/output** (Default pin function) ・**TXD0**: UART transmit data output (Select "Function 1") ・**SPI2_SCLK**: Serial clock for SPI2 (Select "Function 2")
GPIOA1	I/O	BLNS4	80	This pin has the following functions: ・**GPIOA1 input/output** (Default pin function) ・**RXD0**: UART receive data input (Select "Function 1") ・**SPI2_SS**: Chip select signal for SPI2 (Select "Function 2")
GPIOA2	I/O	BLNS4	81	This pin has the following functions: ・**GPIOA2 input/output** (Default pin function) ・**SPI0_SS**: Chip select signal for SPI0 (Select "Function 1")
GPIOA3	I/O	BLNS4	82	This pin has the following functions: ・**GPIOA3 input/output** (Default pin function) ・**SPI0_SCLK**: Serial clock for SPI0 (Select "Function 1")
GPIOA4	I/O	BLNS4	83	This pin has the following functions: ・**GPIOA4 input/output** (Default pin function) ・**SPI0_MISO**: Master In/Slave Out for SPI0 (Select "Function 1")
GPIOA5	I/O	BLNS4	84	This pin has the following functions: ・**GPIOA5 input/output** (Default pin function) ・**SPI0_MOSI**: Master Out/Slave In for SPI0 (Select "Function 1")
GPIOA6	I/O	BLNS4	85	This pin has the following functions: ・**GPIOA6 input/output** (Default pin function) ・**SCL**: Serial clock input/output for I^2C (Select "Function 1")
GPIOA7	I/O	BLNS4	86	This pin has the following functions: ・**GPIOA7 input/output** (Default pin function) ・**SDA**: Serial data input/output for I^2C (Select "Function 1")

Pin Name	Type	Cell Type	Pin No.	Description
GPIOB0	I/O	BLNS4	89	This pin has the following functions: · **GPIOB0 input/output** (Default pin function) · **IINT0 input** · **SPI1_SS**: Chip select signal for SPI1 (Select "Function 2")
GPIOB1	I/O	BLNS4	90	This pin has the following functions: · **GPIOB1 input/output** (Default pin function) · **INT1 input** · **RTS#**: UART request to send output (Select "Function 1") · **SPI1_SCLK**: Serial clock for SPI1 (Select "Function 2")
GPIOB2	I/O	BLNS4	91	This pin has the following functions: · **GPIOB2 input/output** (Default pin function) · **INT2 input** · **CTS#**: UART clear to send input (Select "Function 1") · **SPI1_MISO**: Master In/Slave Out for SPI1 (Select "Function 2")
GPIOB3	I/O	BLNS4	92	This pin has the following functions: · **GPIOB3 input/output** (Default pin function) · **INT3 input** · **Timer0 output** (Select "Function 1") · **SPI1_MOSI**: Master Out/Slave In for SPI1 (Select "Function 2")
GPIOB4	I/O	BLNS4	94	This pin has the following functions: · **GPIOB4 input/output** (Default pin function) · **INT4 input** · **Timer1 output** (Select "Function 1")
GPIOB5	I/O	BLNS4	95	This pin has the following functions: · **GPIOB5 input/output** (Default pin function) · **INT5 input** · **Timer2 output** (Select "Function 1")
GPIOB6	I/O	BLNS4	96	This pin has the following functions: · **GPIOB6 input/output** (Default pin function) · **INT6 input** · **SPI2_MOSI**: Master Out/Slave In for SPI2 (Select "Function 1")
GPIOB7	I/O	BLNS4	97	This pin has the following functions: · **GPIOB7 input/output** (Default pin function) · **INT7 input** · **SPI2_MISO**: Master In/Slave Out for SPI2 (Select "Function 1")
GPIOD0	I/O	BLNS4	114	This pin has the following functions: · **GPIOD0 input/output** (Default pin function) · **INT8 input** · **MA20**: Address output 20 (Select "Function 1")
GPIOD1	I/O	BLNS4	115	This pin has the following functions: · **GPIOD1 input/output** (Default pin function) · **MA21**: Address output 21 (Select "Function 1")
CLKI	I	ICS	67	**32.768kHz Clock Input** Basic clock input to this chip. This clock is used as reference clock input for internal PLL to generate system clock. This pin has a Schmitt trigger input buffer.
VCP	O	OLTR	69	**Test Pin for Built-in PLL** This pin is used to monitor the PLL output when conducting a test. Make this pin open for normal operation.
TRST#	I	ICSU1	73	**Reset input for JTAG Interface** (Low active) This pin has a Schmitt trigger input buffer with pull-up resistor.
TCK	I	ICS	74	**Clock Input Pin for JTAG Interface** This pin has a Schmitt trigger input buffer.
TMS	I	ICU1	75	**TMS Pin for JTAG Interface** This pin has a built-in pull-up resistor.
TDI	I	ICU1	76	**Serial Data Input Pin for JTAG Interface** This pin has a built-in pull-up resistor.
TDO	O	OTLN4	77	**Serial Data Output Pin for JTAG Interface**
TESTEN	I	ICD1	72	**Test Enable** (High active) This pin has a built-in pull-down resistor. Connect this pin to VSS or make it open for normal operation.
RESET#	I	ICS	71	**System Reset Signal** (Low active) Even after HVDD1 and LVDD become stable at power on, keep RESET# active (LOW) for 100ms.

Pin Name	Type	Cell Type	Pin No.	Description
HVDD1	P	P	15, 31, 43, 56, 87, 123, 139	**Power supply for I/O cell** : 3.3V (Excluding camera interface)
HVDD2	P	P	105	**Power supply for camera interface:** 3.0V (Typical) 2.4V (Min.) - 3.6V (Max.)
LVDD	P	P	11, 26, 50, 61, 93, 113, 133	**Power supply for core (internal)**: 1.8V
PLLVDD	P	P	70	**Power supply for analog (PLL)**: 1.8V It is necessary to handle this as an analog power supply. Provides low noise and a stable power supply.
PLLVSS	P	P	68	**Ground for analog (PLL)** It is necessary to handle this as an analog power supply. Provides low noise and a stable ground.
VSS	P	P	6, 18, 25, 36, 44, 55, 66, 78, 88, 98, 112, 122, 132	**Common Ground for I/O cells, camera interface and core power supplies**

■ SYSTEM CONFIGURATION by MODESEL PIN

Pin Name	Pin Function	Value at resetting	
		0	1
MD0	MODESEL0	32kHz Mode	Reserved (for test) *
MD1	MODESEL1	Little Endian	Reserved (Big Endian)
MD2	MODESEL2	Normal operation	Reserved (for test) *
MD3	MODESEL3	Reserved (Use “0.”)	
MD4	MODESEL4	For USER setting Set values are reflected to the chip configuration register inside the system controller. Users can use these bits for their own purpose.	
MD5	MODESEL5		
MD6	MODESEL6		
MD7	MODESEL7		
MD8	MODESEL8	Reserved (Use “0.”)	
MD9	MODESEL9	Reserved (Use “0.”)	
MD10	MODESEL10	Reserved (Use “0.”)	
MD11	MODESEL11	Reserved (Use “0.”)	
MD12	MODESEL12	Reserved (Use “0.”)	
MD13	MODESEL13	Reserved (Use “0.”)	
MD14	MODESEL14	Reserved (Use “0.”)	
MD15	MODESEL15	Reserved (Use “0.”)	

* **Note :** Do not configure the system using the “Reserved” value. IC may be damaged.

■ PHYSICAL SPECIFICATION

Item		Features
Power supply	Core system power supply (LVDD)	1.8V ± 0.15V
	I/O system power supply (HVDD1)	3.3V ± 0.30V
	Camera interface power supply (HVDD2)	2.4V (Min.) – 3.6V (Max.)
	PLL power supply (PLLVDD)	1.8V ± 0.15V
Operating frequency	CPU	50MHz Max.
Power consumption (reference value)		140mW (Typ.), 3mW (When the status is HALT and MII Interface stopped)
Operative temperature		T_a = -40 to +85°C
Package		TQFP 144 pin (TQFP24) 16 × 16 × 1 mm / 0.4mm Pin pitch

■ MULTIPLEX PIN FUNCTION OF GPIO PIN AND PIN FUNCTION AFTER RESETTING

S1S65000 Pin Name	Pin Function after Reset	GPIO	INT	Address bus	UART	I^2C	SPI [2:0]	Timer	Camera Interface	CF card	MII
GPIOA0	GPIOA0	GPIOA0			TXD0		SPI2_SCLK				
GPIOA1	GPIOA1	GPIOA1			RXD0		SPI2_SS				
GPIOA2	GPIOA2	GPIOA2					SPI0_SS				
GPIOA3	GPIOA3	GPIOA3					SPI0_SCLK				
GPIOA4	GPIOA4	GPIOA4					SPI0_MISO				
GPIOA5	GPIOA5	GPIOA5					SPI0_MOSI				
GPIOA6	GPIOA6	GPIOA6				SCL					
GPIOA7	GPIOA7	GPIOA7				SDA					
GPIOB0	GPIOB0	GPIOB0	INT0				SPI1_SS				
GPIOB1	GPIOB1	GPIOB1	INT1		RTS#		SPI1_SCLK				
GPIOB2	GPIOB2	GPIOB2	INT2		CTS#		SPI1_MISO				
GPIOB3	GPIOB3	GPIOB3	INT3				SPI1_MOSI	Timer0out			
GPIOB4	GPIOB4	GPIOB4	INT4					Timer1out			
GPIOB5	GPIOB5	GPIOB5	INT5					Timer2out			
GPIOB6	GPIOB6	GPIOB6	INT6				SPI2_MOSI				
GPIOB7	GPIOB7	GPIOB7	INT7				SPI2_MISO				
CMDATA0	GPIOC0	GPIOC0							CMDATA0		
CMDATA1	GPIOC1	GPIOC1							CMDATA1		
CMDATA2	GPIOC2	GPIOC2							CMDATA2		
CMDATA3	GPIOC3	GPIOC3							CMDATA3		
CMDATA4	GPIOC4	GPIOC4							CMDATA4		
CMDATA5	GPIOC5	GPIOC5							CMDATA5		
CMDATA6	GPIOC6	GPIOC6							CMDATA6		
CMDATA7	GPIOC7	GPIOC7							CMDATA7		
GPIOD0	GPIOD0	GPIOD0	INT8	MA20							
GPIOD1	GPIOD1	GPIOD1		MA21							
CFCE2#	GPIOD2	GPIOD2								CFCE2#	
CFCE1#	GPIOD3	GPIOD3								CFCE1#	
CMVREF	GPIOD4	GPIOD4							CMVREF		
CMHREF	GPIOD5	GPIOD5							CMHREF		
CMCLKOUT	GPIOD6	GPIOD6							CMCLKOUT		
CMCLKIN	GPIOD7	GPIOD7							CMCLKIN		
CFIORD#	GPIOE0	GPIOE0								CFIORD#	
CFIOWR#	GPIOE1	GPIOE1								CFIOWR#	
CFWAIT#	GPIOE2	GPIOE2								CFWAIT#	
CFRST	GPIOE3	GPIOE3								CFRST	
CFIREQ	GPIOE4	GPIOE4								CFIREQ	
CFSTSCHG#	GPIOE5	GPIOE5								CFSTSCHG#	
CFDEN#	GPIOE6	GPIOE6								CFDEN#	
CFDDIR	GPIOE7	GPIOE7								CFDDIR	
MII_CRS	MII_CRS	GPIOF0					SPI1_SS				MII_CRS
MII_COL	MII_COL	GPIOF1					SPI1_MISO				MII_COL
MII_TXD3	MII_TXD3	GPIOF2					SPI1_SCLK				MII_TXD3
MII_TXD2	MII_TXD2	GPIOF3					SPI1_MOSI				MII_TXD2
MII_TXD1	MII_TXD1	GPIOF4					SPI2_SS				MII_TXD1
MII_TXD0	MII_TXD0	GPIOF5					SPI2_MOSI				MII_TXD0
MII_TXEN	MII_TXEN	GPIOF6					SPI2_SCLK				MII_TXEN
MII_TXCLK	MII_TXCLK	GPIOF7									MII_TXCLK
MII_RXER	MII_RXER	GPIOG0									MII_RXER
MII_RXCLK	MII_RXCLK	GPIOG1									MII_RXCLK
MII_RXDV	MII_RXDV	GPIOG2									MII_RXDV
MII_RXD0	MII_RXD0	GPIOG3									MII_RXD0
MII_RXD1	MII_RXD1	GPIOG4									MII_RXD1
MII_RXD2	MII_RXD2	GPIOG5									MII_RXD2
MII_RXD3	MII_RXD3	GPIOG6									MII_RXD3
MII_MDC	MII_MDC	GPIOG7									MII_MDC
MII_MDIO	MII_MDIO	GPIOH0					SPI2_MISO				MII_MDIO

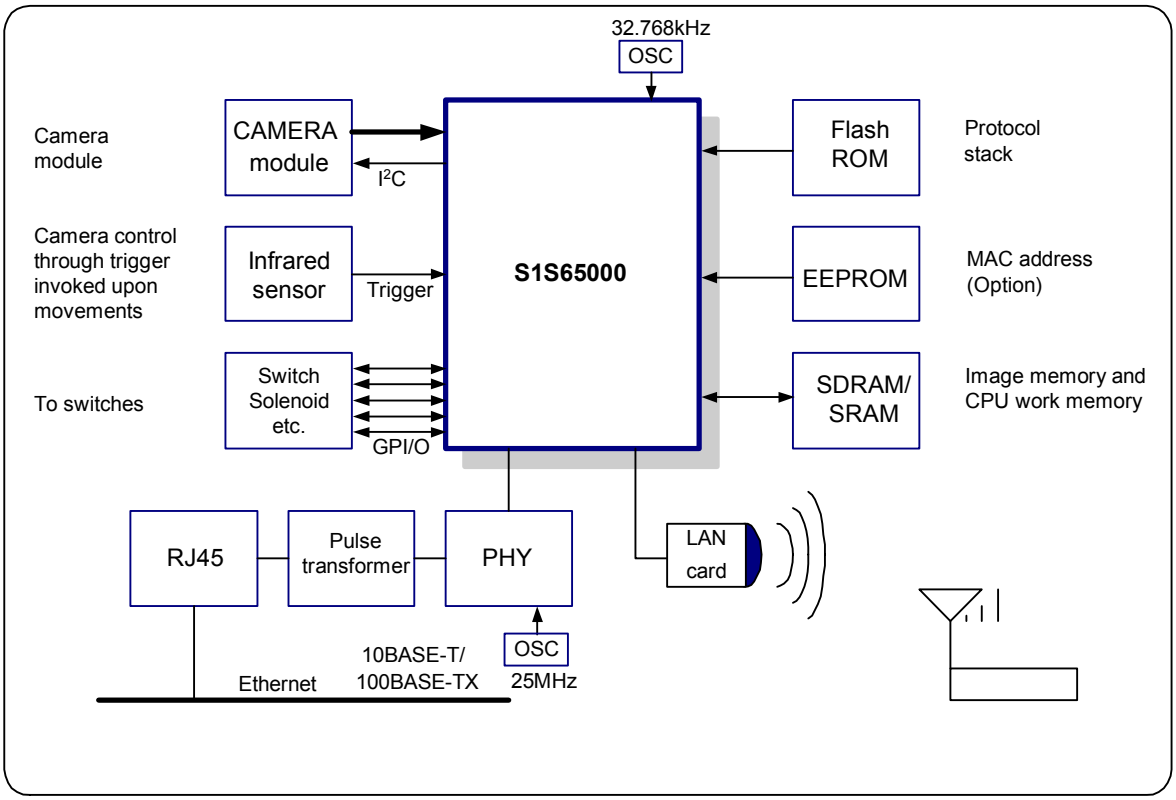
Function 1 : Function 1 Function 2 : Function 2

■ CONDITION OF PIN DURING RESETTING AND AFTER RESETTING

Pin Name	Direction during reset	Value during reset	Value after reset	Internal Resistor	Description
MA [19:0]	Output	LOW	—	None	
MD [15:0]	Input	LOW	LOW	Pull Down Resistor	100kΩ
MCS [2:0]#	Output	HIGH	—	None	
MOE#	Output	HIGH	—	None	
MWE0#	Output	HIGH	—	None	
MWE1#	Output	HIGH	—	None	
MCLK	Output	LOW	—	None	
MCLKEN	Output	LOW	—	None	
MRAS#	Output	HIGH	—	None	
MCAS#	Output	HIGH	—	None	
MDQML	Output	LOW	—	None	
MDQMH	Output	LOW	—	None	
MII_TXCLK	Input	High-Z	High-Z	None	Depend on the external circuit, generally MII-PHY
MII_TXEN	Output	LOW	LOW	None	
MII_TXD [3:0]	Output	Undetermined	Undetermined	None	Undetermined until initializing
MII_RXCLK	Input	High-Z	High-Z	None	Depend on the external circuit, generally MII-PHY
MII_COL	Input	High-Z	High-Z	None	Depend on the external circuit, generally MII-PHY
MII_CRS	Input	High-Z	High-Z	None	Depend on the external circuit, generally MII-PHY
MII_RXDV	Input	High-Z	High-Z	None	Depend on the external circuit, generally MII-PHY
MII_RXD [3:0]	Input	High-Z	High-Z	None	Depend on the external circuit, generally MII-PHY
MII_RXER	Input	High-Z	High-Z	None	Depend on the external circuit, generally MII-PHY
MII_MDC	Output	LOW	—	None	
MII_MDIO	Input	High-Z	High-Z	None	Depend on the external circuit, generally MII-PHY
CMDATA [7:0]	Input	LOW	LOW	Pull Down Resistor	50kΩ
CMVREF	Input	LOW	LOW	Pull Down Resistor	50kΩ
CMHREF	Input	LOW	LOW	Pull Down Resistor	50kΩ
CMCLKOUT	Input	LOW	LOW	Pull Down Resistor	50kΩ
CMCLKIN	Input	LOW	LOW	Pull Down Resistor	50kΩ
CFCE2#	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
CFCE1#	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
CFIORD#	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
CFIOWR#	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
CFWAIT#	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
CFRST	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
CFIREQ	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
CFSTSCHG#	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
CFDEN#	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
CFDDIR	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
GPIOA [7:0]	Input	High-Z	High-Z	None	Depend on the external circuit
GPIOB [7:0]	Input	High-Z	High-Z	None	Depend on the external circuit
GPIOD [1:0]	Input	High-Z	High-Z	None	Depend on the external circuit
CLKI	Input	High-Z	High-Z	None	
VCP	Output	High-Z	High-Z	None	Remain in the Open state to use
TRST#	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
TCK	Input	High-Z	High-Z	None	
TMS	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
TDI	Input	HIGH	HIGH	Pull Up Resistor	50kΩ
TDO	Output	High-Z	High-Z	None	
TESTEN	Input	LOW	LOW	Pull Down Resistor	50kΩ
RESET#	Input	LOW	HIGH	None	

S1S65000

■ USAGE EXAMPLE



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