Agilent Technologies
Innovating the HP Way

TACHYON
Fibre Channel Interface Controller

Technical Data

HPFC-5000

Features

- **Supports 1063, 531, and 266 Mbaud Link Speeds**
- **Supports Fibre Channel Class 1, 2, and 3 Services**
- **Supports Fibre Channel Arbitrated Loop (FC-AL), Point-to-Point, and Fabric (Crosspoint-Switched) Topologies**
- **Compliant with the Fibre Channel Physical and Signaling Interface (FC-PH)**
- **Complies to Fibre Channel System Initiative (FCSI) Profiles**
- **Provides Complete Support of Both Networking and Mass Storage Connections**
- **Supports up to 2-Kbyte Frame Payload Size for All Classes of Service**
- **Manages Sequence Segmentation and Reassembly in the Hardware**
- **Supports up to 16,384 Concurrent SCSI I/O Transactions**
- **Provides FCP Assists for SCSI Initiators and Targets**
- **Processes Inbound and Outbound Data Simultaneously Due to Full Duplex Internal Architecture**
- **Interfaces Directly to Industry and ANSI Standard 10-bit and 20-bit FC-0 Physical Link Modules**
- **Supports Open Broadcast Replicate Transmission and Reception of FC-AL**
- **Supports Reception of Fabric-Addressed Frames for a Fibre Channel Services Server on FC-AL**
- **3.3 V Power Supply**

Applications

- **Mass Storage System I/O Channel**
- **Computer System I/O Channel**
- **High Speed Peripheral Interface**
- **Fibre Channel I/O for Network Switches and Hubs**

Description

Tachyon provides a very highly integrated Fibre Channel (FC) interface controller in a single chip solution. It supports both networking and mass storage over a single host connection. In addition, Tachyon provides a high performance controller at an inexpensive cost due to its significant number of design features.

Tachyon is packaged in a 208 pin Metal Quad (MQuad®) flat pack.

Table of Contents

1. Fibre Channel General Information

Fibre Channel supports both networking and mass storage interconnections. The Fibre Channel standard defines a number of encapsulation methods. These methods enable both networking and mass storage protocols to be transported over a single Fibre Channel physical interface. This Fibre Channel General Information section gives an overview of the Fibre Channel data hierachy and describes how Tachyon manages networking and mass storage (particularly SCSI) devices.

1.1 Fibre Channel Data Hierarchy

Fibre Channel technology defines a hierarchical structure for data transactions. The data terminology of this hierarchy is defined below:

Exchange

The exchange is the highest level of the data transaction hierarchy. The exchange defines a conversation occurring between two nodes. This conversation can be a long or short term interchange of information. An exchange consists of one or more sequences. An exchange is also known as an I/O transaction.

Sequence

The sequence in Fibre Channel protocol correlates to a data packet or datagram in networking protocols. A sequence consists of a set of one or more frames. Each frame of a particular sequence contains a common Sequence_ID. A node sends frames of a sequence unidirectionally to the remote node. The sequence includes the corresponding Link Control frames (e.g., ACKs, BSYs, RJTs, etc.) that may be sent from the remote node.

A sequence can be any length, but to satisfy various timing and complexity constraints, a node may not be able to send the entire sequence all at once. The sequence can be divided into chunks, or frames, of data.

Frame

The frame is the smallest unit of information interchange between two nodes. A frame must meet many stringent constraints. Various fabrics and nodes may impose their own constraints, so some nodes may have to send frames of varying sizes in order to satisfy these constraints. Frames have the following FC frame format:

FIELD NAME	SOF	FRAME HEADER	DATA PAYLOAD	CRC	EOF
# OF BYTES	4	24	0 – 2112	4	4

Figure 1.1 Fibre Channel Frame Format.

The Fibre Channel standard supports a frame payload up to 2112 bytes; however, Tachyon only supports an outbound frame payload up to **2048** bytes. This outbound frame payload includes optional headers.

The following figure shows an exchange example.

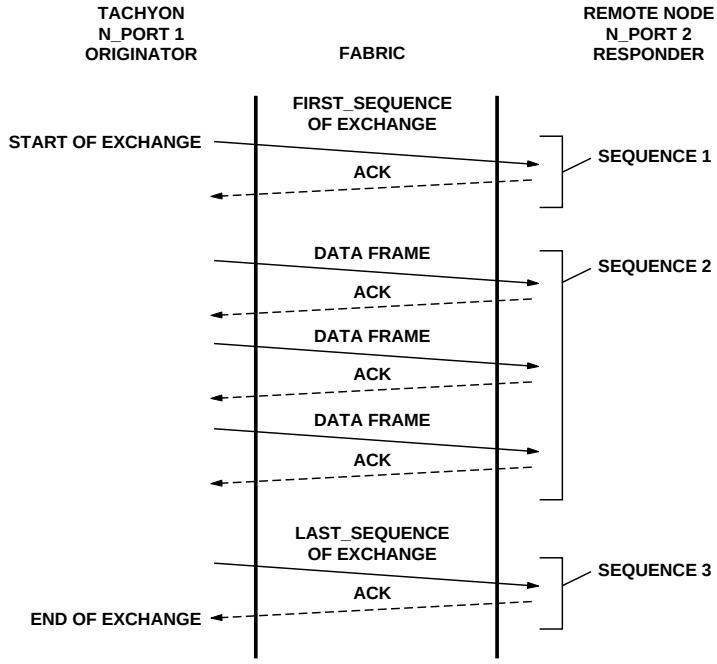


Figure 1.2 Exchange Example.

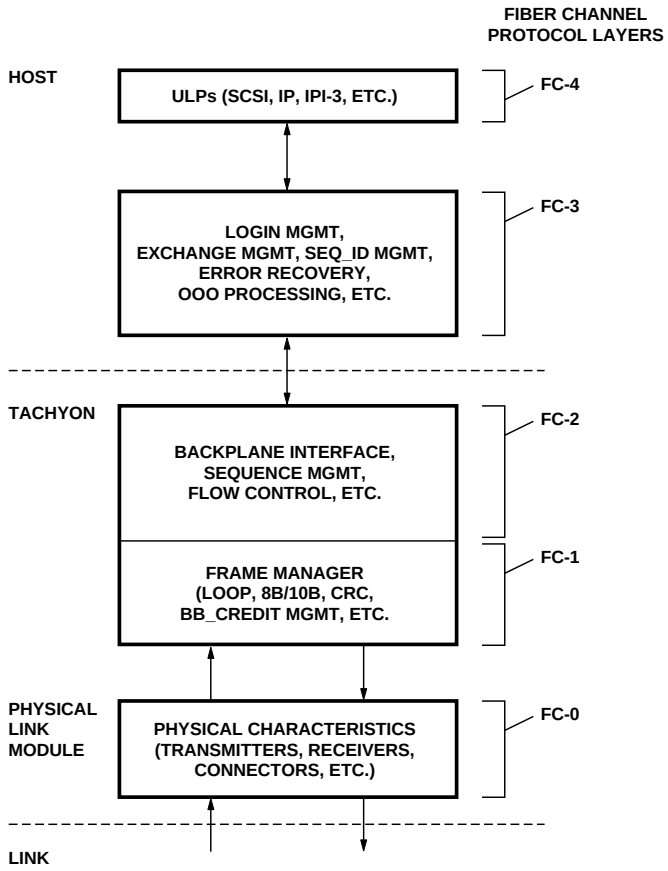


Figure 1.3 Fibre Channel Protocol Block Diagram.

1.2 Networking Encapsulation

Fibre Channel supports any known networking protocol. This is possible because Fibre Channel has defined FC-4, which specifies the mapping of Upper Level Protocols (ULPs) to the lower Fibre Channel levels, FC-3, FC-2, FC-1, and FC-0. Examples of ULPs include SCSI, IP, IPI, etc. The Fibre Channel Physical Interface comprises Fibre Channel protocol levels FC-2, FC-1, and FC-0.

The following figure shows a block diagram of Tachyon with the associated Fibre Channel protocol layers.

Using the Fibre Channel Physical Interface, FC-4 mapping protocols can transfer ULP data. For example, in most networking protocol stacks, the concept of a data packet or datagram exists. The networking data packet or datagram is analogous to the Fibre Channel sequence. To send a sequence, the Originator node segments the sequence into frames. The ULP data packet is written to the data payload field of the Fibre Channel frame(s). Then the SOF, header, CRC, and EOF information is added. The Originator node transmits these encapsulated frames across the Fibre Channel interconnection fabric. The Responder node receives and reassembles the sequence. When the data transmission is complete, the ULP manages the remainder of the data processing.

Mass storage Fibre Channel exchanges map directly to device I/O transactions. However, networking exchanges are not as easily defined and networking exchanges can occur in many

different ways. One way is a “long term” exchange. This is where a node sends data to another node, establishes an exchange between the nodes as a virtual link, and keeps the exchange active. Another way is a “short term” exchange, where a TCP connection is mapped onto an exchange. An exchange is created when an application connects. An exchange is terminated when an application disconnects.

1.3 Mass Storage Encapsulation

Fibre Channel was originally intended as a follow-on technology to lower performance mass storage interconnects. In particular, Fibre Channel focused on improving SCSI and IPI technologies. The Fibre Channel standards groups defined encapsulation methods for both of these protocols. Tachyon supports both SCSI and IPI protocols, and provides special hardware assists for the SCSI protocol. These SCSI hardware assists execute the encapsulation protocol in hardware to provide high performance and low latency I/O transactions. The exchange originator transmits these encapsulated SCSI frames across the Fibre Channel interconnection fabric. The responder receives and reassembles the fibre channel sequence. When the sequence is reassembled, the remainder of the data processing is managed using upper layer SCSI protocol.

1.4 Fibre Channel Protocol for SCSI

This section includes Fibre Channel Protocol for SCSI (FCP) information and how a SCSI I/O transaction maps onto the Fibre Channel transaction hierarchy.

Each SCSI I/O transaction maps on a separate independent Fibre Channel exchange. For FCP, an exchange splits into three distinct phases: the Command Phase, the Data Phase, and the Status Phase. Each phase involves the transmission and/or reception of one or more Fibre Channel sequences. These sequences provide a mechanism of flow control and notification of impending transfers between the initiator and the target device. The Command Phase, Data Phase, and Status Phase are defined below:

Command Phase

The FCP Initiator uses the Command Phase to inform the target device of its intention to perform an I/O transaction. The Command Phase consists of a single frame SCSI Command Sequence (FCP_CMND) that carries information to the target device(s). This information includes the direction of transfer, the length of transfer, and the SCSI address. After the target device processes this SCSI Command Sequence, the transaction enters the Data Phase. If a Data Phase does not exist, the transaction will enter the Status Phase.

Data Phase

The Data Phase consists of a two step process:

1. The target transmits or receives data via the Data Sequence (FCP_DATA). The direction of transfer is identified in the original Command Sequence. This data sequence may consist of one or more frames.
2. The target device sends a Transfer Ready (FCP_XFER_RDY) sequence to inform the initiator that it has the resources ready for a data transfer. The FCP_XFER_RDY sequence is an optional step for an FCP Initiator Read Exchange. When the initiator receives the FCP_XFER_RDY, the process moves on to the second step.

Status Phase

The Status Phase begins when the last FCP_DATA completes. In the Status Phase, the target device sends a single frame SCSI Status Sequence (FCP_RSP) describing how well the transaction proceeded. Once the initiator processes this sequence, the SCSI I/O transaction is complete.

1.5 Profile Support

Tachyon supports the FCSI profiles for FC-IP and FCP. Tachyon does not provide hardware assists for any other profiles, such as IPI-3. By using the generic sequence transmit and receive capabilities of Tachyon, the host can support any known profiles. Agilent Technologies will only test FCSI profiles for FC-IP and FCP.

1.6 Host Bus Adapter Board

A generic Fibre Channel host bus adapter board contains the following components:

1. A Backplane Connector, which connects the backplane interface chip to the host bus

2. A Backplane Interface Chip, which enables connection to PCI, EISA, a propriety bus, etc.

3. Tachyon, the Fibre Channel interface controller chip

4. A Physical Link Module (PLM), for example, a 20-bit Gigabit Link Module (GLM)

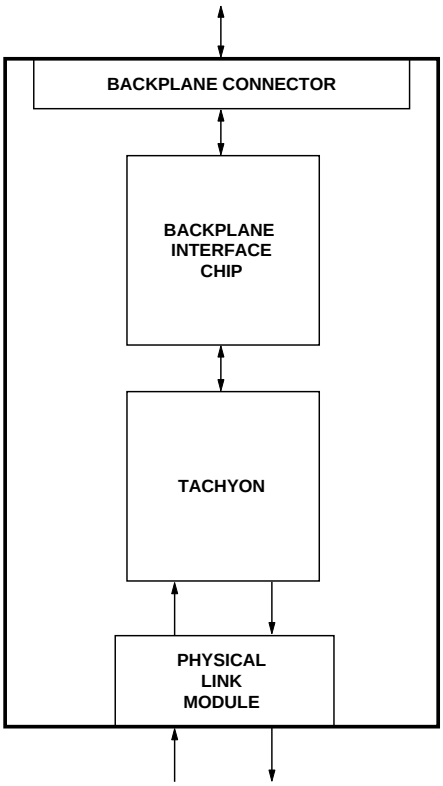


Figure 1.4 Typical Host Bus Adapter Board Block Diagram.

2. Architectural Overview

This section provides an architectural overview of the transmit, receive, and SCSI hardware assists processes of Tachyon.

2.1 Transmit Process Overview

The following figure illustrates the transmit process overview.

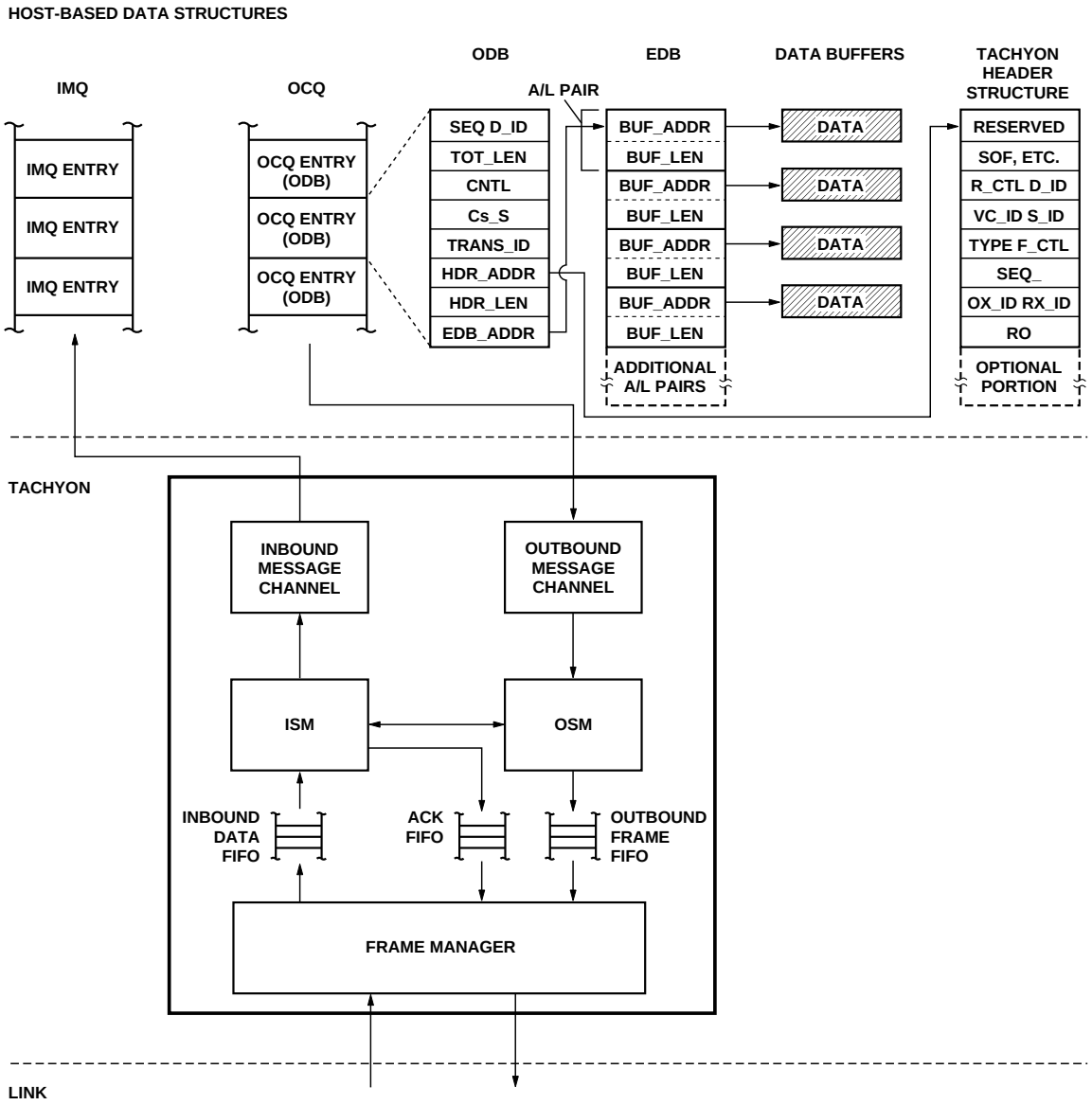


Figure 2.1 Transmit Process Overview.

A normal transmit transaction begins when the host creates buffers of data to be sent. These data buffers are stored in host memory. The host creates a Tachyon Header Structure which contains Fibre Channel header information and resides in host memory. The host creates an Outbound Descriptor Block (ODB) host data structure that defines the sequence of data to be transmitted. The ODB contains Fibre Channel information (e.g., maximum frame size, class of service, exchange identifier, sequence identifier, etc.) that is obtained from the host managed login parameters. The ODB contains a pointer (Hdr_Addr) to the Tachyon Header Structure. Tachyon uses the Fibre Channel information in the ODB and the Tachyon Header Structure to construct the Fibre Channel frame headers. The ODB also contains a pointer (EDB_Addr) to the Extended Descriptor Block (EDB). The EDB contains Address/Length pairs (A/L pairs) that define where the data buffers are located in host memory.

The Outbound Command Queue (OCQ) is an area in host memory consisting of an array of OCQ entries. The producer index of the OCQ, known as the OCQ Producer Index, points to the next available OCQ entry in which an ODB can be created. Once the host creates the ODB, it writes the index of that OCQ entry (ODB) to the OCQ Producer Index register. This notifies Tachyon that a new valid ODB exists. The OCQ Producer Index is incremented to the next available OCQ entry for the following valid ODB.

If Tachyon's Outbound Sequence Manager (OSM) is not currently transmitting a sequence, the OSM performs a DMA operation to move the ODB via the Outbound Message Channel from host memory into an internal Tachyon resource. When the OSM receives the ODB, the OSM has all the information needed to transmit the sequence. It has all of the Fibre Channel information to construct the Fibre Channel frame headers and all of the A/L pairs that point to the data in host memory.

The OSM retrieves data from the Outbound Message Channel in frame size packets for transmission. The OSM DMAs the first frame from the data buffer in host memory to the Outbound Frame FIFO. Once the entire frame is in the Outbound Frame FIFO, the OSM notifies the Frame Manager to begin transmitting the frame onto the link. When the first word of the frame is transmitted onto the link, the OSM is notified. The OSM then begins to move the second frame from host memory to the Outbound Frame FIFO. The first frame is being moved from the Outbound Frame FIFO onto the link during the same time that the second frame is being moved from host memory into the Outbound Frame FIFO. This operation continues until the entire sequence has been transmitted.

For a normal Class 1 (dedicated connection with ACKs) and for a Class 2 (connectionless transaction with ACKs) transmit transaction, the remote node returns ACKs to Tachyon when the remote node receives frames. When Tachyon's Inbound Sequence Manager (ISM) receives a frame, the ISM first determines if it is an ACK frame. If the frame is an ACK frame, the ISM passes the ACK to the OSM. The OSM verifies that the ACK is associated with the current outbound sequence and increments an ACK counter. The OSM maintains a count of the number of frames transmitted for the sequence and the number of ACK frames received. When all frames of the sequence have been transmitted and the number of ACK frames equals the number of transmitted frames, then the sequence has been transmitted successfully to the remote node. For Class 3, when the remote node receives the frames, it does not return ACKs to Tachyon.

When the OSM transmits the sequence successfully, it notifies the ISM to generate an outbound_completion message. The ISM sends this completion message to the host as an entry in the Inbound Message Queue (IMQ). Completion messages contain information on the status of the transfer and any information needed by the host for queue maintenance. In this case, the outbound_completion message notifies the host that the sequence has been transmitted successfully.

2.2 Receive Process Overview

The ISM manages receive processes for four types of sequences: 1) Single Frame Sequences, 2) Multiframe Sequences, In Order, 3) Multiframe Sequences, Out of Order, and 4) Multiframe Sequences, Deferred P_BSY Mode.

The following figure illustrates the SFS and MFS receive Processes:

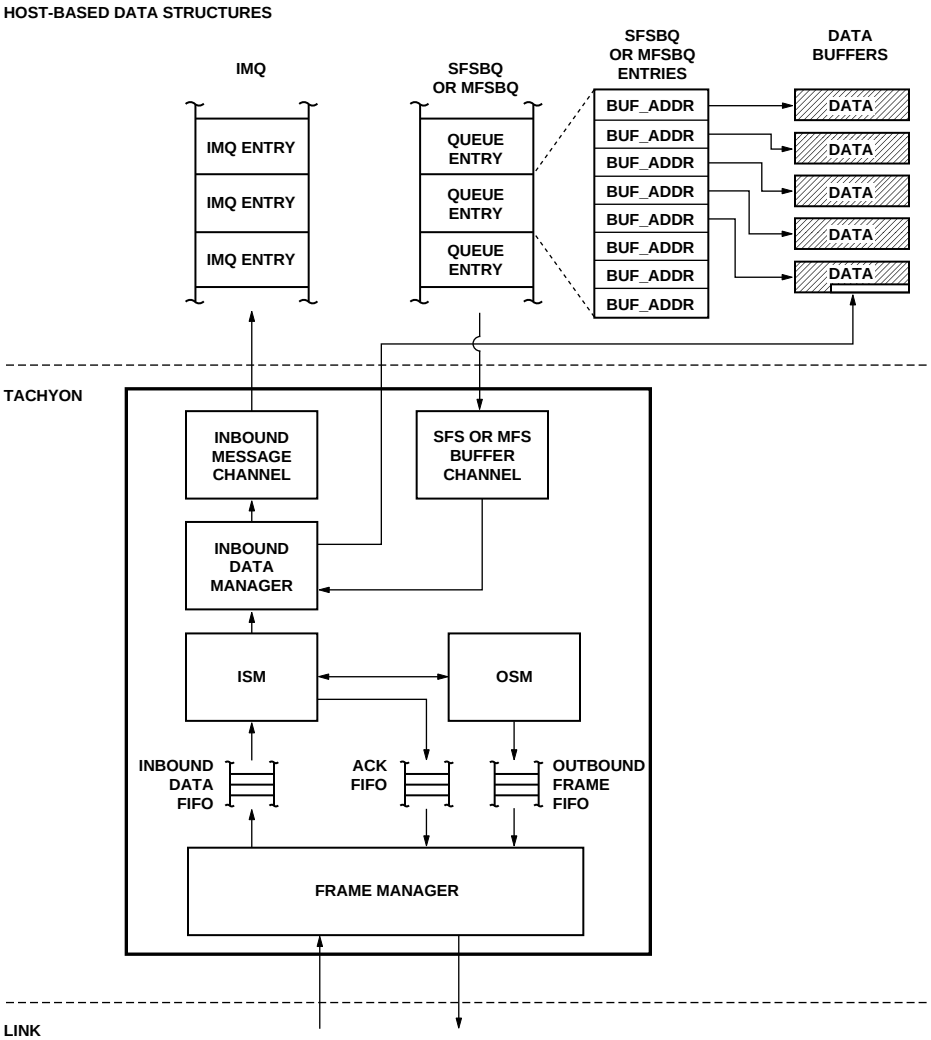


Figure 2.2 Receive Process Overview.

2.2.1 Single Frame Sequence Reception

As Tachyon receives a frame, it stores the frame in the Inbound Data FIFO while it verifies the Cyclic Redundancy Check (CRC). If the CRC fails, Tachyon discards the frame. If the CRC passes, Tachyon notifies the ISM of the received frame.

The ISM checks the frame to determine if it is a single frame sequence (SFS). If it is, Tachyon uses the next available buffer in the Single Frame Sequence Buffer Queue (SFSBQ) and DMAs the SFS (Fibre Channel Header and a data payload) to the host via the Inbound Data Manager and the SFS Buffer Channel. If the entire SFS does not fit into one buffer, Tachyon continues packing the remaining data into the next available buffer until it becomes full. If the buffer becomes full, the ISM provides a new buffer and the process continues until the SFS is totally stored. When the DMA operation completes, the ISM transmits the ACK frame (if the frame is Class 1 or Class 2) that is associated with the SFS.

Next, the ISM generates an inbound_sfs_completion message and passes it through the Inbound Data Manager and Inbound Message Channel as an entry in the IMQ. After Tachyon sends the completion message, Tachyon then generates an interrupt to signal the host to process the received sequence. As its default, Tachyon generates interrupts for inbound sequences. For the host to avoid unnecessary interrupts, interrupt avoidance techniques can be used when any type of completion message is passed as an entry into the IMQ.

2.2.2 Multiframe Sequence, In Order Reception

As Tachyon receives a frame, it is stored in the Inbound Data FIFO while the CRC is verified. If the CRC fails, then the frame is discarded. If the CRC passes, the ISM is notified. The ISM first checks the frame to determine if it is a SFS, which in this case, it is not.

Next, the ISM checks if it is currently reassembling a multiframe sequence (MFS). If the ISM is already reassembling a multiframe sequence, the ISM checks the frame to determine whether the frame belongs to the

current multiframe sequence. If it does not, the ISM generates a busy response (P_BSY) to be sent to the remote node and the frame is discarded. The P_BSY informs the remote node that Tachyon does not have the resources available to reassemble another sequence at this time. If Tachyon is in the Deferred P_BSY mode, Tachyon does not automatically send a P_BSY to the remote node. Refer to "2.2.4 Multiframe Sequence, Deferred P_BSY Mode."

If the ISM receives a frame for a MFS when it is not currently reassembling a MFS, Tachyon DMAs the frame to host memory. The host uses buffers from the Multiframe Sequence Buffer Queue (MFSBQ) to reassemble a MFS. When Tachyon receives the first frame of the MFS, a new buffer is provided from the MFSBQ and the Fibre Channel Header information of the frame is moved into that buffer. Data payload of the frame is packed into the following buffer. As subsequent frames arrive, the ISM checks if each frame is the next expected frame of the sequence. Assuming that Tachyon receives the sequence in order, Tachyon discards the Fibre Channel Header and passes the remaining data payload to the host to be packed into buffers. As each new frame arrives, Tachyon processes it the same way. Tachyon packs the data payload into the current buffer until it becomes full. Once it becomes full, the ISM provides a new buffer and the process continues. As Tachyon receives each frame and moves it into host memory, the ISM sends the ACK frame (if the frame is Class 1 or Class 2) that is associated with the MFS.

When the last frame arrives, various fields in the Fibre Channel Header are saved in internal registers. Tachyon passes the last frame, with the Fibre Channel Header discarded, to the host. The ISM generates an inbound_mfs completion message and passes it as an entry on the IMQ, and updates the IMQ Producer Index. After Tachyon sends the completion message to the host, Tachyon generates an interrupt to signal the host to process the received sequence. As its default, Tachyon generates interrupts for inbound sequences. To avoid unnecessary interrupts, the host can use interrupt avoidance techniques when any type of completion message is passed as an entry into the IMQ.

2.2.3 Multiframe Sequence, Out Of Order (OOO) Reception

The Out of Order Multiframe Reception operates the same as the in order multiframe reception until the first OOO frame arrives. When the ISM determines that the frame is OOO, it generates an inbound_ooo_completion message and passes it as an entry on the IMQ. Then the ISM restarts the reception by copying the entire OOO frame, including the Fibre Channel Header, and sending it to the host using new data buffers. Then the ISM processes the remaining frames in the sequence, assuming that the subsequent frames arrive in order. The ISM does not generate an interrupt until the entire sequence has arrived.

At each point of discontinuity, that is, when a new OOO frame arrives, Tachyon generates an inbound_ooo completion message and uses a new buffer to re-start the reassembly.

2.2.4 Multiframe Sequence, Deferred P_BSY Mode

Tachyon is designed to reassemble one MFS at a time. When Tachyon receives a frame for a new MFS while a current MFS is being reassembled, Tachyon generates a N_Port busy response (P_BSY) for the frame(s) of that new MFS. The remote node that receives the P_BSY can retry the sequence later. Hopefully, when the remote node retries sending the sequence, Tachyon has completed the previous MFS so that it can accept the new MFS.

This process works well when Tachyon communicates with only one other remote node, e.g., a client in a client-server configuration. However, a server in a client-server configuration may be receiving MFS from many clients (remote nodes) at the same time. When Tachyon receives several new MFS frames, other than the current MFS being reassembled, the new frames are P_BSY'd. The remote nodes re-send the frames causing even more interference with the current MFS being reassembled. These excessive retries may cause the remote nodes to stop sending their MFS, which leads to upper layer error recovery overhead. This overhead can be reduced by using the Deferred P_BSY mode.

In Deferred P_BSY mode, the host sets the Disable AUTO P_BSY bit in the Tachyon Configuration register so that Tachyon does not automatically send a P_BSY to the remote node. When Tachyon receives a new MFS in Deferred P_BSY mode, Tachyon sends the new MFS

frame to the host via the SFSBQ. Tachyon generates an inbound_busied_frame completion message. The host stores this frame in a Deferred P_BSY queue.

When Tachyon receives all of the frames for the current MFS it is reassembling, it sets the Deferred ACK bit in the inbound_mfs_completion message and defers the final ACK generation to the host. Tachyon does this so that the host can send a P_BSY to one of the waiting remote nodes. This operation allows one of the waiting remote nodes to retry its MFS before the current remote node can start a new MFS. In Deferred P_BSY mode, Tachyon attempts to process MFSs in a way that all remote nodes have fair access.

2.3 SCSI Hardware Assists Overview

The ability to reassemble only one multiframe sequence may be sufficient for client-based or request reply networking traffic, but is not adequate for I/O traffic. A typical scenario is a host that is connected to many SCSI I/O devices. Because SCSI I/O devices are typically mechanical devices and are relatively slow compared to the host, a host may have hundreds or even thousands of active SCSI I/O transactions. Since it is possible to have many active SCSI I/O transactions, it is necessary to reassemble more than one inbound sequence at a time. By using Tachyon's SCSI hardware assists, the host is capable of concurrently reassembling 16,384 SCSI-assisted sequences.

2.3.1 FCP Read for Tachyon as an Initiator

An FCP Read transaction is considered "inbound" for Tachyon as an initiator. When the initiator host wants to perform a Read transaction, it creates an entry in the host-based SCSI Exchange State Table (SEST). Each used entry in the SEST contains exchange state information for one SCSI I/O transaction. An Inbound SEST Entry contains a pointer to the SCSI Descriptor Block (SDB). The SDB is a list of pointers to empty buffers in host memory. The host pre-allocates these empty buffers to receive all the Read data for the exchange.

The initiator host sends an FCP_CMND for a Read to the target. The FCP_CMND requests the target to send the SCSI read data.

When the target is ready to transmit the SCSI read data to the initiator, it may send an FCP_XFER_RDY, which is an optional step for an FCP Read Exchange. When the initiator Tachyon receives the FCP_XFER_RDY, it discards it. When the initiator Tachyon receives a frame for the Read data sequence from the target, the initiator Tachyon operates in one of two modes, 1) Out of Order Reassembly mode or 2) In Order Reassembly mode. When the initiator host enables OOO Reassembly, then frames for a sequence from the target can arrive in any order. When the host enables In Order Reassembly, then frames must arrive in order.

For each frame received, Tachyon uses the Originator Exchange Identifier (OX_ID) in the Fibre Channel Header as an index into the initiator host SEST. Once Tachyon has identified the appropriate Inbound SEST Entry, the ISM DMAs the SCSI read data to the host buffers. Tachyon continues receiving the data until all of the data is packed into host buffers.

In the final phase of the FCP Read, the initiator Tachyon receives a FCP_RSP from the target. When the ISM receives the FCP_RSP, it passes the FCP_RSP to host memory via the SFSBQ. This FCP_RSP notifies the host that the FCP Read transaction is complete. Then, the ISM generates an inbound_scsi_status completion message and passes this completion message as an entry on the IMQ. The ISM interrupts the host. The interrupt avoidance rules apply here as well.

The following figure illustrates the FCP Read process for Tachyon as an initiator:

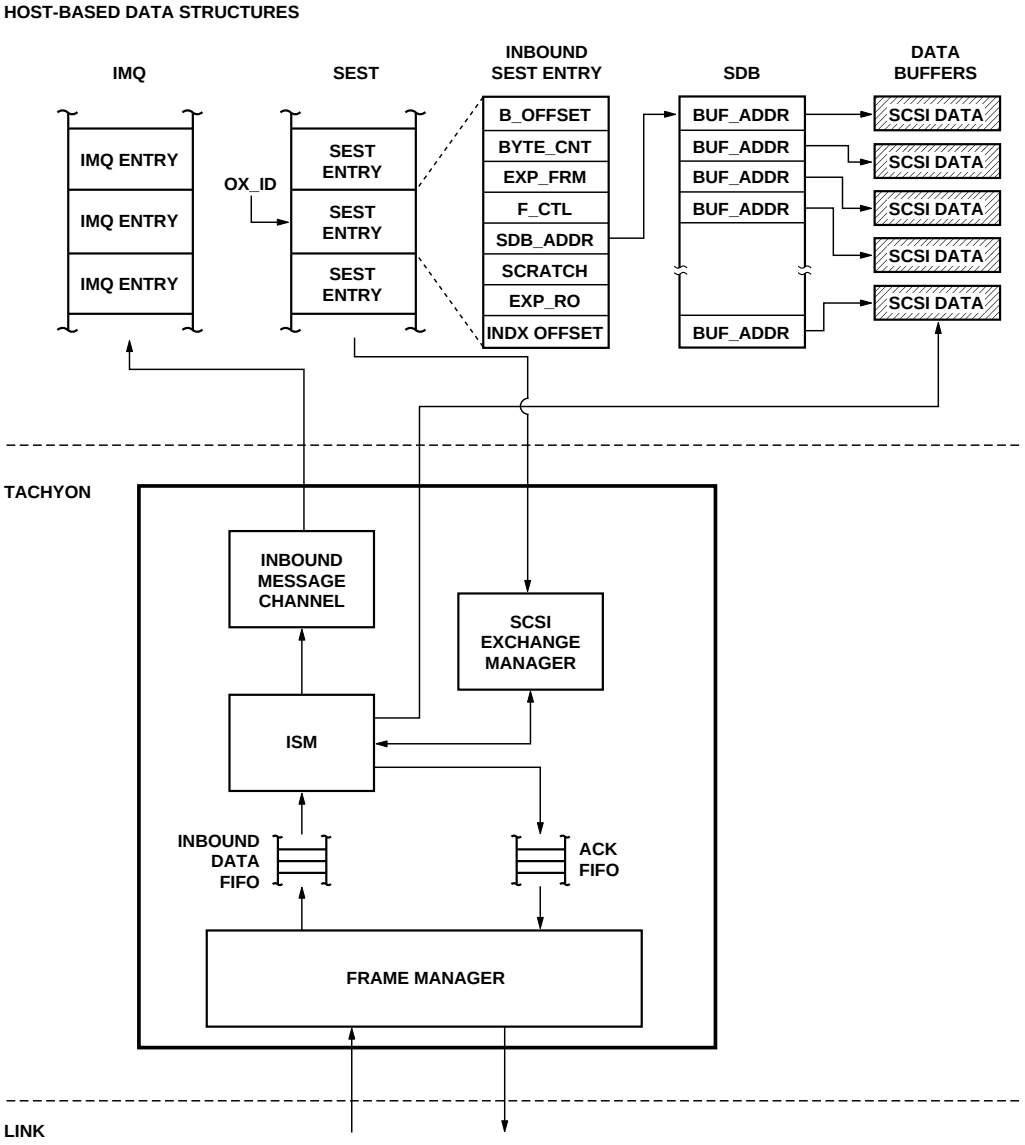


Figure 2.3 FCP Read for Tachyon as an Initiator.

2.3.2 FCP Read for Tachyon as a Target

An FCP Read exchange is considered “outbound” for Tachyon as a target. For FCP Read transactions for the target Tachyon, SCSI hardware assists are not used.

The target Tachyon receives an FCP_CMND for an FCP Read from the initiator and passes it to the target host. The target host builds an EDB that defines where the Read data is located in the target host memory. The target host may program the target Tachyon to send an FCP_XFER_RDY via the OCQ to the initiator indicating that it is ready to send the Read data. The target host then programs the target Tachyon to send the requested SCSI read data via the OCQ to the initiator. When it is finished, the target host programs the target Tachyon to send an FCP_RSP indicating that the FCP Read transaction is complete.

2.3.3 FCP Write for Tachyon as an Initiator

An FCP Write transaction is considered “outbound” for Tachyon as an initiator. When the initiator host wants to perform a Write transaction, it creates an Outbound SEST Entry. The Outbound SEST Entry contains a pointer to an EDB that points to the SCSI write data.

The initiator host sends an FCP_CMND for a Write to the target. When the initiator Tachyon receives an FCP_XFER_RDY from the target, it checks the value of the DATA_RO field. If the DATA_RO is zero, the initiator Tachyon manages the Write transaction. If the DATA_RO field is non-zero, Tachyon passes this FCP_XFER_RDY to the host. In this case, the initiator host is responsible for managing the data transfer.

When the initiator Tachyon sends all the Write data, it waits to receive an FCP_RSP from the target. Initiator Tachyon passes the FCP_RSP and an inbound_scsi_status_completion message to the initiator host. This informs the host that the exchange completed.

2.3.4 FCP Write for Tachyon as a Target

An FCP Write exchange is considered “inbound” for Tachyon as a target. The target Tachyon receives an FCP_CMND for an FCP Write from the initiator. The target host must create an SDB that points to an empty buffer that receives the Write data from the initiator. When the target host has allocated enough buffers and is ready to receive the data, it sends an FCP_XFER_RDY with the DATA_RO field equal to zero to the initiator. If the target host is not ready to manage the entire requested Write transaction, it sends multiple FCP_XFER_RDYs to complete the transaction.

When the target Tachyon receives the SCSI write data, it operates in one of two modes, 1) Out of Order Reassembly mode or 2) In Order Reassembly mode. When the target Tachyon receives all of the data, the target Tachyon sends an inbound_scsi_data completion message to the IMQ of the target host. The target Tachyon then sends an FCP_RSP to the initiator indicating that the exchange has completed.

3. Architectural Details

3.1 Tachyon Internal Block Diagram

The Tachyon Internal Block Diagram shows the high level chip architecture.

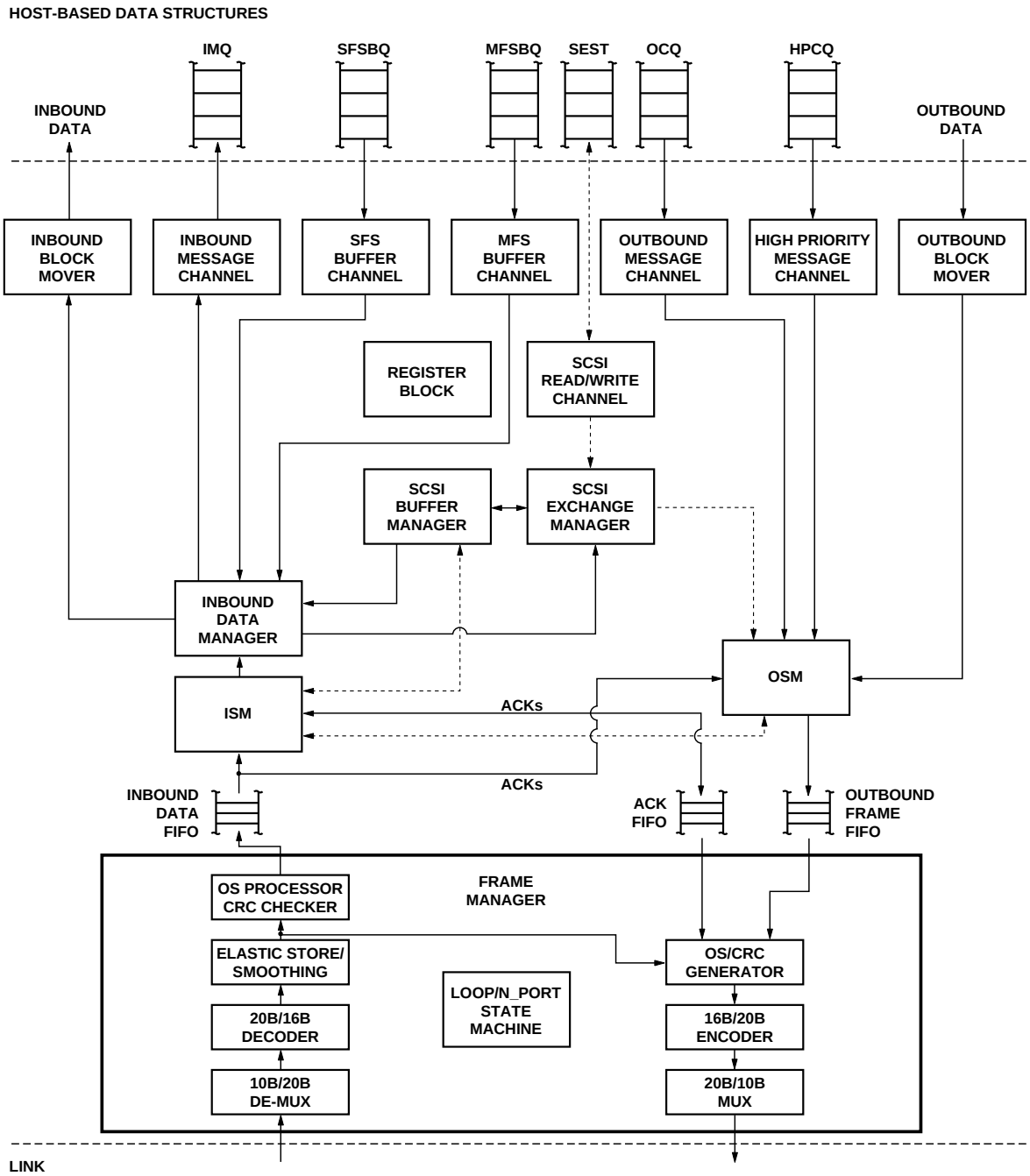


Figure 3.1 Tachyon Internal Block Diagram.

4. Tachyon Signal Descriptions
4.1 Tachyon Logic Symbol

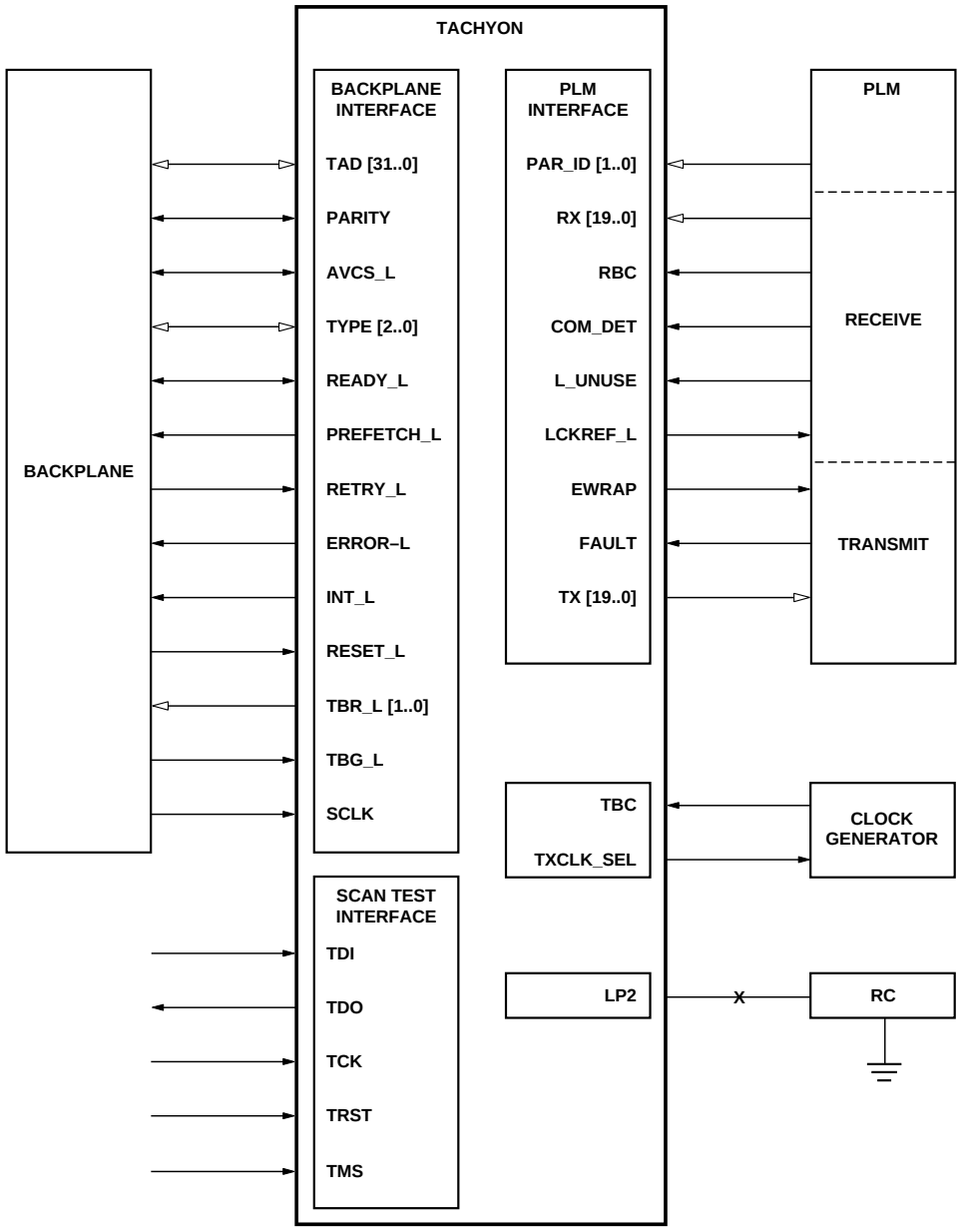


Figure 4.1 Tachyon Logic Symbol.

4.2 Tachyon Pin-out

Pin	Pad Label	Pin	Pad Label	Pin	Pad Label	Pin	Pad Label
1	Vdd2 (a)	53	Vdd	105	Vdd2 (a)	157	Vdd
2	Vss2 (e)	54	Vss2 (e)	106	TAD[26]	158	Vss
3	RX[8]	55	IDD_TEST (c)	107	TAD[27]	159	TX[17]
4	RX[9]	56	LP2	108	TAD[28]	160	TX[[19]
5	RX[19]	57	PLLAGND	109	Vdd	161	L_UNUSE
6	Vdd	58	PLLVdd	110	Vss	162	TXCL_SEL
7	Vss	59	PLLVss	111	TAD[29]	163	Vdd2 (a)
8	RX[17]	60	TAD[0]	112	TAD[30]	164	Vss
9	RX[15]	61	TAD[1]	113	TAD[31]	165	TBC
10	RX[13]	62	TAD[2]	114	VDD2 (a)	166	Vdd2 (a)
11	Vdd2 (a)	63	Vdd	115	Vss2 (e)	167	Vss2 (e)
12	Vss2 (e)	64	Vss	116	TYPE[0]	168	TX[1]
13	RX[11]	65	TAD[3]	117	TYPE[1]	169	TX[3]
14	RX[10]	66	TAD[4]	118	TYPE[2]	170	TX[5]
15	EWRAP	67	TAD[5]	119	PARITY	171	Vss
16	Vdd2 (a)	68	Vdd2 (a)	120	Vdd	172	Vss
17	Vss2 (e)	69	Vss2 (e)	121	Vss	173	TX[7]
18	RX[18]	70	TAD[6]	122	TCK	174	TX[0]
19	RX[16]	71	TAD[7]	123	Vss2 (e)	175	TX[2]
20	RX[14]	72	Vdd	124	TMS	176	Vss
21	Vdd	73	Vss	125	RSTN	177	Vss
22	Vss	74	TAD[8]	126	TDI	178	TX[4]
23	RX[12]	75	TAD[9]	127	Vss2 (e)	179	TX[6]
24	PAR_ID[1]	76	TAD[10]	128	TDO	180	TX[8]
25	Vdd	77	Vss	129	Vss2 (e)	181	Vdd
26	Vss2 (e)	78	Vss	130	Vss2 (e)	182	Vss
27	Vss	79	Vdd	131	Vdd2 (a)	183	Vss
28	PREFETCH_L	80	TAD[11]	132	reserved (d)	184	TX[9]
29	TBG_L	81	TAD[12]	133	reserved (d)	185	PAR_ID[0]
30	TBR_L[1]	82	TAD[13]	134	reserved (d)	186	Vss
31	TBR_L[0]	83	TAD[14]	135	Vdd	187	Vss
32	Vdd2 (a)	84	Vdd2 (a)	136	SCAN_EN (d)	188	RBC
33	Vss2 (e)	85	Vss2 (e)	137	reserved (b)	189	Vdd
34	RESET_L	86	TAD[15]	138	reserved (b)	190	Vss
35	INT_L	87	TAD[16]	139	reserved (b)	191	RX[1]
36	ERROR_L	88	Vdd	140	TEST_MODE	193	RX[3]
37	Vdd2 (a)	89	Vss	141	reserved (d)	193	RX[5]
38	Vss2 (e)	90	TAD[17]	142	Vdd2 (a)	194	Vdd2 (a)
39	RETRY_L	91	TAD[18]	143	Vss2 (e)	195	Vss2 (e)
40	READY_L	92	TAD[19]	144	TX[12]	196	RX[7]
41	AVCS_L	93	Vdd2 (a)	145	TX[14]	197	LCKREF_L
42	Vdd	94	Vss2 (e)	146	TX[16]	198	FAULT
43	Vss	95	TAD[20]	147	Vdd2 (a)	199	Vdd2 (a)
44	PLL_RSTN	96	TAD[21]	148	Vss2 (e)	200	Vss2 (e)
45	reserved (c)	97	TAD[22]	149	TX[18]	201	COM_DET
46	PLL_IDD_TEST (b)	98	Vdd	150	TX[10]	202	RX[0]
47	PLL_TEST_DATA (b)	99	Vss	151	TX[11]	203	RX[2]
48	PLL_TEST_MODE (c)	100	TAD[23]	152	Vdd	204	Vdd2 (a)
49	Vdd	101	TAD[24]	153	Vss	205	Vss
50	Vss	102	TAD[25]	154	TX[13]	206	RX[4]
51	SCLK	103	Vss2 (e)	155	TX[15]	207	RX[6]
52	Vdd2 (a)	104	Vdd2 (a)	156	Vdd2 (a)	208	Vdd

Table 4.1 Tachyon Pinout.

Tachyon Pinout Notes

(a) For most applications, Vdd and Vdd2 internal power straps may be connected on the printed circuit board (PCB). Refer to “A.3 PCB Layout Suggestions”.

(b) Pin has internal pull-up and may be left unconnected (solder pad only) or pulled up to Vdd (3.6 V) with a 4.7 kΩ resistor.

WARNING Do not pull up reserved pins to a voltage greater than Vdd (3.6 V)

(c) Pin has internal pull-down and may be left unconnected (solder pad only) or connected to Vss.

(d) Pin must be left unconnected.

(e) For most applications, Vss and Vss2 may be connected on the PCB. Refer to “A.3 PCB Layout Suggestions”.

4.3 Physical Link Module (PLM) Interface

Pin #	I/O	Pad Label	Pad Name	Description
Various	O	TX[19..0]	Transmit Data	10-bit or 20-bit transmit data bus to the PLM. For 10-bit PLMs, only the TX[9..0] outputs are used. The PAR_ID bit determines whether a 10-bit or 20-bit PLM should be used.
165	I	TBC	Transmit Byte Clock	53.125 MHz or 26.5625 MHz clock (± 0.01% average tolerance) supplied by the oscillator. Note that for the TBC: 1) at 26 MHz, a maximum 40/60 duty cycle is allowed; 2) at 53 MHz, only a maximum 45/55 duty cycle is allowed.
Various	I	RX[19..0]	Receive Data	10-bit or 20-bit receive data bus from the PLM. For 10-bit PLMs, only the RX[9..0] outputs are used. The PAR_ID bit determines whether a 10-bit or 20-bit PLM should be used.
188	I	RBC	Receive Byte Clock	The receive byte clock signal is derived from the incoming data stream. The clock frequency is 53.125 MHz for 1063 Mbaud and 10-bit 531 Mbaud PLMs, and 26.5625 MHz for 10-bit 266 Mbaud PLMs (± 0.01%). 20-bit 531 Mbaud PLMs are not supported. Note that for RBC: 1) at 26 MHz, a maximum 40/60 duty cycle is allowed; 2) at 53 MHz, only a maximum 45/55 duty cycle is allowed.
15	O	EWRAP	Electrical Wrap Enable	When asserted high by a host Write to the Frame Manager Configuration register, this signal tells the PLM to loopback the serialized transmit data to the receive deserializer. This signal is also used as a reset to internal logic on the PLM in response to a laser fault signal to perform recovery. An external loopback hood is not required for EWRAP.

Table 4.2 Physical Link Module (PLM) Interface.

4.3 Physical Link Module (PLM) Interface (Continued)

<table>
<tr><th>Pin #</th><th>I/O</th><th>Pad Label</th><th>Pad Name</th><th>Description</th></tr>
<tr><td>197</td><td>O</td><td>LCKREF_L</td><td>Lock to Reference</td><td>When asserted low, this signal provides the mechanism for directing the receive clock generation circuits to obtain frequency lock on a multiple of the Transmit Byte Clock (TBC). Also, when asserted low, this signal causes the PLM to lock its PLL to the TBC.</td></tr>
<tr><td>201</td><td>I</td><td>COM_DET</td><td>Comma Detect</td><td>When asserted high by the PLM, this signal indicates when a K28.5 control character containing a comma of positive disparity (Refer to the “FC-PH”) is detected on the link data stream at the same time as the data is presented on the Receive Data Lines.</td></tr>
<tr><td>161</td><td>I</td><td>L_UNUSE</td><td>Link Unusable</td><td>When asserted high, this signal indicates that the link is unusable for data transfer, that is, light is no longer being received.</td></tr>
<tr><td>198</td><td>I</td><td>FAULT</td><td>Fault</td><td>When asserted high, this signal indicates that a fault has been detected on the module, for example, an improper power level has occurred on the laser.</td></tr>
<tr><td>162</td><td>O</td><td>TXCLK_SEL</td><td>Transmit Clock Select</td><td>Indicates which clock frequency the external clock multiplexing hardware should supply. This signal is derived from the PAR_ID lines.
<table>
<tr><th>TXCLK_SEL</th><th>Clock Frequency</th></tr>
<tr><td>0</td><td>53.1250 MHz</td></tr>
<tr><td>1</td><td>26.5625 MHz</td></tr>
</table></td></tr>
<tr><td>24
185</td><td>I</td><td>PAR_ID[1]
PAR_ID[0]</td><td>Parallel ID</td><td>These two bits are asserted by the PLM to indicate the link rate and assumed interface width of the PLM. They are interpreted by Tachyon as follows.
<table>
<tr><th>PAR_ID[1..0]</th><th>Link Rate</th><th>Data Width</th></tr>
<tr><td>01</td><td>265.625 MHz</td><td>10 bits</td></tr>
<tr><td>10</td><td>531.25 MHz</td><td>10 bits</td></tr>
<tr><td>11</td><td>1062.5 MHz</td><td>20 bits</td></tr>
</table></td></tr>
</table>

Table 4.2 Physical Link Module (PLM) Interface.

Note:
Tachyon supports GLMs that conform to the FCSI-301-Revision 1.0 GLM family.

4.4 PLL External Connections

Tachyon contains a PLL which is used for internal functionality. This section describes how the external pins of this PLL should be connected.

Pin #	I/O	Pad Label	Pad Name	Description
44	I	PLL_RSTN	PLL Reset	When asserted low, this signal is the reset signal for the PLL. During normal operation this pin should be left unconnected. This pin has an internal pull-up.
46	I	PLL_IDD_TEST	PLL Quiescent Current (IDDQ) Test Enable	This pin has an internal pull-up. Refer to "LSI's LCB500K Design Manual, 1994, sections 3.24 and 3.6.3 (IDD Test)" for usage.
47	I	PLL_TEST_DATA	PLL Test Data Input	This pin controls the system clock when PLL_TEST_MODE is asserted high. This pin has an internal pull-up.
48	I	PLL_TEST_MODE	PLL Test Mode Select	When asserted high, the PLL's VCO output is bypassed, and PLL_TEST_DATA drives the system clock. This pin has an internal pulldown.
56	I	LP2	PLL External RC Network	This pin is used for external RC circuitry of the PLL. This pin should be connected to a 200Ω 5% resistor, 1nF 5% capacitor, and the PLLAGND pin in series. Refer to "7.6 External PLL Components" on page 99.
57	I	PLLAGND	PLL Analog Ground	This pin is used for external RC circuitry of the PLL. This pin should be connected to a 1nF 5% capacitor, 200 Ω 5% resistor, and the LP2 pin in series. Refer to "7.6 External PLL Components" on page 99.
58	I	PLLVdd	PLL Vdd	This pin should be connected to a Vdd source via ferrite bead with capacitor to Vss. For additional details and alternative methods of connecting this pin, refer to "A.3 PCB Layout Suggestions" on page 106.
59	I	PLLVss	PLL Vss	This pin should be connected to a Vss source. Refer to "A.3 PCB Layout Suggestions" on page 106.

Table 4.3 PLL External Connections.

4.5 JTAG 1149.1 Scan Test Interface

Pin #	I/O	Pad Label	Pad Name	Description
55	I	IDD_TEST	Boundary Scan (JTAG) Cells' IDDQ Test Enable	This pin has an internal pulldown. Refer to LSI or "LSI's LCB500K Design Manual, 1994, p. 13-82" for details.
122	I	TCK	Test Clock	Transitions the Test Access Port (TAP) state machine to the next state on the rising edge of this signal. If not used, leave unconnected or pull up with a 4.7 kΩ resistor to Vdd.
124	I	TMS	Test Mode Select	This signal determines the next state of the TAP state machine. If not used, leave unconnected or pull up with a 4.7 kΩ resistor to Vdd.
125	I	RSTN	TAP Reset	When asserted low, the TAP controller and RAM BIST are reset. If not used, leave unconnected or pull up with a 4.7 kΩ resistor to Vdd.
126	I	TDI	Test Data In	Used to scan data serially into the boundary register cells. If not used, leave unconnected or pull up with a 4.7 Ω resistor to Vdd.
128	O	TDO	Test Data Out	Used to scan data serially from the boundary register cells. If not used, leave unconnected or pull up with a 4.7 kΩ resistor to Vdd.
136	I	SCAN_EN	Internal Scan Chain Enable	This pin has an internal pulldown. Assert this pin high when performing internal scan chain tests.
140	I	TEST_MODE	Test Enable	When asserted high, this control signal tri-states all pins on the Tachyon package, with the exception of "reserved" pins 132, 133, 134, and 141. If not used, connect Vss through a 4.7 kΩ resistor.

Table 4.4 JTAG Scan Test Interface.

4.5.1 JTAG Instructions

Instruction	Instruction Type	Encoding
Bypass	Mandatory	11111
Extest	Mandatory	00000
Sample	Mandatory	00001
Clamp	Optional	00110
High-z	Optional	00111

Table 4.5 JTAG Instructions.

For information on the use of JTAG Boundary Scan, refer to the "IEEE 1149.1 Boundary Scan specification".

4.6 Tachyon System Interface (TSI)

This section describes the Tachyon System Interface for the Tachyon Fibre Channel chip. Included in this discussion is a description of the signals as well as a description of the protocol used across this interface.

4.6.1 TSI Signal List

Pin #	I/O	Pad Label	Pad Name	Description
Various	I/O	TAD[31..0]	Multiplexed Address/ Data	Address is driven by the transaction master during the address phase. The master drives only word addresses, so only bits TAD[31..2] contain useful information; however, parity must be generated for TAD[31..0]. During the data cycles(s), data is driven by the device being read or by the device mastering a write.
119	I/O	PARITY	Parity Information	This bi-directional signal carries parity information for address and data on the TSI. Parity is optional, and is defined by the Parity Even (bit 1) and Parity Enable (bit 2) bits in the Tachyon Configuration register.
41	I/O	AVCS_L	Address Valid Chip Select	This signal is driven by the master of a transaction during the address phase.
118 117 116	I/O	TYPE[2] TYPE[1] TYPE[0]	Transaction Types	Asserted low by the master of a transaction. TYPE indicates the size and direction of the transaction. Refer to “6.1.1 TSI Transaction Types” on page 60.
40	I/O	READY_L	Device Ready	Asserted by a transaction responder when a transaction is complete. Refer to “6.1.7 Driving Bi-Directional Signals” on page 62. More information about READY_L is available in “4.6 Tachyon System Interface (TSI)” and “6.2 TSI Functional Waveforms”.
39	I	RETRY_L	Read Retry	Asserted by the host to terminate a read request if the read data cannot be available to Tachyon.
28	O	PREFETCH_L	Prefetch Request	Asserted low by Tachyon to signal that the next sequential data will be read. This signal may be active during retry. Refer to “6.1.9 Read Transactions” on page 62.
36	O	ERROR_L	Error Out	Asserted low by Tachyon to indicate a bus parparity error, protocol error, or internal parity error.
35	O	INT_L	Interrupt	Asserted low by Tachyon to signal that a message has been posted to the host.
34	I	RESET_L	Synchronous Reset	Asserted low by the host to perform a hard reset of Tachyon. RESET_L must be held low for a minimum of 10 clock periods. All configuration information is lost on reset.

Table 4.6 TSI Signal List.

4.6.1 TSI Signal List (Continued)

Pin #	I/O	Pad Label	Pad Name	Description
30 31	O	TBR_L[1] TBR_L[0]	Bus Requests	One bus request signal is asserted when Tachyon needs to master a transaction. TBR_L[1] indicates a read using the pre-fetched channel. TBR_L[0] is used for writes and non-prefetched reads. If only one bus request signal is desired, these two active low signals should be ANDed together, external to the chip. Refer to “6.1.16 Arbitration” on page 66.
29	I	TBG_L	Bus Grant	Asserted low by the host to signal acceptance of Bus Request.
51	I	SCLK	System Clock	24-40 MHz system clock used to drive the backplane side of Tachyon.

Table 4.6 TSI Signal List.

5. Registers

5.1 Register Overview

Register Name	Read/ Write	Address	Reset Value
OCQ Base register	W	0x0000	0x00000000
OCQ Length register	W	0x0004	0x00000000
OCQ Producer Index register	W	0x0008	0x00000000
OCQ Consumer Index Address register (3)	W	0x000C	0x00000000
Host's Copy of Tachyon's OCQ Consumer Index	R	host memory	
HPCQ Base register	W	0x0040	0x00000000
HPCQ Length register	W	0x0044	0x00000000
HPCQ Producer Index register	W	0x0048	0x00000000
HPCQ Consumer Index Address register (3)	W	0x004C	0x00000000
Host's Copy of Tachyon's HPCQ Consumer Index	R	host memory	
IMQ Base register	W	0x0080	0x00000000
IMQ Length register	W	0x0084	0x00000000
IMQ Consumer Index register	W	0x0088	0x00000000
IMQ Producer Index Address register (3)	W	0x008C	0x00000000
Host's Copy of Tachyon's IMQ Producer Index	R	host memory	
MFSBQ Base register	W	0x00C0	0x00000000
MFSBQ Length register	W	0x00C4	0x00000000
MFSBQ Producer Index register	W	0x00C8	0x00000000
MFSBQ Consumer Index register	R	0x00CC	0x00000000
MFS Buffer Length register	W	0x00D0	0x00000000
SFSBQ Base register	W	0x0100	0x00000000
SFSBQ Length register	W	0x0104	0x00000000
SFSBQ Producer Index register	W	0x0108	0x00000000
SFSBQ Consumer Index register	R	0x010C	0x00000000
SFS Buffer Length register	W	0x0110	0x00000000
SEST Base register	W	0x0140	0x00000000
SEST Length register	W	0x0144	0x00000000
SCSI Buffer Length register	W	0x0148	0x00000000
Tachyon Configuration register	R/W	0x0184	0x00000002
Tachyon Control register	W	0x0188	0x00000000
Tachyon Status register	R	0x018C	HW dependent
Tachyon Flush SEST Cache Entry register	R/W	0x0190	0x00000000
Tachyon EE_Credit Zero Timer register	R	0x0194	0x00000000 (2)
Tachyon BB_Credit Zero Timer register	R	0x0198	0x00000000 (2)
Tachyon Receive Frame Error Counter register	R	0x019C	0x00000000
Frame Manager Configuration register	R/W	0x01C0	0x00000000
Frame Manager Control register	W	0x01C4	0x00000000
Frame Manager Status register	R	0x01C8	0x00000000
Frame Manager RT_TOV/AL_TIME & ED_TOV register	W	0x01CC	0x001001F5

Table 5.1 Tachyon Memory Map.

5.1 Register Overview (Continued)

Register Name	Read/ Write	Address	Reset Value
Frame Manager Link Error Counters #1 register	R	0x01D0	0x00000000
Frame Manager Link Error Counters #2 register	R	0x01D4	0x00000000
Frame Manager World Wide Name Hi register	R/W	0x01E0	0x00000000
Frame Manager World Wide Name Lo register	R/W	0x01E4	0x00000000
Frame Manager Received AL_PA register	R	0x01E8	0x00000000
Frame Manager Primitive register	W	0x01EC	0x00000000

Table 5.1 Tachyon Memory Map. (Continued)

Tachyon Memory Map Notes

1. At reset, Tachyon clears all registers to zero, unless otherwise noted. Reset is defined as power-on, a hardware reset, or a software reset.

2. While Tachyon clears registers to zero at reset, certain registers (such as EE_Credit Zero Timer and BB_Credit Zero Timer registers) begin counting up immediately following a reset. As a result, if the host reads a register immediately after a reset, the value may be non-zero.

3. If the host reads an invalid or Write only (W) register, the transaction completes normally, and Tachyon returns 0x00000000.

4. Tachyon ignores bits 31..9 of the address during register accesses.

5. If the host writes to Read only (R) registers, the transaction completes but Tachyon does not write the data to the register.

6. Some Tachyon registers contain bits that indicate a certain parameter is either active or inactive. For most cases, 1=active and 0=inactive, but there are exceptions. Refer to the detailed description of each register bit for specifics.

5.2 Length Register Values

The following table summarizes the programmed values for length registers.

Length Register Name	Length (n)	Programmed Length Field Value (n-1)	Minimum Programmed Value	Maximum Programmed Value
OCQ Length register	The Number of OCQ Queue Entries (Must be a power of 2)	n-1	1	255
HPCQ Length register	The Number of HPCQ Queue Entries (Must be a power of 2)	n-1	1	255
IMQ Length register	The Number of IMQ Queue Entries (Must be a power of 2)	n-1	3	255
MFSBQ Length register	The Number of MFSBQ Queue Entries (Must be a power of 2)	n-1	1	255
MFS Buffer Length register	The Number of Bytes of the MFS Receive Buffers (Must be a power of 2)	n-1	511	65,535
SFSBQ Length register	The Number of SFSBQ Queue Entries (Must be a power of 2)	n-1	1	255
SFS Buffer Length register	The Number of Bytes of the SFS Receive Buffers (Must be a power of 2)	n-1	511	4095
SEST Length register	The Number of SEST Entries (Must be a power of 2)	n-1	0	16,383
SCSI Buffer Length register-OOO Reassembly	The Number of Bytes of the SCSI Receive Buffers (Must be a power of 2)	n-1	511	65,535
SCSI Buffer Length register-In Order Reassembly	The Number of Bytes of the SCSI Receive Buffers (Must be a multiple of 4 bytes)	n-1	3	65,535

Table 5.2 Length Registers Information.

5.3 OCQ Registers

5.3.1 OCQ Base Register

Register Address: 0x0000
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..0	Base Address	Base Address	The physcial address in host memory of the start of the OCQ.

Table 5.3 OCQ Base Register.

OCQ Base Register Notes

1. The OCQ must be aligned on a sizeof (queue) boundary. For example, if the sizeof (OCQ) equals 512 bytes, then bits 8..0 are cleared to zero. The minimum size of the OCQ is 64 bytes (bits 5..0 are cleared to zero).
2. When the host writes the OCQ Base register, Tachyon clears the corresponding consumer index to zero. Therefore, the host must not write to the OCQ Base register after initialization.

5.3.2 OCQ Length Register

Register Address: 0x0004
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Length	Queue Length	The number (zero-based) of OCQ entries.

Table 5.4 OCQ Length Register.

OCQ Length Register Notes

1. The Queue Length field must be a power of 2. The minimum queue length is 2 entries, corresponding to a programmed value of 1. The maximum queue length is 256 entries, corresponding to a programmed value of 255.
2. When the host writes to the OCQ Length register, Tachyon clears the corresponding consumer index to zero. Therefore, the host must not write to the OCQ Length register after initialization.

5.3.3 OCQ Producer Index Register

Register Address: 0x0008
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Length	Queue Index	The producer index value of the next empty OCQ entry.

Table 5.5 OCQ Producer Index Register.

OCQ Producer Index Register Note

1. The host uses the OCQ Producer Index register to inform Tachyon that there are new commands to process in the OCQ. After the host uses an OCQ entry, the host writes the index of the next empty OCQ entry to the OCQ Producer Index register. When the host written producer index is different than the internally maintained consumer index, Tachyon processes the new commands.

5.3.4 OCQ Consumer Index Address Register

Register Address: 0x000C
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..0	Host Index Address	Host Index Address	The address of the host's copy of the OCQ consumer index.

Table 5.6 OCQ Consumer Index Address Register.

OCQ Consumer Index Address Register Notes

1. The OCQ Consumer Index Address register contains the host memory address where Tachyon maintains its consumer index.
2. This index resides in host memory to allow the host fast access to the consumer index.
3. The host index address must be aligned on a 32-byte boundary (bits 4..0 are cleared to zero).

5.3.5 Host's Copy of the OCQ Consumer Index Register

Register Address: Determined by the host
Reset Value: Determined by the host

Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Value is undefined.
7..0	Queue Index	Queue Index	The consumer index value of the OCQ.

Table 5.7 Host's Copy of the OCQ Consumer Index Register.

Host's Copy of the OCQ Consumer Index Register Notes

1. This memory location described by the OCQ Consumer Index Address register contains the host's copy of Tachyon's OCQ consumer index.
2. Tachyon updates this index when it reads an OCQ entry.

5.4 HPCQ Registers

5.4.1 HPCQ Base Register

Register Address: 0x00040
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..0	Base Address	Base Address	The physical address in host memory of the start of the HPCQ.

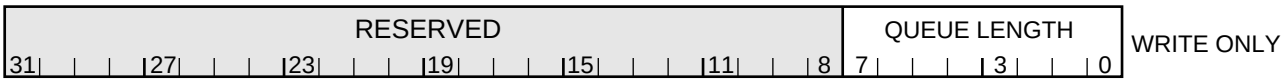
Table 5.8 HPCQ Base Register.

HPCQ Base Register Notes

1. The HPCQ must be aligned on a sizeof(queue) boundary. The minimum size of the HPCQ is 64 bytes (bits 5..0 are cleared to zero).
2. When the host writes to the HPCQ Base register, Tachyon clears the corresponding consumer index to zero; therefore, the host must not write to this register after initialization.

5.4.2 HPCQ Length Register

Register Address: 0x0044
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Length	Queue Length	The number (zero-based) of HPCQ entries.

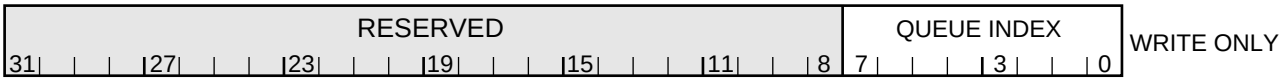
Table 5.9 HPCQ Length Register.

HPCQ Length Register Notes

1. The Queue Length field must be a power of 2. The minimum queue length is 2 entries, corresponding to a programmed value of 1. The maximum queue length is 256 entries, corresponding to a programmed value of 255.
2. When the host writes to the HPCQ Length register, Tachyon clears the corresponding consumer index to zero; therefore, the host must not write to this register after initialization.

5.4.3 HPCQ Producer Index Register

Register Address: 0x0048
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Index	Queue Index	The producer index value of the next empty HPCQ entry.

Table 5.10 HPCQ Producer Index Register.

HPCQ Producer Index Register Note

1. The host uses the HPCQ Producer Index register to indicate to Tachyon that there are new commands to process in the circular queue. After the host uses an HPCQ entry, it writes the index of the next empty entry in the queue to this register. When Tachyon notices that the host written producer index is different from the internally maintained consumer index, Tachyon processes the new commands.

5.4.4 HPCQ Consumer Index Address Register

Register Address: 0x004C
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..0	Host Index Address	Host Index Address	The address of the host's copy of the HPCQ consumer index.

Table 5.11 HPCQ Consumer Index Address Register.

HPCQ Consumer Index Address Register Notes

1. The HPCQ Consumer Index Address register contains the host memory address where Tachyon maintains its consumer index.
2. This index resides in host memory to allow the host fast access to the consumer index.
3. The host index address must be aligned on a 32-byte boundary (bits 4..0 are cleared to zero).

5.4.5 Host's Copy of the HPCQ Consumer Index Register

Register Address: Determined by the host
Reset Value: Determined by the host

Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Value is undefined.
7..0	Queue Index	Queue Index	The consumer index value of the HPCQ.

Table 5.12 Host's Copy of the HPCQ Consumer Index Register.

Host's Copy of the HPCQ Consumer Index Register Notes

1. This memory location described by the HPCQ Consumer Index Address register contains the host's copy of Tachyon's HPCQ consumer index.
2. Tachyon updates this index when it reads an HPCQ entry.

5.5 IMQ Registers

5.5.1 IMQ Base Register

Register Address: 0x0080
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..0	Base Address	Base Address	The physical address in host memory of the start of the IMQ.

Table 5.13 IMQ Base Register.

IMQ Base Register Notes

1. The IMQ must be aligned on a sizeof(queue) boundary. The minimum size of the IMQ is 128 bytes (bits 6..0 are cleared to zero).
2. When the host writes to the IMQ Base register, Tachyon clears the corresponding producer index to zero; therefore, the host must not write to this register after initialization.

5.5.2 IMQ Length Register

Register Address: 0x0084
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Length	Queue Length	The number (zero-based) of IMQ entries.

Table 5.14 IMQ Length Register.

IMQ Length Register Notes

1. The Queue Length field must be a power of 2. The minimum queue length is 4 entries corresponding to a programmed value of 3. The maximum queue length is 256 entries corresponding to a programmed value of 255.
2. When the host writes to the IMQ Length register, Tachyon clears the corresponding consumer index to zero; therefore, the host must not write to this register after initialization.

5.5.3 IMQ Consumer Index Register

Register Address: 0x0088
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Index	Queue Index	The consumer index value of the IMQ entry following the last entry processed by the host.

Table 5.15 IMQ Consumer Index Register.

IMQ Consumer Index Register Notes

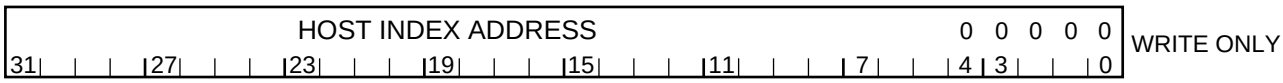
1. This register is used by the host to indicate the completion messages that have been processed by the host and the number of IMQ entries available to Tachyon for posting new completion messages. The host must process completion messages in sequential order and return them to Tachyon in sequential order. As Tachyon generates each interrupt, the host reads the copy of Tachyon's producer pointer in host memory. This value, along with the host's copy of its consumer index, gives the host an indication of how many completion messages Tachyon has posted since the last interrupt. The host processes each completion message and then writes the index of the next entry following the last one it processed.

2. Tachyon uses a pulsed interrupt line that is asserted only once until the host writes back to the IMQ consumer index. This is important in implementations that use latched interrupts. Always enable interrupts before writing the IMQ consumer index. A race condition may occur if the following algorithm is not used.

```
do interrupts
{
      . . .
      . . .
}
enable interrupts
write IMQ consumer index
```

5.5.4 IMQ Producer Index Address Register

Register Address: 0x008C
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..0	Host Index Address	Host Index Address	The address of the host's copy of the IMQ producer index.

Table 5.16 IMQ Producer Index Address Register.

IMQ Producer Index Address Register Notes

1. The Inbound Message Queue Index Address register contains the host memory address where Tachyon maintains its producer index.

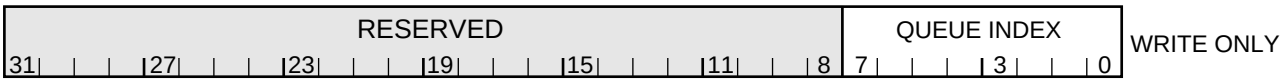
2. The host index address must be aligned on a 32-byte boundary (bits 4..0 are cleared to zero).

3. This index resides in host memory to allow the host fast access to the producer index.

4. The host must not access this register after initialization. The host enables the IMQ by writing to the IMQ Producer Index Address register; therefore, the host should initialize this register after the IMQ Base and IMQ Length registers are initialized.

5.5.5 Host's Copy of the IMQ Producer Index

Register Address: Determined by the host
Reset Value: Determined by the host



Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Index	Queue Index	The address of the host's copy of the producer index value of the IMQ.

Table 5.17 Host's Copy of the IMQ Producer Index.

Host's Copy of the IMQ Producer Index Register Notes

1. This memory location described by the IMQ Producer Index Address register contains the host's copy of Tachyon's producer Index.
2. Tachyon updates this index when it writes an IMQ entry.

5.6 MFSBQ Registers

5.6.1 MFSBQ Base Register

Register Address: 0x00C0
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..0	Base Address	Base Address	The physical address in host memory of the start of the MFSBQ.

Table 5.18 MFSBQ Base Register.

MFSBQ Base Register Notes

1. The MFSBQ must be aligned on a sizeof(queue) boundary.
2. The minimum size for the MFSBQ is 64 bytes (bits 5..0 are cleared to zero).
3. When the host writes a value to the MFSBQ Base register, Tachyon clears the corresponding consumer index to zero; therefore, the host must not write to this register after initialization.

5.6.2 MFSBQ Length Register

Register Address: 0x00C4
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Length	Queue Length	The number (zero-based) of MFSBQ entries.

Table 5.19 MFSBQ Length Register.

MFSBQ Length Register Notes

1. The Queue Length field must be a power of 2. The minimum queue length is 2 entries, corresponding to a programmed value of 1. The maximum queue length is 256 entries, corresponding to a programmed value of 255.
2. When the host writes to the MFSBQ length register, Tachyon clears the corresponding consumer index to zero; therefore, the host must not write to this register after initialization.

5.6.3 MFSBQ Producer Index Register

Register Address: 0x00C8
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Index	Queue Index	The producer index value that points to the end of the MFSBQ.

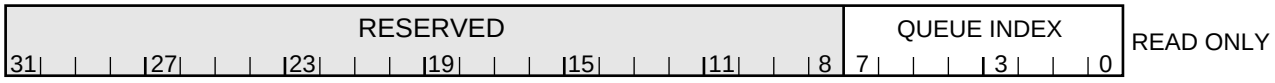
Table 5.20 MFSBQ Producer Index Register.

MFSBQ Producer Index Register Notes

1. The host uses the MFSBQ Producer Index Register to pass buffers to Tachyon for use in reassembling incoming multiframe sequences in host memory.
2. The host must initialize all other MFSBQ registers before it writes to this register.

5.6.4 MFSBQ Consumer Index Register

Register Address: 0x00CC
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Index	Queue Index	The MFSBQ entry that Tachyon is currently using to process an MFS.

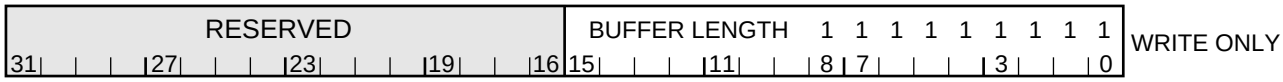
Table 5.21 MFSBQ Consumer Index Register.

MFSBQ Consumer Index Register Note

1. Tachyon updates this register to indicate the MFSBQ entry that it is currently using to process the incoming multiframe sequence.

5.6.5 MFS Buffer Length Register

Register Address: 0x00D0
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..16	Reserved	Reserved	Initialize to zero.
15..0	Buffer Length	Buffer Length	The (zero-based) length in bytes of the MFS receive buffers.

Table 5.22 MFS Buffer Length Register.

MFS Buffer Length Register Notes

1. The Buffer Length field must be a power of 2 bytes.
2. The minimum buffer length is 512 bytes corresponding to a programmed value of 511.
3. The reset value of this register is 511.
4. The maximum buffer length is 65,536 bytes, corresponding to a programmed value of 65,535.
5. When the host writes to this register, Tachyon masks bits 8..0 and always sets them to one.
6. The host should not modify the contents of this register after initialization.

5.7 SFSBQ Registers

5.7.1 SFSBQ Base Register

Register Address: 0x0100
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..0	Base Address	Base Address	The physical address in host memory of the start of the SFSBQ.

Table 5.23 SFSBQ Base Register.

SFSBQ Base Register Notes

1. The SFSBQ must be aligned on a sizeof(queue) boundary.
2. The minimum size of the SFSBQ is 64 bytes (bits 5..0 are cleared to zero).
3. When the host writes to the SFSBQ Base register, Tachyon clears the corresponding consumer index to zero; therefore, the host must not write to this register after initialization.

5.7.2 SFSBQ Length Register

Register Address: 0x0104
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Length	Queue Length	The number (zero-based) of SFSBQ entries.

Table 5.24 SFSBQ Length Register.

SFSBQ Length Register Notes

1. The Queue Length field must be a power of 2. The minimum queue length is 2 entries corresponding to a programmed value of 1. The maximum queue length is 256 entries corresponding to a programmed value of 255.
2. When the host writes to the SFSBQ Length register, Tachyon clears the corresponding consumer index to zero; therefore, the host must not write to this register after initialization.

5.7.3 SFSBQ Producer Index Register

Register Address: 0x0108
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..00	Queue Index	Queue Index	The producer index value that points to the end of the SFSBQ.

Table 5.25 SFSBQ Producer Index Register.

SFSBQ Producer Index Register Notes

1. The host uses the SFSBQ Producer Index register to pass buffers to Tachyon for use in receiving incoming single frame sequences in host memory.
2. The host must initialize all other SFSBQ registers before it writes to this register.

5.7.4 SFSBQ Consumer Index Register

Register Address: 0x010C
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..8	Reserved	Reserved	Initialize to zero.
7..0	Queue Index	Queue Index	The SFSBQ entry Tachyon is currently using to process SFSs.

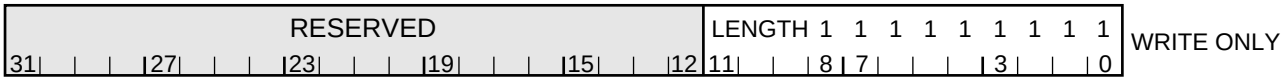
Table 5.26 SFSBQ Consumer Index Register.

SFSBQ Consumer Index Register Note

1. Tachyon updates this register with the index of the SFSBQ entry that it is currently using to process the incoming single frame sequences.

5.7.5 SFS Buffer Length Register

Register Address: 0x0110
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..16	Reserved	Reserved	Initialize to zero.
15..0	Length	Buffer Length	The (zero-based) length in bytes of the SFS receive buffers.

Table 5.27 SFS Buffer Length Register.

SFS Buffer Length Register Notes

1. The Length field must be a power of 2 bytes.
2. The minimum buffer length is 512 bytes corresponding to a programmed value of 511.
3. The reset value of this register is 31.
4. The maximum buffer length is 4096 bytes, corresponding to a programmed value of 4095.
5. When the host writes to this register, Tachyon masks bits 8..0 and always sets them to one.
6. The host should not modify the contents of this register after initialization.

5.8 SEST Registers

5.8.1 SEST Base Register

Register Address: 0x0140
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..0	Base Address	Base Address	The physical address in host memory of the start of the SEST.

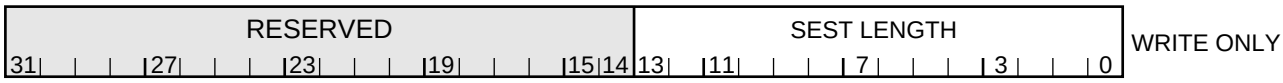
Table 5.28 SEST Base Register.

SEST Base Register Notes

1. The SEST must be aligned on a sizeof(SEST) boundary. For example, if the SEST is 512 bytes, then bits 8..0 of the SEST Base register are cleared to zero.
2. The minimum size for the SEST is 32 bytes (bits 4..0 are cleared to zero).

5.8.2 SEST Length Register

Register Address: 0x0144
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..14	Reserved	Reserved	Initialize to zero.
13..0	SEST Length	SEST Length	The number (zero-based) of SEST entries.

Table 5.29 SEST Length Register.

SEST Length Register Note

1. The SEST Length must be a power of 2. The minimum SEST Length is 1 entry, corresponding to a programmed value of 0. The maximum SEST Length is 65,536 entries corresponding to a programmed value of 65,535.

5.8.3 SCSI Buffer Length Register

Register Address: 0x0148
Reset Value: 0x00000000

Bit(s)	Field Label	Field Name	Description
31..16	Reserved	Reserved	Initialize to zero.
15..0	Buffer Length	Buffer Length	The (zero-based) length in bytes of the SCSI receive buffers.

Table 5.30 SCSI Buffer Length Register.

SCSI Buffer Length Register Notes

1. The host should not modify the contents of this register after initialization.

2. If the host cleared bit 6 in the Tachyon Configuration register to zero (OOO Reassembly), then the buffer size must be a power of 2, and the minimum value is 512 bytes, corresponding to a programmed value of 511.

3. If the host sets bit 6 in the Tachyon Configuration register to one (In Order Reassembly), then the buffer size must be a multiple of 4 bytes, so that the minimum value is 4 bytes, corresponding to a programmed value of 3.

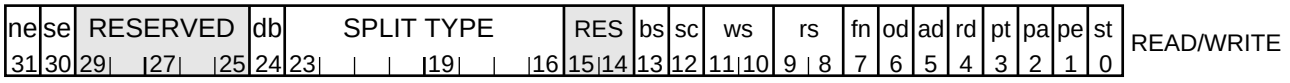
4. The maximum value is 65,536 bytes, corresponding to a programmed value of 65,535 bytes.

5. When the host writes to this register, it must always set bits 1..0 each to one.

5.9 Tachyon Registers

5.9.1 Tachyon Configuration Register

Register Address: 0x0184
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31	ne	TCP/UDP Assists Enable	Set to one to enable TCP/UDP hardware assists.
30	se	SCSI Enable	Set to one to enable SCSI FCP hardware assists.
29..25	Reserved	Reserved	Initialize to zero.
24	db	Disable AUTO P_BSY	When the host sets this bit to one, Tachyon does not automatically P_BSY new MFS frames while a current MFS is being re-assembled. Instead, it passes the new frames to the host.
23..16	Split Type	Split Type	The host-specified Fibre Channel frame type for which to perform header/data splits. Tachyon splits by default for type 5 (LLC/SNAP packets). The host uses this field to specify an additional frame type. If the host clears this field to zero, Tachyon disables splitting for a second type.
15..14	Res	Reserved	Initialize to zero.
13	bs	Bad SCSI Auto ACK	If the host sets this bit to one, Tachyon generates an ACK for bad SCSI frames. If the host clears this bit to zero, the host is responsible for generating the ACK.
12	sc	SCSI Command Auto ACK	If the host sets this bit to one, Tachyon generates an ACK for the SCSI command frame. If the host clears this bit to zero, the host is responsible for generating the ACK.
11..10	ws	Write Stream Size	The maximum number of Write transactions to perform per bus tenancy.
			ws value: Maximum Stream Count 00: 1 01: 4 10: 16 11: 64
9..8	rs	Read Stream Size	The maximum number of Read transactions to perform per bus tenancy.
			rs value: Maximum Read Stream Count 00: 1 01: 4 10: 16 11: 64

Table 5.31 Tachyon Configuration Register.

5.9.1 Tachyon Configuration Register (Continued)

Bit(s)	Field Label	Field Name	Description
7	fn	ACK Generation Assist Enable	The host sets this bit to one to inform Tachyon, as the recipient of frames, to look at the ACK generation assist bits (bits 12 and 13) of the F_CTL field of the Fibre Channel header. These bits inform Tachyon which ACK model to use when responding to received frames. Refer to “5.10.9 Acknowledgement of Received Frames” on page 59.
6	od	OOO Reassembly Disable	When the host sets this bit to one, Tachyon does not reassemble OOO SCSI FCP frames. This allows for more freedom in selecting receive buffer sizes. The host should not set this bit if the topology allows OOO delivery.
5	ad	ACK Disable	When the host sets this bit to one, Tachyon disables automatic ACK generation. Tachyon then passes all received frames to the host as unknown frames via the SFSBQ. Tachyon does not perform any automatic processing of sequences. The host should use this for debugging purposes only.
4	rd	Retry Disable	When the host sets this bit to one, Tachyon disables retries of the first frame of a sequence. The first BSY that Tachyon receives will terminate the sequence.
3	pt	Point-to-Point	The host sets this bit to one to indicate that it has detected that Tachyon is directly connected to another N_Port. If this bit is set to one and the OSM tries to establish an outgoing Class I connection, then the ISM busies any attempts for inbound Class 1 connections.
2	pa	Parity Enable	Set to one to enable parity checking within Tachyon.
1	pe	Parity Even	The host sets this bit to one for even parity and clears it to zero for odd parity. This bit is valid only if the host has parity enabled. The default value for this bit is one. Refer to “6.1.13 Parity” on page 63.
0	st	Stacked Connect Requests	The host sets this bit to one when it detects that the fabric supports stacked connect requests.

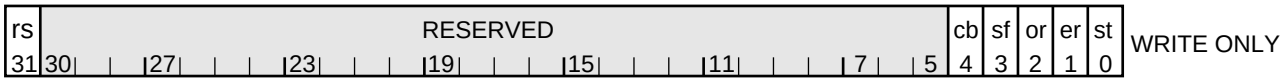
Table 5.31 Tachyon Configuration Register. (Continued)

Tachyon Configuration Register Notes

1. The host uses the Tachyon Configuration register to initialize and configure Tachyon’s operating modes.
2. The Stacked Connect Requests (st) and Point-to-Point (pt) bits of the Tachyon Configuration register are the only bits that the host can modify after initial configuration.

5.9.2 Tachyon Control Register

Register Address: 0x0188
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31	rs	Software Reset	The host sets this bit to one to initiate a software reset of Tachyon. 1. At reset, Tachyon clears all registers to zero, unless otherwise noted. Reset is defined as power-on, a hardware reset, or a software reset. 2. While Tachyon clears registers to zero at reset, certain registers (such as EE_Credit Zero Timer and BB_Credit Zero Timer register) begin counting up immediately following a reset. As a result, if the host reads a register immediately after a reset, the value may be non-zero. 3. If the host reads an invalid or Write only (W) register, the transaction completes normally, and Tachyon returns 0x00000000. 4. Tachyon ignores bits 31..9 of the address during register accesses. 5. If the host writes to Read only (R) registers, the transaction completes but Tachyon does not write the data to the register.
30..5	Reserved	Reserved	Initialize to zero.
4	cb	Clear Deferred P_BSY	The host sets this bit to one to clear Tachyon's Deferred P_BSY flag. This allows Tachyon to ACK MFSs normally until the next MFS collision occurs.
3	sf	SCSI Freeze	The host sets this bit to one to stop the processing of XFER_RDYs for outbound exchanges and Outbound SEST Entries. The host clears this bit to zero to resume processing. This bit is cleared to zero for normal operation. This bit affects outbound operations only.
2	or	OCQ Reset	The host sets this bit to one to clear the OCQ parameters. Tachyon resets the OCQ producer and consumer indices to zero. Tachyon may not return an outbound_completion message for the last OCQ entry read if the OCQ is reset.
1	er	Error Release	The host sets this bit to one to unfreeze the OSM from the Error state. Tachyon does not allow the OSM to unfreeze if the Link Down bit in the Frame Manager Status register is set to one.
0	st	Status Request	The host sets this bit to one to request Tachyon to DMA current status to the host.

Table 5.32 Tachyon Control Register.

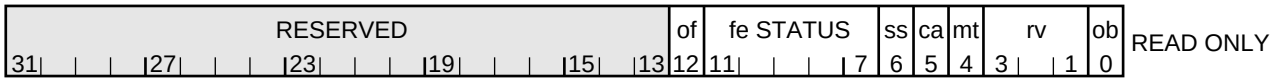
Tachyon Control Register
Notes

1. The host uses the Tachyon Control register to reset all or portions of Tachyon as well as to request a dump of all internal Tachyon status.

2. The OCQ reset does not necessarily occur the instant that the host writes to the Tachyon Control register. Tachyon performs the reset when the channel is at an idle point to prevent hanging the remainder of Tachyon in the middle of an operation. The Tachyon Status register has a status bit that indicates whether or not the reset procedure is still in progress. Tachyon should always complete the reset procedure in less than ~30 clocks, but Tachyon updates the reset status bit for cases where the host must guarantee the reset is complete before proceeding.

5.9.3 Tachyon Status Register

Register Address: 0x018C
Reset Value: HW dependent



Bit(s)	Field Label	Field Name	Description	
31..13	Reserved	Reserved	Value is undefined	
12	of	Outbound FIFO	Tachyon sets this bit to one when the outbound FIFO either is empty or is in the process of being emptied by the Frame Manager. If Tachyon clears this bit to zero, then the FIFO contains a frame that is not being moved.	
11..7	fe status	Fatal Error Status	Allows the host to determine what caused ERROR_L to be asserted.	
			State	Definition
			00000 00001 00010 00100 01000 10000	Tachyon has not logged an error Frame Manager outbound data parity error Slave write data parity error Type signals not asserted correctly for slave transactions. Address parity error DMA read data parity error
6	ss	SCSI Freeze Status	Tachyon sets this bit to one to indicate that the processing of XFER_RDYs and Outbound SEST Entries in the SEST has stopped. This bit corresponds to bit 3 of the Tachyon Control register.	
5	ca	OCQ Reset Status	Tachyon sets this bit to one to indicate that a reset of the OCQ is in progress.	
4	mt	Receive FIFO Empty	Tachyon sets this bit to one to indicate that the inbound data FIFO is empty.	
3..1	rv	Chip Revision	Tachyon's hardware revision code. Refer to the Tachyon Status register on page 46.	
0	ob	OSM Frozen	Tachyon sets this bit to one to indicate that the OSM is in a Frozen state due to an error.	

Table 5.33 Tachyon Status Register.

Tachyon Status Register Notes

1. The host uses the Tachyon Status register to read error information and operational status of the Tachyon chip.
2. The Chip Revision field reads as follows:

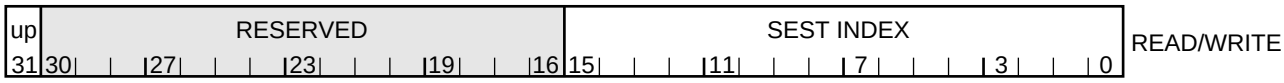
Description	Agilent Part Number	Bits 3..1	Release Date
Pre-Release 5 V Tachyon	HPFC-300K	000	January, 1995
Pilot 3.3 V Tachyon	HPFC-500P (HPFC-5000)	001	July, 1995
Pre-Production 3.3 V Tachyon Revision 1	HPFC-500K (HPFC-5000)	001	August, 1995
Pre-Production 3.3 V Tachyon Revision 2	HPFC-5000	010	February, 1996
Production 3.3 V Tachyon Revision 2	HPFC-5000	010	March, 1996

Table 5.34 Tachyon Chip Revisions.

No functional differences exist between HPFC-500P and HPFC-500K (Revision 001b). No functional differences are planned between the Pre-Production 3.3 V Tachyon Revision 2 and the Production 3.3 V Tachyon Revision 2 (Revision 010b).

5.9.4 Tachyon Flush SEST Cache Entry Register

Register Address: 0x0190
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31	up	Update	This bit indicates that Tachyon is able to handle an OX_ID flush request from the host. Set to one by the host when it wants to update the SEST entry. Cleared to zero by Tachyon when the cache update is complete.
30..16	Reserved	Reserved	Initialize to zero.
15..0	SEST Index	SEST Index	The index of the SEST entry the host wants updated.

Table 5.35 Tachyon Flush SEST Cache Entry Register.

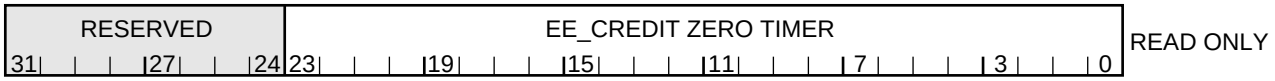
Tachyon Flush SEST Cache Entry Register Notes

1. The host uses this register to force Tachyon to write back any internal status for the indicated Inbound SEST Entry and to invalidate the Inbound SEST Entry. The host performs this operation when it detects an error with the exchange and wants to abnormally terminate it. The host should not use this register to flush Outbound SEST Entries since they are not cached on Tachyon. To terminate an outbound transaction abnormally, the host needs to clear only the Valid bit in the Outbound SEST Entry.

2. If no internal status is associated with the indicated Inbound SEST Entry, then Tachyon does nothing. Therefore, the host should clear the Valid bit in the Inbound SEST Entry before writing the register to prevent race conditions where Tachyon is trying to start processing an incoming transfer at the same time the host is trying to invalidate and flush the Inbound SEST Entry.

5.9.5 Tachyon EE_Credit Zero Timer Register

Register Address: 0x0194
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..24	Reserved	Reserved	Value is undefined.
23..0	EE_Credit Zero Timer	EE_Credit Zero Timer	The amount of time Tachyon has waited to transmit, but could not, because it had no EE_Credit.

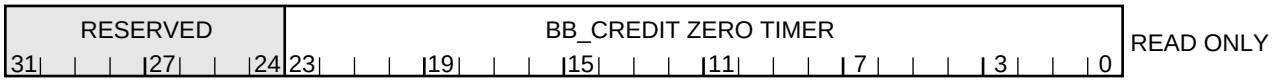
Table 5.36 Tachyon EE_Credit Zero Timer Register.

Tachyon EE_Credit Zero Timer Register Note

1. This register provides a timer that runs whenever the EE_Credit for a sequence goes to zero. This indicates to the host the time that Tachyon is congested due to lack of EE_Credit. The timer is clocked by a 10 us pulse which can result in the timer rolling over approximately every two minutes in a heavy congestion environment. If the host uses this timer, the host should read the timer frequently enough to detect rolling over.

5.9.6 Tachyon BB_Credit Zero Timer Register

Register Address: 0x0198
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..24	Reserved	Reserved	Value is undefined.
23..0	BB_Credit Zero Timer	BB_Credit Zero Timer	The amount of time Tachyon has waited to transmit, but could not, because it had no BB_Credit.

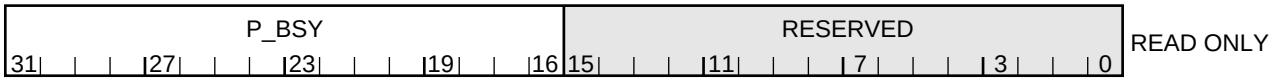
Table 5.37 Tachyon BB_Credit Zero Timer Register.

Tachyon BB_Credit Zero Timer Register Note

1. This register provides a timer that runs whenever the BB_Credit goes to zero. This indicates to the host the time that Tachyon is congested due to lack of credit. The timer is clocked by a 10 us pulse which can result in the timer rolling over approximately every two minutes in a heavy congestion environment. If the host uses this timer, the host should read the timer frequently enough to detect rolling over.

5.9.7 Tachyon Receive Frame Error Counter Register

Register Address: 0x019C
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..16	P_BSY	P_BSYs Sent	The number of frames received whose response was a P_BSY. Reading this register resets this counter to zero.
15..0	Reserved	Reserved	Value is undefined.

Table 5.38 Tachyon Receive Frame Error Counter Register.

Tachyon Receive Frame Error Counter Register Note

1. This register allows the host to monitor the number of busies (P_BSYs) transmitted by Tachyon.

5.10 Frame Manager Registers

5.10.1 Frame Manager Configuration Register

Register Address: 0x01C0
Reset Value: 0x00000000

AL_PA								BB_CREDIT								np	il	el	R	td	fa	aq	ha	sa	R	rf	if	lr	RES			READ/WRITE
31				27			24	23				19			16	15	14	13	12	11	10	9	8	7	6	5	4	3	2		0	

Bit(s)	Field Label	Field Name	Description
31..24	AL_PA	AL_PA	The AL_PA is the address the Frame Manager uses when arbitrating on the loop and the address that it recognizes in an OPN primitive signal. The host sets the AL_PA to an initial value. Tachyon sets this address after acquiring an AL_PA on the loop.
23..16	BB_Credit	BB_Credit	The amount of BB_Credit, as determined from login parameters. Valid only if Tachyon is an N_Port.
15	np	N_Port	Force Tachyon to start initialization as a non-loop N_Port. This bit should be cleared before issuing the Offline command (Frame Manager Control register).
14	il	Enable Internal Loopback	Enable Tachyon's internal loopback path.
13	el	Enable External Loopback	Assert the PLM loopback signal (EWRAP) to loopback data at the PLM.
12	R	Reserved	Initialize to zero.
11	td	Timer Disable	Disable the ED_TOV timer. For debugging purposes only.
10	fa	Loop Initialization Fabric Acquired Address	Indicates whether the AL_PA field was previously assigned by a fabric. If Tachyon does not acquire the AL_PA the host wrote into the AL_PA field, then Tachyon clears this bit to zero.
9	aq	Loop Initialization Previously Acquired Address	Indicates whether the AL_PA field was previously assigned by Loop Initialization. Tachyon sets this bit to one after acquiring an AL_PA on the loop. Refer to Frame Manager Configuration register note 6 on page 50.
8	ha	Loop Initialization Hard (Preferred) Address	Indicates whether the host set the AL_PA field from switches or another fixed address method. Tachyon clears this bit to zero after acquiring an AL_PA on the loop.
7	sa	Loop Initialization Soft Address	Indicates no AL_PA was provided, so Tachyon must participate in self-assignment during Loop Initialization. After acquiring an AL_PA on the loop, Tachyon clears this bit to zero.
6	R	Reserved	Initialize to zero.
5	rf	Respond to Fabric Address	Recognize the fabric AL_PA value of zero in addition to the assigned AL_PA. The host should not set this bit to one if a fabric exists on the loop.

Table 5.39 Frame Manager Configuration Register.

Bit(s)	Field Label	Field Name	Description
4	if	Initialize as Fabric	This bit causes the Frame Manager to use a D_ID and S_ID of zero when generating LISM frames on FC-AL. The host should not set this bit to one if a fabric exists on the loop.
3	lr	Login Required	This bit indicates that Tachyon should assert the Fabric Login bit in LIFA, LIPA, LIHA, and LISA frames. This bit is valid only when the host also sets the Initialize as Fabric (if) bit.
2..0	Reserve	Reserved	Initialize to zero.

Table 5.39 Frame Manager Configuration Register. (Continued)

Frame Manager Configuration Notes

1. The host should only modify the Frame Manager Configuration register while the Frame Manager is in the OFFLINE state (except for BB_Credit, refer to Note 2 below). For a Fabric as an L_Port, other Frame Manager Configuration register bits may change.

2. The BB_Credit field (bits 23..16) and the Fabric Acquired Address bit (fa, bit 10) are the only fields/bits which can be modified while the Frame Manager is online.

3. While online as an N_Port, if the BB_Credit field is changed, the host should issue the Link Reset command (in the Frame Manager Control register) to synchronize the BB_Credit with the remote node.

4. If BB_Credit is not initialized to a non-zero value, then Tachyon never issues a BB_Credit warning in N_Port mode. The BB_Credit default is zero.

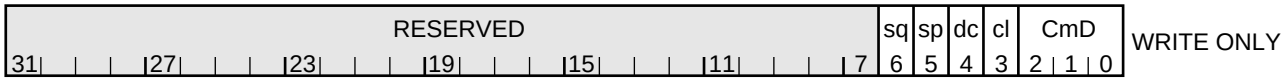
5. If the host sets the Fabric Acquired Address (fa, bit 10) to one, then the host must also set the Previously Acquired Address (aq, bit 9) to one or an error condition may occur.

6. Setting more than one of the following bits is illegal: Previously Acquired Address (aq, bit 9), Hard Address (ha, bit 8), and Soft Address (sa, bit 7). Tachyon does not check for this situation. Therefore, setting more than one address bit produces unpredictable results. The host must set one of these bits (fa, aq, ha, and sa) for proper loop participation; otherwise, Tachyon cannot acquire an AL_PA.

7. If the host wants non-participating mode on the loop, the host should clear bits 7..10 to zero.

5.10.2 Frame Manager Control Register

Register Address: 0x01C4
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..7	Reserved	Reserved	Initialize to zero.
6	sq	Primitive Sequence	This bit has a meaning only in the Host Control state when a one is written to the Send Primitive register (sp) bit. One occurrence of the primitive in the Primitive Register field of the Frame Manager Primitive register is sent when this bit contains a one. At least 12 occurrences of the primitive are sent when this bit contains a zero.
5	sp	Send Primitive Register	This bit has a meaning only in the Host Control state. It has no meaning when cleared to zero. When a one is written to this bit, it directs the Loop State Machine to send the primitive in the Primitive Register field of the Frame Manager Primitive register. The number of times the primitive is sent is controlled by the Primitive Sequence (sq) bit. This bit is automatically cleared to zero after the primitive(s) have been sent. Writing a one to this bit while primitives are being sent has no effect.
4	dc	Don't Close Loop Request	This bit forces the Loop State Machine to remain open after sending a sequence. When this bit is set to one, the loop is not closed until the Close Loop Request (cl) bit in the Frame Manager Control register is set to one. The Close Loop Request bit overrides the effect of the Loop Close (cl) bit in the Tachyon Header Structure for the current outbound sequence, preventing CLOSE after any frame in the sequence. When Tachyon closes the loop, it does not automatically clear the Don't Close Loop Request (dc) bit to zero.
3	cl	Close Loop Request	This bit forces the Loop State Machine to send a loop CLS. Tachyon does not transmit the CLS until it has sent all of the frame data from the outbound FIFO. After Tachyon closes the loop, it automatically clears this bit to zero.
2..0	Cmd	State Machine Command	Command Port State Machine operations:

Field Value	Command Name	Description
000 001	NOP	No command.
010	Host Control	Directs the Loop State Machine to transition to the Host Control state.

Table 5.40 Frame Manager Control Register.

5.10.2 Frame Manager Control Register (Continued)

			Field Value	Command Name	Description
			011	Exit Host Control	Directs the Loop State Machine to exit the Host Control state.
			100	Link Reset	Forces the Port State Machine to the LRI state where LR is transmitted.
			101	Offline	Forces the Frame Manager to go offline and stay offline. This is the power up state.
			110	Initialize	Forces the Frame Manager to start initialization. Refer to the Frame Manager Control register note 1 below.
			111	Clear LF	Enables the Port State Machine to transition out of the Link Failure state.

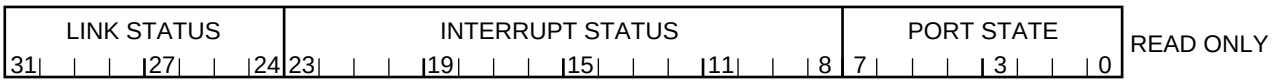
Table 5.40 Frame Manager Control Register. (Continued)

Frame Manager Control Register Note

1. If the host programs the Initialize Command when the link is up in N_port mode, Tachyon ignores the command. If the host programs the Initialize Command when the link is up in L_port mode, Tachyon performs Loop Initialization.

5.10.3 Frame Manager Status Register

Register Address: 0x01C8
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
	Link Status	Link Status	Link Status comprises the following sub-fields.
31	lp	Loop	A loop circuit has been established.
30	tp	Transmit Parity Error	This bit is set to one when Tachyon detects an internal data parity error. The host clears this error only by performing a hardware reset.
29	np	Non-Participat-ing	The port could not successfully complete Loop Initialization and is not participating in the loop.
28..27	par_id	Parallel ID	These two bits reflect the external PAR_ID bits received by the Frame Manager. Bit 28 is PAR_ID[1] and bit 27 is PAR_ID[0]. Refer to “4.3 Physical Link Module (PLM) Interface” on page 19.
26	lflt	Laser Fault	The PLM has detected a laser fault. The host must reset the PLM with EWRAP.
25	os	Out of Syn-chronization	The port has lost synchronization with the incoming data stream.
24	ls	Loss of Signal	The port is not receiving a signal from the remote node.
	Interrupt Status	Interrupt Status	Interrupt Status comprises the following sub-fields. These conditions generate a completion message and an interrupt to the host. The host clears these conditions by reading this register.
23..20	Reserved	Reserved	Value is undefined.
19	nos/ols	NOS/OLS Received	Tachyon received a NOS or OLS.
18	lst	Loop State Timeout	The Loop State Machine is in one of the following states: ARB, OPEN, OPENED, XMIT CLS, or RX CLS for longer than ED_TOV.
17	lipf	LIPf	LIPf has been received. A LIPf is a LIP indicating a loop failure, either LIP(F8, AL_PS) or LIP(F8, F7).
16	ba	Bad AL_PA	This bit indicates that an OPN primitive signal was sent to an AL_PA which did not respond.
15	pr_rxd	Primitive Received	The primitive in the Primitive Register field of the Frame Manager Primitive register was received while in the Host Control state.
14	pr_sent	Primitive Transmitted	The primitive in the Primitive Register field of the Frame Manager Primitive register has been transmitted (12 times if the sq bit of the Frame Manager Control register is set to one.)

Table 5.41 Frame Manager Status Register.

5.10.3 Frame Manager Status Register (Continued)

Bit(s)	Field Label	Field Name	Description
13	lg	Fabric Login Required	Loop Initialization detected a new fabric. The N_Port must perform fabric login.
12	lf	Link Failure	This bit indicates that one of the following conditions has been detected: Loss of Sync for greater than ED_TOV, Loss of Signal, Laser Fault, or Elastic Store Error.
11	ce	Credit Error	This bit indicates a BB_Credit of zero for ED_TOV error condition.
10	ew	Elastic Store Error	This bit indicates an error condition caused by an Elastic Store over-write or under-read. This indicates a serious timing difference between the receive and transmit clocks.
9	lup	Link Up	This bit indicates that the link has gone into the ACTIVE state or that the link has transitioned from O_I_PROTOCOL to MONITORING on the loop. If both this bit and the ldwn bit are asserted, the loop has reinitialized or a link reset has occurred.
8	ldwn	Link Down	This bit indicates that the link has gone inactive or that Loop Initialization has been reinitialized. The OSM freezes when the link goes down and needs to be unfrozen when the link is back up. Tachyon does not unfreeze the OSM if this bit is set to one.
	Port State	Port State	Port State comprises the following sub-fields.
7..4	lfsm	Loop State Machine	The Fibre Channel Arbitrated Loop State Machine. Refer to the “FC-AL” for state definitions.

State	Definition	State	Definition
0000	MONITORING	1000	INITIALIZING
0001	ARBITRATING	1001	O_I INIT FINISH
0010	ARBITRATION WON	1010	O_I PROTOCOL
0011	OPEN	1011	O_I LIP RECEIVED
0100	OPENED	1100	HOST CONTROL
0101	XMITTED CLOSE	1101	LOOP FAIL
0110	RECEIVED CLOSE	1111	OLD PORT
0111	TRANSFER		

3..0	pfsm	Port State Machine	N_Port State Machine. Refer to the FC-PH for state definitions.

State	Definition	State	Definition
0000	OFFLINE	0110	LR2
0001	OL1	0111	LR3
0010	0L2	1001	LF1
0011	0L3	1010	LF2
0101	LR1	1111	ACTIVE

Table 5.41 Frame Manager Status Register. (Continued)

5.10.4 Frame Manager RT_TOV/AL_TIME & ED_TOV Register

Register Address: 0x01CC
Reset Value: 0x001001F5

Bit(s)	Field Label	Field Name	Description
31..25	Reserved	Reserved	Initialize to zero.
24..16	RT_TOV/AL_TIME	RT_TOV/AL_TIME	The host uses this register to program both the Receiver Transmitter Time Out Value (RT_TOV) and the Arbitrated Loop Time Out (AL_TIME) value. The host should program this value to 100 milliseconds (ms) for RT_TOV and 15 ms for AL_TIME. The default is 15 ms. If the host does not know the topology prior to initialization, this value must be programmed to 15 ms for Loop Initialization and reprogrammed to 100 ms if it is determined that no loop exists.
15..0	ED_TOV	ED_TOV	The Error Detect Time Out Value (ED_TOV) in milliseconds. The default is 500 ms.

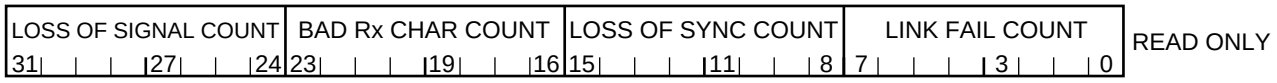
Table 5.42 Frame Manager RT_TOV/AL_TIME and ED_TOV Register.

Frame Manager RT_TOV/ AL_TIME & ED_TOV Register Note

1. The host should only modify the Frame Manager RT_TOV/ AL_TIME & ED_TOV register while the Frame Manager is in the OFFLINE State.

5.10.5 Frame Manager Link Error Status Counters #1 Register

Register Address: 0x01D0
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..24	Loss of Signal Count	Loss of Signal Count	Indicates the number of times the Frame Manager detected a low to high transition on the lnk_unuse signal.
23..16	Bad Rx Char Count	Bad Received Character Count	Indicates the number of times the 8B/10B decode detected an invalid 10-bit code. FC-PH denotes this value as “Invalid Transmission Word during frame reception.” This field may be non-zero after initialization. After initialization, the host should read this value to determine the correct starting value for this error count.
15..8	Loss of Sync Count	Loss of Sync Count	Indicates the number of times the loss of sync is greater than RT_TOV.
7..0	Link Fail Count	Link Fail Count	Indicates the number of times the Frame Manager detected a NOS or other initialization protocol failure that caused a transition to the Link Failure state.

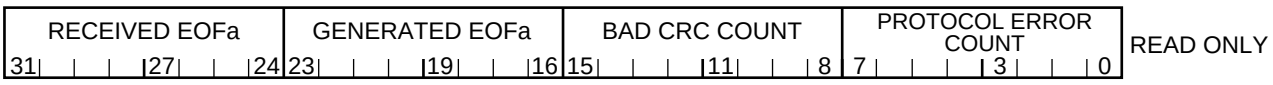
Table 5.43 Frame Manager Link Error Status Counters #1 Register.

Frame Manager Link Error Status Counters #1 Register Note

1. This register contains four error counters that Tachyon increments each time the associated error occurs. When these counters reach the maximum count (0xff), they rollover to 0x00 and continue counting. The host should poll these error counters every second or so. Since these errors should be infrequent, each counter is only 8 bits in length. The host must maintain longer counters if needed. A read of this register resets the counters to zero.

5.10.6 Frame Manager Link Error Status Counters #2 Register

Register Address: 0x01D4
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..24	Received EOFa	Received EOFa	The number of frames containing an EOFa delimiter that Tachyon has received.
23..16	Generated EOFa	Generated EOFa	The number of problem frames that Tachyon has received that caused the Frame Manager to attach an EOFa delimiter. Frames that Tachyon discarded due to internal FIFO overflow are not included in this or any other statistic.
15..8	Bad CRC Count	Bad CRC Count	The number of bad CRC frames that Tachyon has received.
7..0	Protocol Error Count	Protocol Error Count	The number of protocol errors that the Frame Manager has detected.

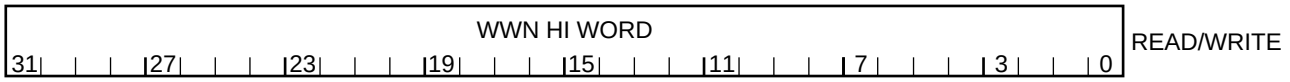
Table 5.44 Frame Manager Link Error Status Counters #2 Register.

Frame Manager Link Error Status Counters #2 Register Note

1. This register contains four error counters that Tachyon increments each time the associated error occurs. When these counters reach the maximum count (0xff), they rollover to 0x00 and continue counting. The host should poll these error counters every second or so. Since these errors should be infrequent, each counter is only 8 bits in length. The host must maintain longer counters if needed. When the host reads this register, Tachyon resets the counters to zero.

5.10.7 Frame Manager World Wide Name Hi Register

Register Address: 0x01E0
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..0	WWN Hi Word	World Wide Name High Word	The most significant four bytes of the WWN.

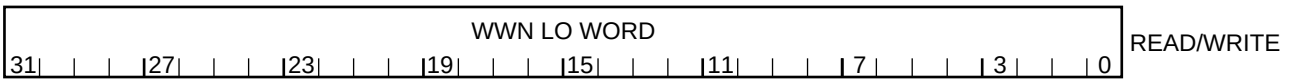
Table 5.45 Frame Manager World Wide Name Hi Register Register.

Frame Manager World Wide Name Hi Register Note

1. The host uses this register to indicate the high order 4 bytes of the 8-byte unique World Wide Name (WWN) that Tachyon should use during initialization. Note that Tachyon does not specify which type of WWN to use. It simply copies all 8 bytes from the registers to the loop initialization frames. The host should only modify the Frame Manager World Wide Name Hi register while Frame Manager is in the Offline state.

5.10.8 Frame Manager World Wide Name Lo Register

Register Address: 0x01E4
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..0	WWN Lo Word	World Wide Name Low Word	The least significant four bytes of the WWN.

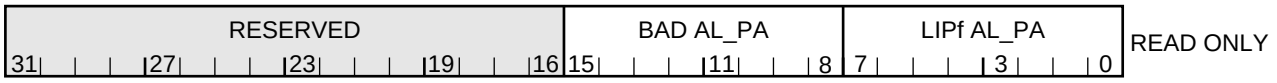
Table 5.46 Frame Manager World Wide Name Lo Register.

Frame Manager World Wide Name Lo Register Note

1. The host uses this register to indicate the low order 4 bytes of the 8-byte unique World Wide Name (WWN) that Tachyon should use during initialization. Note that Tachyon does not specify which type of WWN to use. It simply copies all 8 bytes from the registers to the loop initialization frames. The host should only modify the Frame Manager World Wide Name Lo register while Frame Manager is in the Offline state.

5.10.9 Frame Manager Received AL_PA Register

Register Address: 0x01E8
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..16	Reserved	Reserved	Value is undefined.
15..8	Bad AL_PA	Bad AL_PA	The AL_PA of an OPN primitive signal that was sent and returned without being accepted by the remote node.
7..0	LIPf AL_PA	LIPf AL_PA	The AL_PA of the most recent LIPf.

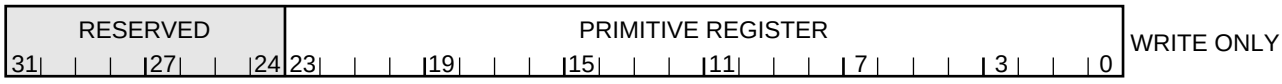
Table 5.47 Frame Manager Received AL_PA Register.

Frame Manager Received AL_PA Register Note

1. This register contains the 8-bit AL_PA which was received on the last LIPf or as a bad AL_PA. The LIPf AL_PA is only valid when the lipf bit is set in the Frame Manager Status register. The Bad AL_PA is only valid when the ba bit is set in the Frame Manager Status register.

5.10.10 Frame Manager Primitive Register

Register Address: 0x01EC
Reset Value: 0x00000000



Bit(s)	Field Label	Field Name	Description
31..24	Reserved	Reserved	Initialize to zero.
23..0	Primitive Register	Primitive Register	The lower three bytes of the ordered set to be sent.

Table 5.48 Frame Manager Primitive Register.

Frame Manager Primitive Register Note

1. The host writes to this register to tell Tachyon the lower 24 bits for the Primitive it should transmit in the host control state. Refer to “FC-AL” and “FC-PH” specifications for a list of ordered sets.

6. TSI

6.1.1 TSI Transaction Types

The transaction type is encoded onto the TYPE[2..0] signals during the address phase. The master of a transaction asserts AVCS_L along with the TYPE [ ] and TAD [ ] busses to indicate that an address cycle is in progress. TSI transaction types are noted in the following table.

TYPE[2..0]		Transaction Type	Transaction Name
Binary	Hexadecimal		
000	0x0	Single-word read	READ1
001	0x1	Double-word read	READ2
010	0x2	Four-word read	READ4
011	0x3	Eight-word read	READ8
100	0x4	Single-word write	WRITE1
101	0x5	Double-word write	WRITE2
110	0x6	Four-word write	WRITE4
111	0x7	Eight-word write	WRITE8

Table 6.1 TSI Transaction Types.

All transactions must be aligned to their size. For example, the three least significant word address bits for an 8 word transaction (TAD[4..2]) must all be zero. The two least significant bits (TAD[1..0]) are never used, and it is recommended they are cleared to zero for future compatibility.

In transactions where the host is master of the transaction and Tachyon is the responder, only single word Read and Write transaction types are allowed. Tachyon asserts ERROR_L in response to any other size transaction.

6.1.2 Data Structure Transaction Size

Data Structure Transaction Size

The following table shows the size of transactions that Tachyon uses when accessing host-based and SCSI data structures.

Host Data Structure	Operation
Outbound Command Queue (OCQ)	READ8
High Priority Command Queue (HPCQ)	READ8
Inbound Message Queue (IMQ)	WRITE8
Single Frame Sequence Buffer Queue (SFSBQ)	READ8
Multiframe Sequence Buffer Queue	READ8
Outbound SEST Entry Read	READ4, and sometime later, a READ8 is performed
Inbound SEST Entry Read	READ4, and sometime later, a READ1 is performed
Outbound SEST Entry Writeback	WRITE4 of words 0 through 3
Inbound SEST Entry Writeback	WRITE1 for each of words 0, 2, and 3

Table 6.2 Host Data Structure Transaction Size.

6.1.3 TSI Transaction Protocol

TSI provides a basic transaction protocol which uses two major operations: Write transactions and Read transactions. Every transaction has a master (which performs either a Write or a Read) and a responder. If the host is the master of a transaction, Tachyon is the responder in that transaction. Similarly, if Tachyon is the master of a transaction, then the host is the responder in that transaction.

The master of a transaction drives an address and transaction type onto the TAD [ ] and TYPE [ ] busses, respectively, while asserting AVCS_L to indicate the start of the transaction. If Tachyon masters a transaction, the host, as the responder, uses READY_L as its acknowledgment signal. Similarly, if the host masters the transaction, Tachyon, as the responder, uses READY_L as its acknowledgment signal. Transaction protocol, including timing and details of use of acknowledgment signals, is described in the following sections.

When Tachyon is the responder, only transactions of one word are allowed. Transaction sizes of other than one word, when Tachyon is the responder, causes Tachyon to assert ERROR_L.

6.1.4 Streaming

When Tachyon obtains mastership of TSI and has more than one transaction to perform, Tachyon may extend its bus tenancy and perform several TSI transactions (up to the maximum programmed limit) before releasing mastership. This is known as “streaming”.

Streaming Rules

1. The maximum number of transactions that may occur during a stream is programmable. The Write Stream Size and Read Stream Size fields in the Tachyon Configuration register indicate the maximum number of Write or Read transactions to perform per bus tenancy. This maximum number can be different for Writes and Reads.

2. Streaming occurs in only one direction, i.e., a Write and a Read transaction never occurs during the same stream.

3. Streaming may occur with different transaction sizes, e.g., a Read of 8 words and a Read of 4 words can occur during the same stream.

4. Streaming does not cross non-contiguous address locations, i.e., Tachyon releases ownership of the bus whenever the next address to be accessed is not sizeof (last_transaction) past the address of the last transaction.

5. Streaming does not cross A/L pairs.

6. Tachyon does not stream across frames.

Tachyon Terminates TSI Bus Tenancy When:

1. Tachyon determines that it does not have more data to transfer (e.g., an end of frame occurs, end of sequence data occurs, Tachyon encounters an error, etc).

2. In the current tenancy, Tachyon completes the number of transactions in the programmed maximum stream size in the Tachyon Configuration register.

3. The host asserts RETRY_L during a Read transaction.

4. Tachyon becomes 32-byte aligned and additional Read transactions are queued. Specifically, when Tachyon transfers from a NON-READ8 transaction to a READ8 transaction, bus tenancy ends and a new stream starts in a new tenancy. Tachyon must start a new stream to start asserting PREFETCH_L, if appropriate.

5. The Internal Outbound Frame FIFO is full.

6.1.5 Data Extend Using PREFETCH_L

Tachyon uses the PREFETCH_L to notify the host that Tachyon will request the next sequentially addressed block of data on the next TBR_L[1] bus tenancy. This enables the host to read the data for the next memory address into its cache in order to minimize the read access delay on TSI.

Data Prefetch Rules

1. Tachyon only asserts PREFETCH_L if Tachyon will read the next 32-byte block.

2. Tachyon only asserts PREFETCH_L for READ8 (word) transactions.

3. Tachyon may assert PREFETCH_L for all or part of the bus tenancy, which can contain one or more transactions.

4. Tachyon initially asserts PREFETCH_L with TBR_L[1].

5. PREFETCH_L is valid during the address cycle of each transaction. The host must sample it during the address cycle to determine whether or not the Tachyon reads the next sequential block of 8 words.

6. PREFETCH_L does not guarantee that Tachyon requests the data immediately. PREFETCH_L only indicates that the next transaction from the TBR_L[1] channel is a READ8 from the next sequential address. Tachyon may begin a new bus tenancy using TBR_L[0] at any time and perform any number of non-prefetched reads on that channel, independent of the prefetching activity present on TBR_L[1].

7. Prefetching can wrap across bus tenancies, e.g., if Tachyon asserts PREFETCH_L during the final phase of a streamed transaction, then Tachyon reads the prefetched data the next time it requests the bus using TBR_L[1].

8. During a bus tenancy, if Tachyon deasserts PREFETCH_L in an address cycle, then Tachyon does not assert the signal again during that particular bus tenancy. Tachyon begins a new bus tenancy for each contiguous block of data.

6.1.6 Address Cycle

For the address cycle, the bus master asserts the following signals:

1. The address of the transaction on TAD [31..0]

2. The calculated value of parity on the PARITY line (parity can be even, odd, or disabled)

3. The type of transaction on TYPE [2..0]

4. AVCS_L to indicate the validity of the address

Tachyon ignores TAD [31..9] in an address cycle when it is the responder. However, if parity is enabled, Tachyon checks parity for these bits, so TAD [31..9] should be driven to known values with valid PARITY.

The host must drive the TYPE[ ] signal in the Address cycle of a host mastered transaction and may continue to drive it throughout the transaction. The host must release all TYPE [2..0] signals before granting TSI to Tachyon.

6.1.7 Driving Bi-Directional Signals

Either the host or Tachyon can assert the AVCS_L and READY_L signals. The signals are both asserted low for just one cycle at a time. To operate one of these signals properly and guarantee timing margins, the host or Tachyon must drive the signal high for one cycle after it has been driven low. In the following cycle, it must be released (tri-stated). This is illustrated in all the timing diagrams provided in the examples in this chapter.

6.1.8 Write Transactions

A TSI Write transaction consists of an address cycle followed immediately by 1, 2, 4, or 8 data cycles. If the host masters the Write transaction, Tachyon asserts READY_L to acknowledge the transaction. If Tachyon masters the Write transaction, the host asserts READY_L to acknowledge the transaction. The responder may assert READY_L as soon as the cycle after the address cycle, or as late as after the last data cycle.

There is no timeout on TSI, so if Tachyon is the master, Tachyon waits to receive a READY_L or for a hard reset to occur. No other transactions are able to occur.

The Write transaction is not complete until the last data cycle or the acknowledgment cycle occurs, whichever occurs later. The master must stop driving TAD and PARITY the cycle after the last data cycle.

If Tachyon masters a Write transaction, it requests the bus using the TBR_L[0] line.

Only single word Write transactions are allowed when Tachyon is the responder.

6.1.9 Read Transactions

A TSI Read transaction consists of an address cycle, a turn cycle, zero or more wait cycles, the data (1, 2, 4, or 8 data cycles), and a recovery cycle. In the turn cycle, the master stops driving its TAD[ ], PARITY, and TYPE[ ] lines. After the turn cycle, the responder may drive data on the TAD[ ] lines and PARITY. READY_L must be asserted along with the first data cycle.

Only single word Read transactions are allowed when Tachyon is the responder.

For multiple word Read transactions, the remaining data must be transferred on

consecutive bus cycles until all data is returned. If the responder is not ready to return Read data in the cycle after the turn cycle, it delays the assertion of READY_L, thereby inserting wait cycles on the bus until data is available. If many wait cycles are needed before the responder is ready to return the read data, the interface is locked during this time.

If the Read data cannot currently be made available to Tachyon, the host may assert RETRY_L for one cycle, instead of asserting READY_L. On the cycle after the host asserts RETRY_L, Tachyon releases TBR_L, waits for TBG_L to be deasserted for one cycle, and then reasserts TBR_L to re-arbitrate for the bus.

If Tachyon asserts the PREFETCH_L signal concurrently with the TBR_L[1] signal and the host then decides to retry the read transaction using the RETRY_L signal, then the PREFETCH_L signal will remain asserted even after Tachyon has given up the bus.

RETRY_L Rules

1. The host may assert RETRY_L only during DMA read operations.

2. RETRY_L and READY_L are mutually exclusive, i.e., the host may only assert one of the signals per Read transaction.

3. The host asserts RETRY_L only prior to the data cycle, which is signaled by the responder asserting READY_L. Once the data cycles have started, the host may not assert RETRY_L on that transaction.

6.1.10 TSI Transaction Window

A TSI transaction window starts when the master asserts AVCS_L. For a Read transaction, the transaction window ends one cycle after the last data cycle, i.e., the recovery cycle is the end of the transaction window. For a Write transaction, the transaction window ends the cycle after the responder asserts READY_L or the cycle after the last data cycle, whichever is later. If the host wants to perform back-to-back Writes, it may do so without an idle cycle to separate the transactions. For example, the transaction window for the first transaction ends in the last data cycle or in the cycle in which the responder asserts READY_L, whichever is later.

6.1.11 TSI Transaction Ordering

Whenever more than one DMA channel is available between the host and a host bus adapter board, the possibility of an out of order transaction exists. For example, one block of data may arrive at the adapter board before an earlier requested block if the delays for the two channels are different.

Since Tachyon provides two DMA channels (via the two bus request lines), the following rules ensure that TSI transaction ordering is maintained.

Maintaining TSI Transaction Ordering

1. The order in which Tachyon initiates transactions is not altered if the host asserts RETRY_L. Thus, if the host aborts a Read operation by asserting RETRY_L, Tachyon immediately re-arbitrates for the bus in order to complete the aborted Read operation. No other Tachyon-mastered transactions, particularly other reads, occur until the original Read operation is completed.

2. Tachyon never asserts more than one bus request signal at a time. The two bus request lines, TBR_L[1:0] are mutually exclusive, i.e. the two are never asserted at the same time in an attempt to master two concurrent transactions.

3. Write transactions only occur on bus tenancies initiated with the TBR_L[0] (non-prefetch) signal, therefore Write transaction ordering is preserved.

Because Tachyon only initiates one Read and Write operation at a time, overall transaction ordering is maintained.

6.1.12 Endian-ness

Big Endian

Tachyon is big endian. On the address/data bus (TAD[ ]) and in all registers, bit 31 is the most significant bit and bit 0 is the least significant bit.

Little Endian

Refer to “A.2 Implementing Tachyon with Little Endian System”.

6.1.13 Parity

Tachyon asserts the Error Out signal (ERROR_L) if a parity error is detected (if parity is enabled), or if an invalid transaction size is used on a host-mastered Read or Write. The host must determine what caused the error, log the error if necessary,

and reset Tachyon to clear the error condition.

Parity is enabled or disabled via the Tachyon Configuration register. If enabled, Tachyon checks parity for both address and data. For a DMA Read that is mastered by Tachyon, if Tachyon detects a parity error, it asserts the ERROR_L signal two cycles after the cycle with bad parity. For a DIO Write transaction, if Tachyon detects a parity error, it asserts the ERROR_L signal one cycle after the cycle with bad parity for both address and data. For a DIO Read transaction, if Tachyon detects a parity error, it asserts the ERROR_L signal one cycle after the cycle with bad parity for address only. Refer to "6.1.14 Error Handling" on this page.

Due to the delayed nature of data parity errors, assertion of ERROR_L may overlap subsequent transactions. After Tachyon asserts ERROR_L, the host should read the Tachyon Status register to determine the cause of the error. The host must reset Tachyon to clear the error condition and deassert ERROR_L.

EVEN parity is the total number of ones on the address/data bus (TAD [31..0]) and the parity bit (PARITY) equals an even number. For example, if there is an odd number of ones on TAD [31..0], PARITY is driven high for EVEN parity.

ODD parity is the total number of ones on the address/data bus (TAD[31..0]) and the parity bit (PARITY) equals an odd number. For example, if there is an odd number of ones on TAD (31..0], PARITY is driven low for ODD parity.

Tachyon generates and drives the parity bit when it drives address or data information on TSI. If a Tachyon-driven transaction has a parity error, the host is responsible for resetting Tachyon to clear the error. During cycles where data or address are not valid (as defined by AVCS_L, READY_L, and TSI timing rules), parity is not valid.

6.1.14 Error Handling

Assertion of ERROR_L

Assuming that parity is enabled, Tachyon asserts ERROR_L for error conditions which occur in different TSI bus cycles:

1. Address parity error to Tachyon: Asserted in the next cycle.

2. TYPE signal not equal to binary 000 or 100 during Address cycle to Tachyon: Asserted in the next cycle.

3. Write data parity error to Tachyon: Asserted in the next cycle.

4. DMA Read data parity error: Asserted in the second cycle after the cycle with error.

5. Internal parity error: Asserted in any cycle on TSI.

Tachyon asserts ERROR_L and sets the appropriate bits in the Fatal Error Status field of the Tachyon Status register. If another error occurs, the Fatal Error Status field does not change and the new error is not logged. To determine the cause of the error, the host should read the Tachyon Status register.

Once Tachyon asserts ERROR_L, it will keep ERROR_L asserted until the host resets Tachyon by asserting RESET_L or by writing 0x8000 0000 to the Tachyon Control register.

For any address parity error, TYPE error, or write data parity error for a transaction to Tachyon, Tachyon does not return READY_L. ERROR_L is the only indication of Tachyon's response.

Tachyon Mastership Under ERROR_L

While Tachyon asserts ERROR_L, Tachyon cannot master any more DMA transactions. Tachyon completes the current transaction, then terminates its bus tenancy, no matter what streaming or prefetch state it is in. If Tachyon is arbitrating for the bus when it asserts ERROR_L, Tachyon continues arbitrating, but it releases TBR_L as soon as it sees TBG_L asserted, and it does not proceed with the bus transaction.

Tachyon Fibre Channel Operation Under ERROR_L

When Tachyon asserts ERROR_L, the OSM freezes. An outbound frame in progress on the link at the time of ERROR_L assertion finishes transmitting, but no more frames follow. The link state machine is still active, so Tachyon still responds to some Fibre Channel link and loop primitive sequences, like OLS or NOS. The host has limited ability to manage the situation since many Tachyon functions are disabled by the error.

Tachyon Response Under ERROR_L

When Tachyon asserts ERROR_L, Tachyon enters a state where it can no longer master transactions on the TSI. Even though Tachyon can no longer master transactions

on the TSI, all registers can be accessed. Tachyon does attempt to respond to slave accesses to status registers, which contain information about what type of error occurred. The slave accesses may fail if it experiences a fatal error.

If Tachyon asserts ERROR_L due to a host-mastered address parity error or host-mastered Write data parity error, Tachyon does not assert READY_L for that transaction.

If Tachyon is already asserting ERROR_L, and a host-mastered Write occurs, Tachyon does not accept data and asserts READY_L if no address or data parity errors exist. The only exception to this condition is the Tachyon Control register where the host can perform a soft reset. The Tachyon Control register accepts the data and asserts READY_L if no address or data parity error occurs.

If Tachyon is already asserting ERROR_L, and a host-mastered Read occurs, Tachyon asserts READY_L and returns data if no address parity error exists.

When Tachyon is asserting ERROR_L, the host must provide a timeout of at least 20 clocks from its assertion of AVCS_L. If Tachyon does not assert READY_L within this time, the transaction had a parity error. The host may begin a new transaction.

Host Error Handling for DMA Reads

The host is responsible for detecting parity errors in addresses for DMA Reads initiated by Tachyon. When the host detects these errors, it has four response options:

1. The host does not respond to Tachyon. It just leaves the bus locked up. Tachyon waits for a response and does not issue any further transactions. The host asserts RESET_L to reset Tachyon.

2. The host returns READY_L and data, but does not grant mastership to Tachyon. Tachyon has no indication that there was a problem. Tachyon only knows that the transaction completed. If Tachyon is streaming, Tachyon continues streaming, and does not relinquish the bus. The master should continue responding until the stream is exhausted. Then the master can prevent another Tachyon tenancy by withholding TBG_L. If streaming is disabled, then Tachyon terminates its tenancy after the current transaction. However, Tachyon could send incorrect data on the Fibre Channel since the host received an incorrect memory address.

3. The host returns READY_L with data containing incorrect parity. Tachyon is forced to assert ERROR_L and stop mastering on the bus.

4. The host asserts RETRY_L, which forces Tachyon to relinquish the bus immediately. The host should not grant mastership to Tachyon afterwards.

Host Error Handling of DMA Writes

The host must check and handle parity errors on DMA addresses and data for DMA Writes initiated by Tachyon. The host has only two possible responses for these Write transactions, because Write transactions do not have RETRY_L support and the host does not return any data, as for DMA reads:

1. The host does not respond to Tachyon. It just leaves the bus locked up. Tachyon waits for a response and does not issue any further transactions. The host asserts RESET_L to reset Tachyon.

2. The host returns READY_L and data, but does not grant mastership to Tachyon. Tachyon has no indication that there was a problem. Tachyon only knows that the transaction completed. If Tachyon is streaming, Tachyon continues streaming, and does not relinquish the bus. The master should continue responding until the stream is exhausted. Then the master can prevent another Tachyon tenancy by withholding TBG_L. If streaming is disabled, then Tachyon terminates its tenancy after the current transaction.

6.1.15 Reset

The RESET_L signal performs a synchronous reset of Tachyon. The host asserts RESET_L for at least 10 SCLK cycles to ensure proper operation. Tachyon starts in an arbitrary state and RESET_L should be asserted while power is being applied. This forces Tachyon into a known state.

Following a reset, Tachyon is in an IDLE state. The power-on value of all Tachyon internal registers is defined in “5.1 Register Overview” on page 25.

6.1.16 Arbitration

Since only two devices are present on TSI, arbitration is not that complex. If Tachyon requires control of TSI, Tachyon asserts one of the request (TBR_L[ ]) lines. TBR_L[0] indicates reads and writes using the non-prefetched channel. TBR_L[1] indicates reads using the prefetch channel, except for the following situations:

1. At the beginning of a block of prefetched data TBR_L[1] is used, even though no data has been prefetched yet.

2. At the end of a prefetched block within a sequence the next A/L pair is read via the prefetch channel, even though the actual A/L pair data is not prefetched. The prefetching channel must be able to process these cases, in addition to the normal prefetched cases.

The two TBR_L signals are mutually exclusive, i.e., the two signals are never asserted simultaneously. Each TBR_L signal is guaranteed to be de-asserted for at least one clock cycle prior to other TBR_L signal being asserted.

Regardless of the type of request signal (TBR_L[0] or TBR_L[1], the host asserts the grant line (TBG_L) to grant the bus to Tachyon. The host must assert TBG_L for a minimum of one clock cycle. Afterwards, TBG_L may be de-asserted at any time without effect. To avoid latency, the host can de-assert the grant line as soon as possible.

After the host asserts TBG_L, Tachyon begins a transaction one cycle later. Tachyon begins the transaction by asserting AVCS_L and starting the address cycle.

After Tachyon begins the transaction, it holds TBR_L[ ] asserted until at least the later of:

1. The last data cycle of the transaction

2. The cycle after READY_L or RETRY_L is asserted. The host can assert its READY_L at the conclusion of the transfer (on the cycle following the last data cycle) as a confirmation that the transfer is complete or to avoid latency, the host may elect to assert READY_L sooner.

Tachyon keeps the TBR_L signal asserted until it relinquishes its bus tenancy following its last transaction.

Tachyon stops driving all lines by the cycle when Tachyon de-asserts the TBR_L[ ] signal.

Once the host de-asserts TBG_L, it must not re-assert until after both of the TBR_L[ ] signals are de-asserted and after Tachyon asserts one of them again.

6.1.17 Interrupts

When Tachyon places an entry into the IMQ, Tachyon generates an interrupt to notify the host, except for the following conditions:

1. The host requests Tachyon not to generate an interrupt for an outbound completion message.

2. A previous entry in the IMQ has not yet been consumed by the host. In this case, Tachyon does not generate another interrupt until the IMQ Consumer Index is updated by the host.

When Tachyon generates an interrupt, the interrupt signal, INT_L, is asserted for one TSI clock cycle. INT_L is then de-asserted and remains de-asserted until Tachyon generates the next interrupt.

Interrupts may not be generated when Tachyon is the owner of TSI, i.e., INT_L is always de-asserted when either TBR_L signal is asserted.

When software services interrupts, maintain the following order:

1. Software receives interrupt.

2. Software reads IMQ entry(ies).

3. Software re-enables the hardware interrupts (e.g. resets a latch which detects Tachyon interrupts).

4. Software updates IMQ Consumer Index, which re-enables interrupts within Tachyon.

WARNING	If Step 4 is performed before Step 3 above, a race condition occurs and a subsequent interrupt may be missed.

If the host software decides not to consume all IMQ entries before updating the IMQ Consumer Index, Tachyon immediately issues another interrupt to ensure that messages are not left on the IMQ. The normal mode of operation is to read all entries on the IMQ before updating the IMQ Consumer Index.

6.1.18 Host Interface Design Notes

Arbitration

1. Host transactions may begin one delay cycle after Tachyon de-asserts TBR_L[ ].

2. Tachyon may de-assert TBR_L[ ] for as little as one cycle, then re-arbitrate if TBG_L is de-asserted.

3. If the host asserts TBG_L when Tachyon is asserting TBR_L[ ], Tachyon starts a transaction. Give a grant no sooner than one cycle before the host is finished with its transaction (for reads, at the start of the recovery cycle; for writes, in the last data cycle or the cycle after READY_L is asserted, whichever is later).

4. Do not anticipate the number of cycles from TBG_L that Tachyon asserts AVCS_L; wait for it.

5. Do not anticipate the number of cycles after READY_L that Tachyon de-asserts TBR_L[ ].

6. Tachyon bus tenancy can span up to 64 transactions. Individual applications can limit this number by programmable configuration.

Host-Mastered Transactions

1. Do not anticipate the number of cycles Tachyon takes to assert READY_L.

2. Tachyon checks parity on all 32 TAD[ ] signals during address cycles.

3. The responder may assert READY_L the cycle after Address for Writes.

4. A host-mastered transaction with address or TYPE error does not complete with READY_L.

Tachyon-Mastered Reads

1. Check PREFETCH_L in the Address cycle (optional).

2. Note the short time between streamed Reads.

3. The host may assert RETRY_L only during Reads. This forces Tachyon to terminate its tenancy.

4. Tachyon reads a prefetched address during the next transaction that it asserts TBR_L[1].

Tachyon-Mastered Writes

1. Responder may assert READY_L before the last data cycle.

2. Note the short time between streamed Writes.

3. There is no mechanism to stop a Write stream, unless the host asserts RESET_L. Withholding READY_L only suspends the Write stream.

6.2 TSI Functional Waveforms

TSI Functional Waveform Signal Notes

- De-assertion of the TBR_L[ ] signal by Tachyon at the end of a transaction is determined by which internal Tachyon module is accessing the bus and the current state of streaming.

- The re-assertion delay of TBR_L[ ] depends on the state of TBG_L when TBR_L[ ] is de-asserted and other transactions that are queued in Tachyon.

- Transactions can start (assertion of AVCS_L) no sooner than one clock cycle after the de-assertion of the TBG_L signal.

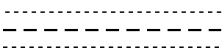
- When the host or Tachyon drives either AVCS_L or READY_L; it asserts (driving low) the signal for one clock cycle, actively de-asserts (driving high) the signal for one cycle, and then tri-states the signal.

- The host interface must not attempt to drive either AVCS_L or READY_L when Tachyon is driving these signals either high or low.

- To meet timing parameters, it is recommended that the host actively de-assert AVCS_L and READY_L after driving them. All waveforms in this document show the host behaving in this manner.

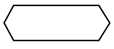
TSI Functional Waveform Graphic Notes

- A tri-stated (high-impedance) signal is indicated by a dashed line between high and low.

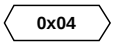


- An undefined signal, e.g., wait states, is indicated by a shaded area.

- A parity signal is indicated by a white boxed area.



- A valid bus value is indicated in boxed areas.



Note The following TSI waveform examples depict realistic possibilities for Tachyon Revision 2, however, the waveform examples do not reflect the exact timing of every possible transaction, nor for every possible version of Tachyon.

Note The following TSI functional waveform examples are meant to show functionality and are not intended to show any timing information. For timing information, refer to “6.3 TSI Timing Requirements” on page 92.

6.2.1 Slave Reads and Writes

In these examples of Slave Reads and Writes, the host asserts three host-mastered, or slave, transactions, a slave WRITE1, a slave READ1, and an illegal slave READ4, shown in the following three figures.

During slave Write or Read transactions, only single word transactions are allowed. If the host requests a slave transaction of other than one word, Tachyon asserts ERROR_L.

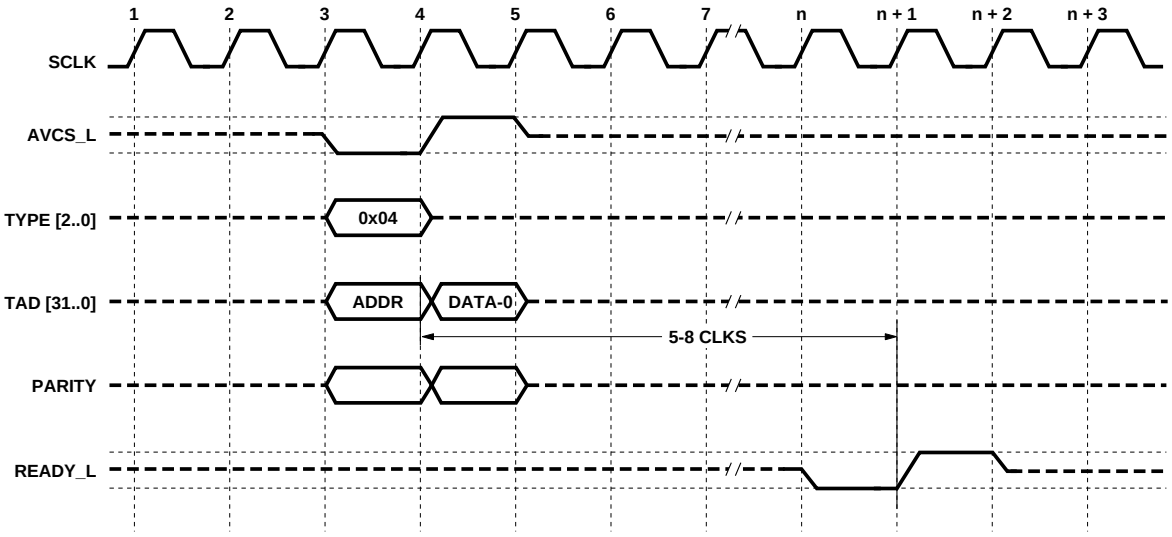


Figure 6.1 Slave WRITE1.

This is a slave WRITE1 transaction, indicated by Type [2..0] = 0x04. The host initiates the transaction by strobing AVCS_L and driving the TYPE [2..0], TAD [31..0], and PARITY signals. The following clock cycle is the data cycle (DATA-0), with no wait states possible. Tachyon then ends the transaction by asserting READY_L as an acknowledgment.

The delay from the sampling of AVCS_L to the assertion of READY_L for a Write depends on which register is being written and the Fibre Channel speed selected. For Writes of non-Frame Manager registers, the delay is five clock cycles. If the fastest TSI clock (40 MHz) and the slowest Fibre Channel speed (266 MBaud) is selected, then the delay is between five and eight clock cycles.

Design should depend on the host waiting for the assertion of READY_L, rather than waiting for a specific number of clock cycles to occur. This ensures compatibility with future revisions of Tachyon.

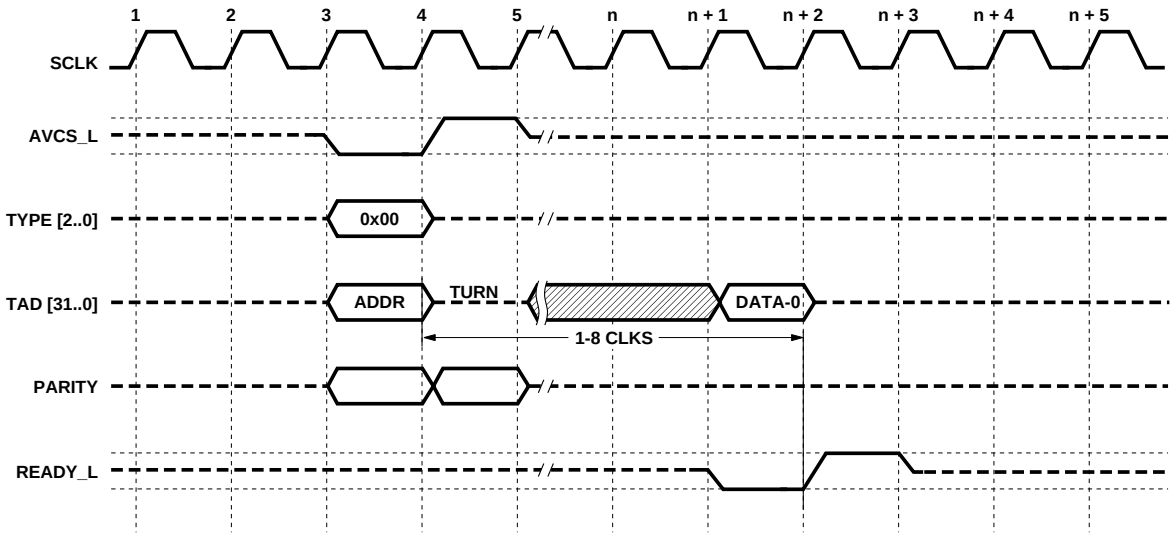


Figure 6.2 Slave READ1.

This is a Slave READ1 transaction, indicated by TYPE [2..0] = 0x00. Following the assertion of AVCS_L on any Read transaction, the next clock cycle is defined as a “turn” cycle. A turn cycle gives a finite period of time for the initiator of the transaction to stop driving the address on TAD [31..0] before the responder begins driving data on TAD [31..0]. After the turn cycle, Tachyon generates wait states before the data cycle (DATA-0) begins.

The delay from the sampling of AVCS_L to the assertion of READY_L for a Read depends on which register is being read and the Fibre Channel speed selected. For Reads of non-Frame Manager registers, the delay is one clock cycle. For Frame Manager registers, the delay is between one and eight clock cycles. If the fastest TSI clock (40 MHz) and the slowest Fibre Channel speed (266 MBaud) is selected, then the delay is between one and eight clock cycles.

Note Parity is only depicted in these first two waveform examples, but may be used for all DMA transactions.

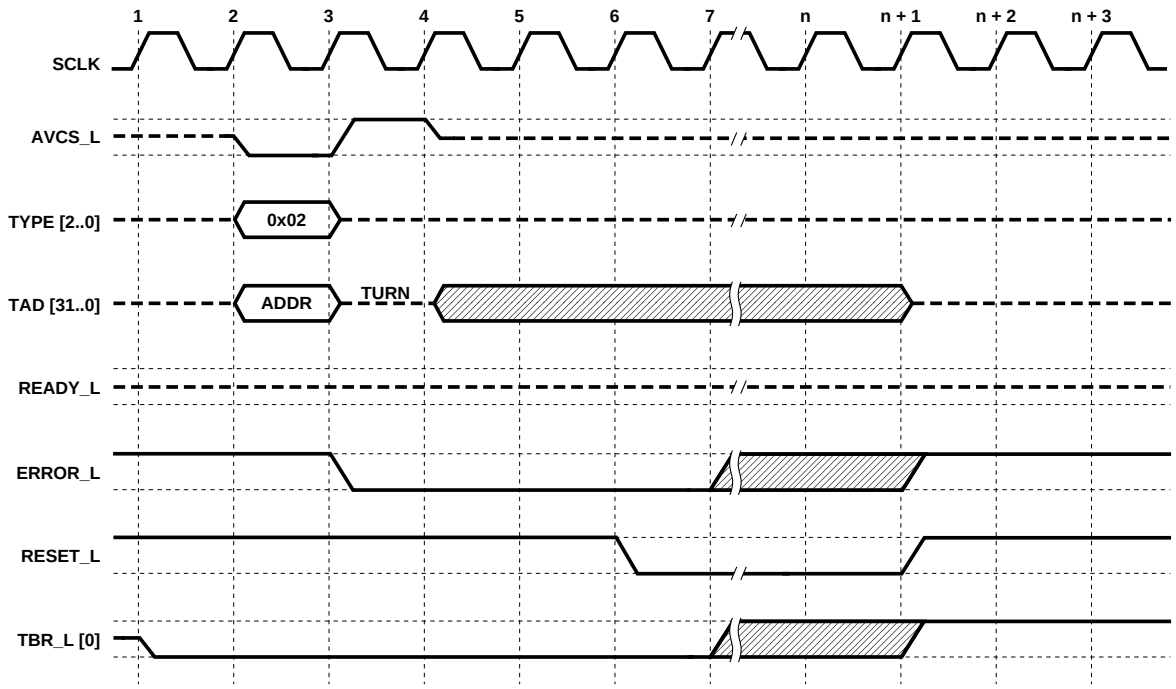


Figure 6.3 RESET_L of an Illegal Slave READ4.

This third slave transaction demonstrates the effect of performing a slave transaction of other than one word. The host initiates an illegal slave READ4 (four words) transaction causing Tachyon to assert ERROR_L.

The host resets Tachyon by asserting RESET_L. RESET_L must remain asserted for a minimum of ten clock cycles. When the host resets Tachyon, asserted signals are released before the end of the RESET_L assertion. In this case, the asserted signals, ERROR_L, TBR_L [0], and TAD[31..0] are released.

TBR_L [0] is completely independent of the slave transaction. However, if it is asserted prior to an illegal slave transaction, it remains asserted while ERROR_L is asserted, until the reset of Tachyon occurs.

6.2.2 DMA Writes

In this example of a DMA Write, Tachyon has 28 bytes of data to write to host memory. Tachyon writes this data with a series of three transactions; a WRITE4 a WRITE2, and a WRITE1, shown in the following three figures.

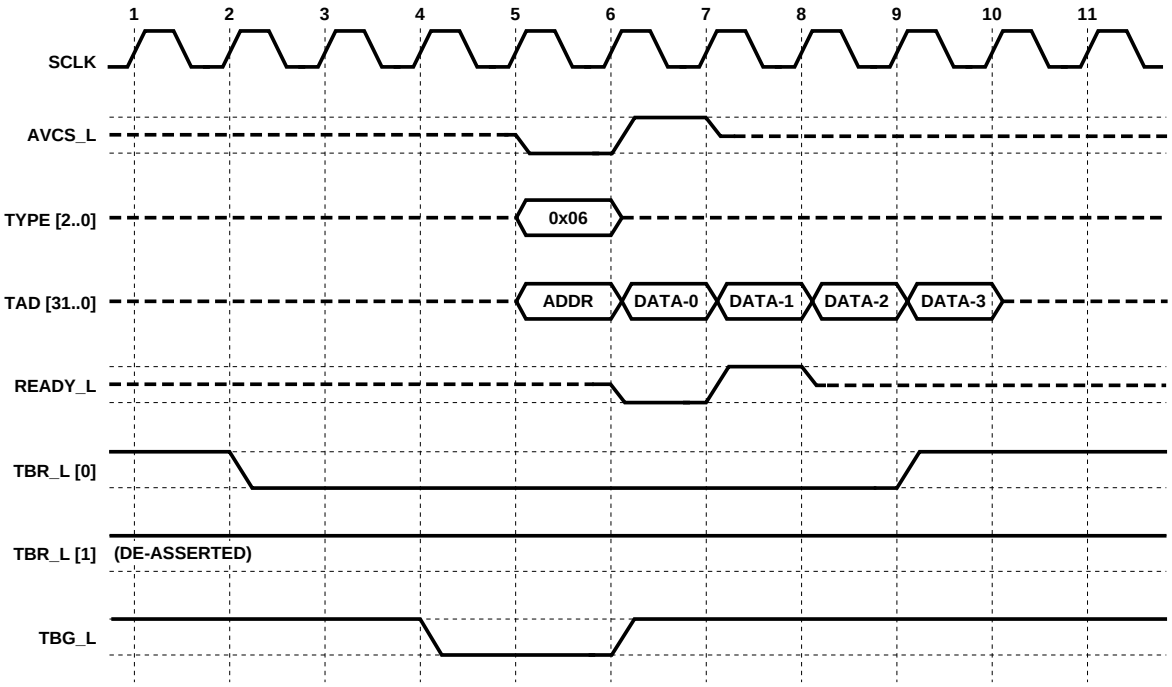


Figure 6.4 DMA Write, WRITE4 Transaction.

This is a WRITE4 transaction indicated by TYPE [2..0] = 0x06.

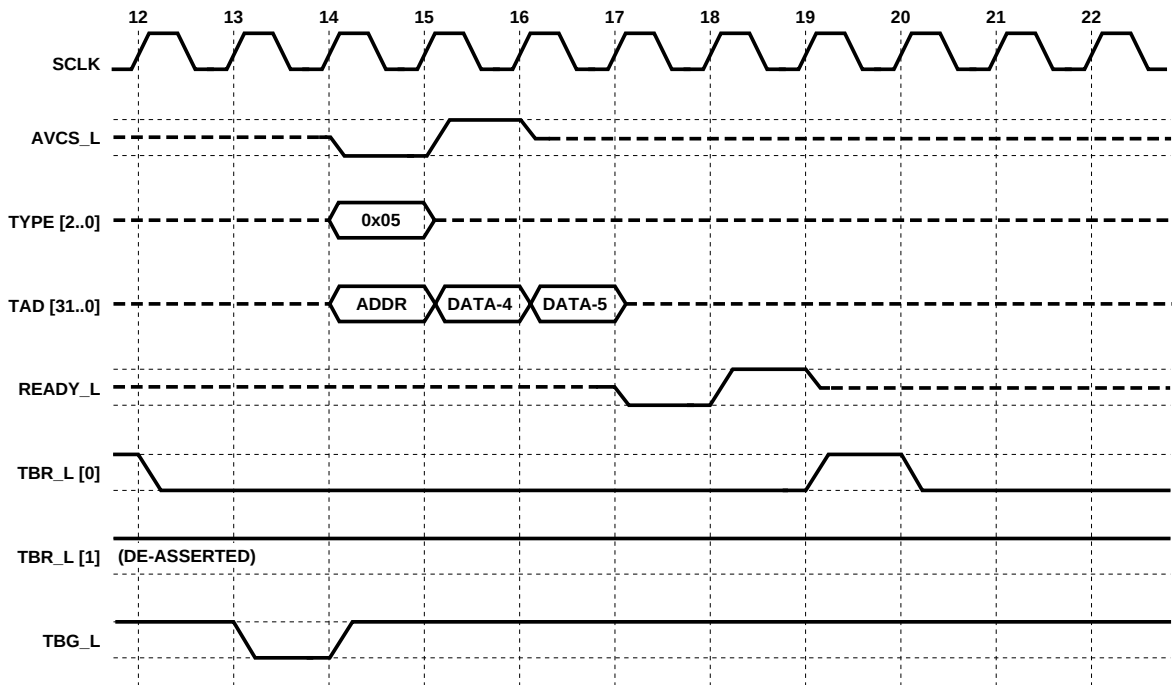


Figure 6.5 DMA Write, WRITE2 Transaction.

This is a WRITE2 transaction indicated by TYPE [2..0] = 0x05.

Since TBG_L is already de-asserted when TBR_L[0] is de-asserted, Tachyon can assert TBR_L [0] again without waiting.

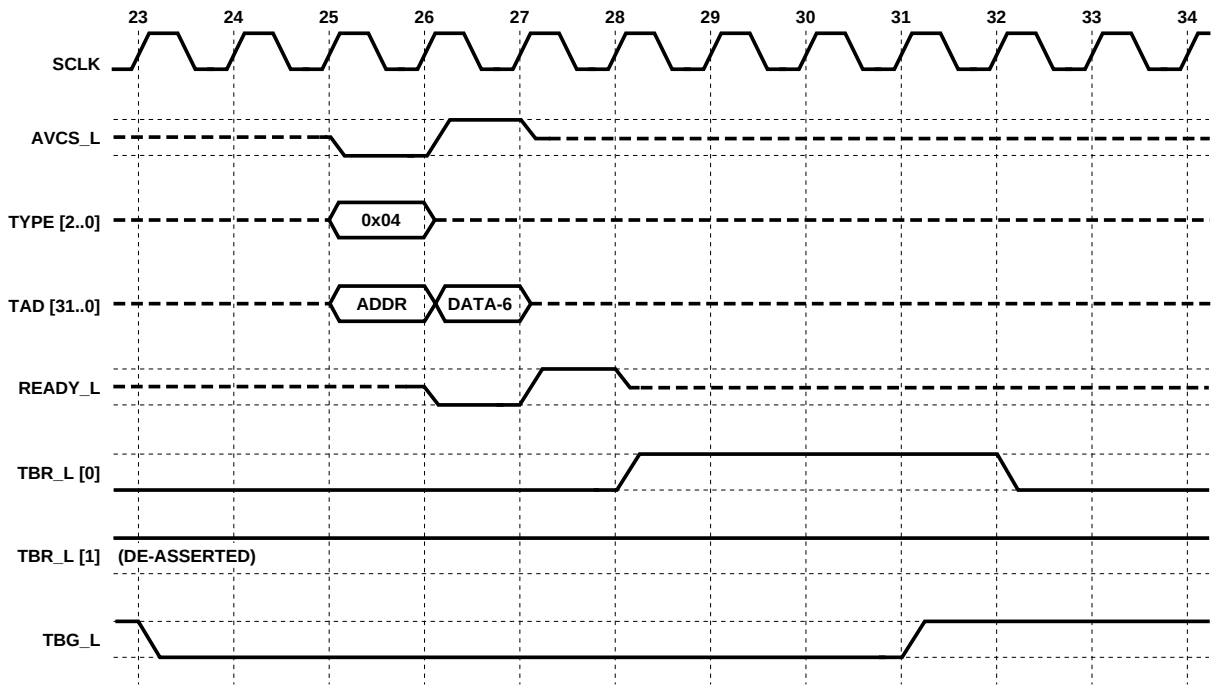


Figure 6.6 DMA Write, WRITE1 Transaction.

In this example, the de-assertion of TBG_L is delayed and Tachyon cannot arbitrate for the next bus tenancy (assert TBR_L[0]) until TBG_L is de-asserted.

6.2.3 DMA Write Streaming

When streaming, i.e., performing multiple transactions per bus tenancy, a new transaction cannot begin until two clock cycles after the last data cycle has finished and READY_L has been asserted.

In this example of a DMA Write Stream, Tachyon has 28 bytes of data to write to host memory. Tachyon writes this data with a series of three write transactions; a WRITE4, a WRITE2, and a WRITE1 shown in the following two figures.

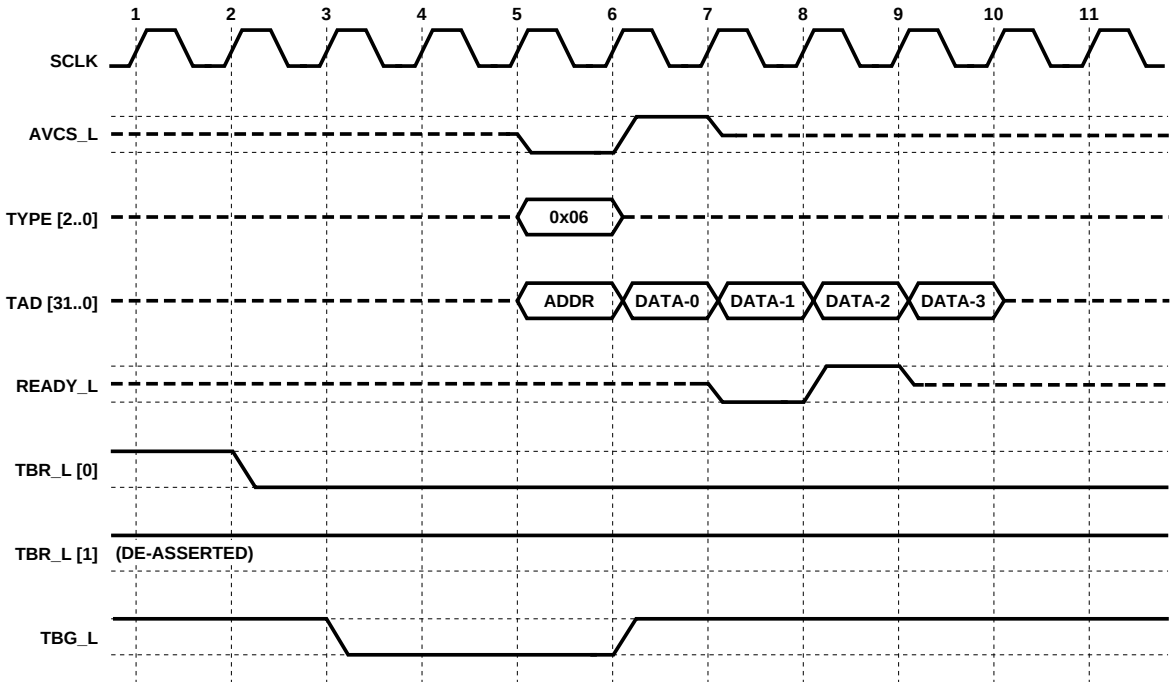


Figure 6.7 DMA Write Stream, WRITE4 Transaction.

In the figure above, READY_L is asserted during the data cycles of the first transaction (WRITE4), therefore, the second transaction (WRITE2) can begin two cycles after the last data cycle of the first transaction. Refer to “Figure 6.8 DMA Write Stream, WRITE2 and WRITE1 Transactions” on page 75.

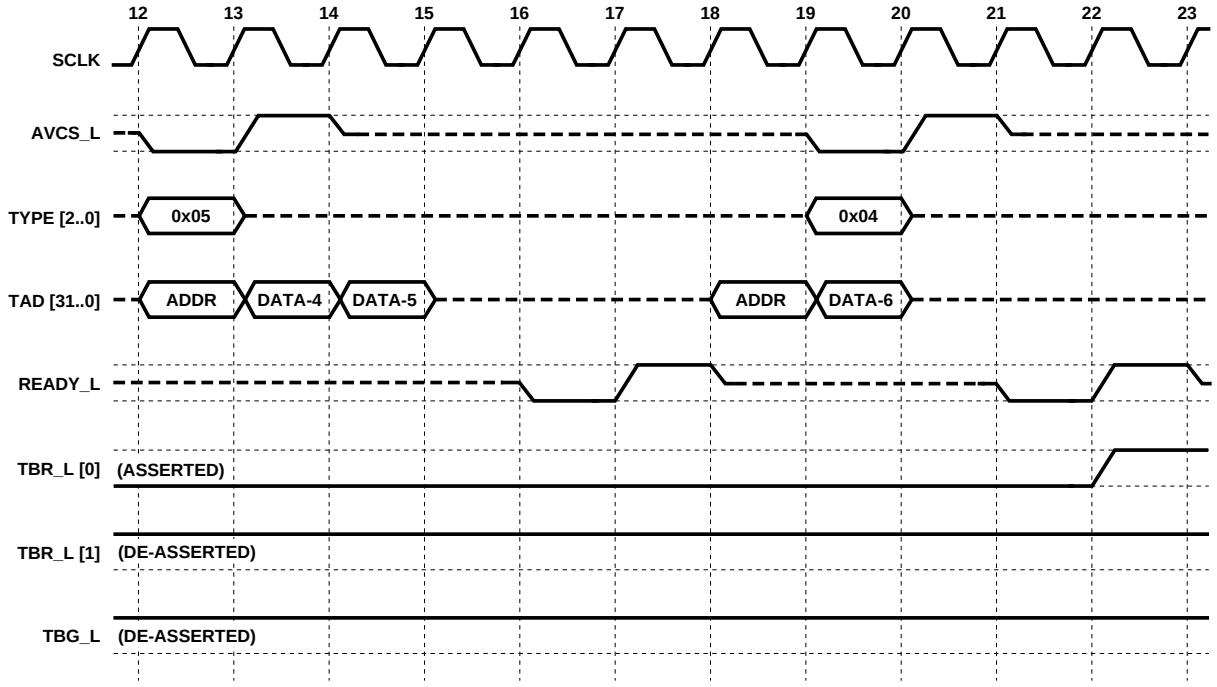


Figure 6.8 DMA Write Stream, WRITE2 and WRITE1 Transactions.

This figure shows the second (WRITE2) and third (WRITE1) transactions of the DMA Write Stream.

The third transaction cannot occur two cycles after the last data cycle of the second transaction because it must wait until the host asserts READY_L.

After the host asserts READY_L, Tachyon ends the bus tenancy by de-asserting TBR_L[0].

6.2.4 DMA Reads

In this example, two of the four DMA read transactions, a READ2 and a READ4, are shown in the following two figures.

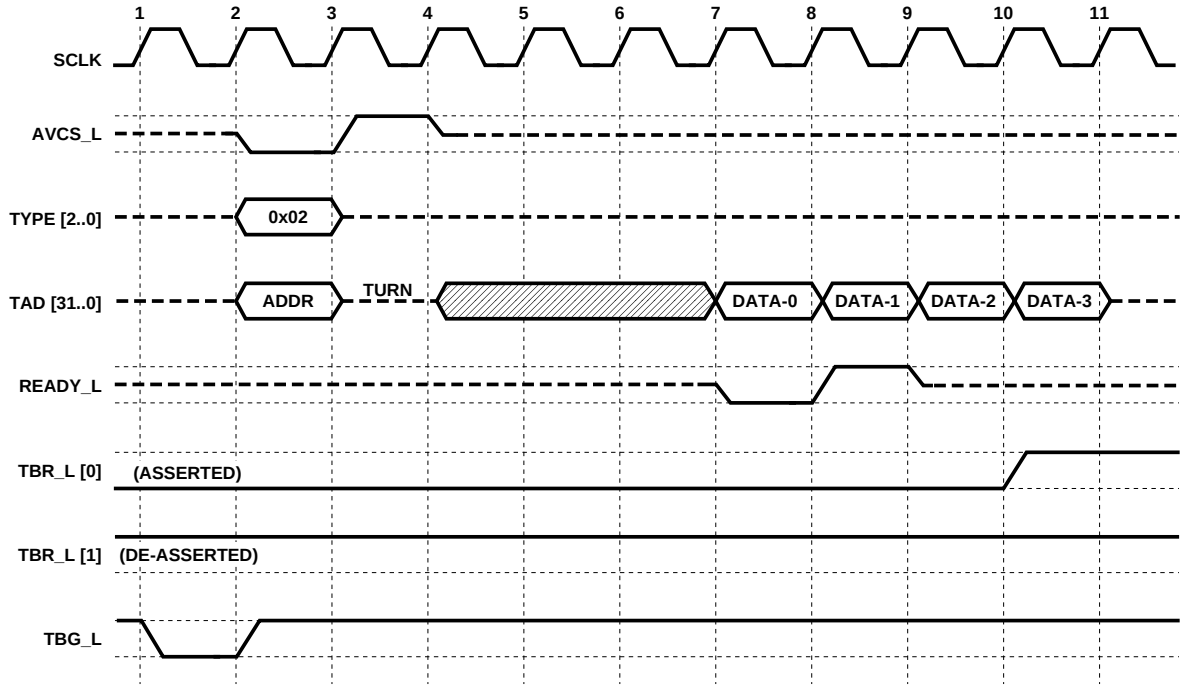


Figure 6.9 DMA Reads, READ4 Transaction.

The bus request signal (TBR_L[0] in this example) is de-asserted just before the last data cycle.

If streaming is enabled, the de-assertion of TBR_L may occur just before the last data cycle or up to four cycles after that.

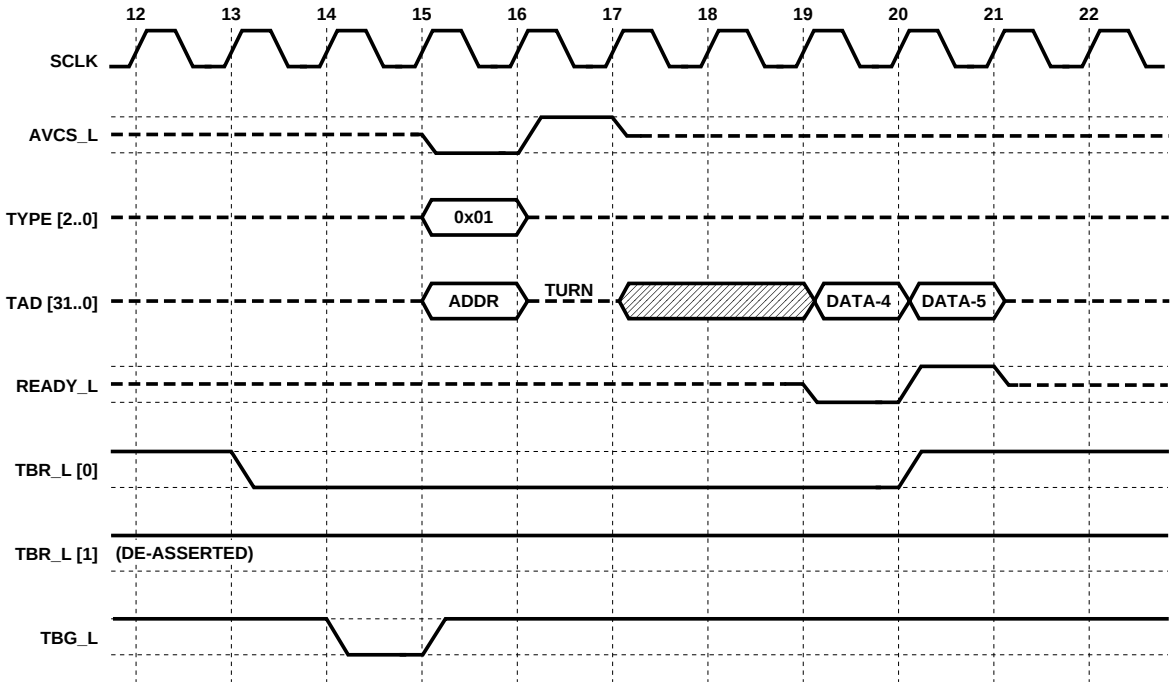


Figure 6.10 DMA Reads, READ2 Transaction.

The above figure shows a READ2 transaction indicated by TYPE [2..0] = 0x01.

6.2.5 DMA Read Prefetching

In this example, the basic behavior of prefetch-indication is depicted in the following two transactions. READ8 at ADDR-1 and READ8 at ADDR-2, shown in the following two figures.

In this example, streaming is not enabled.

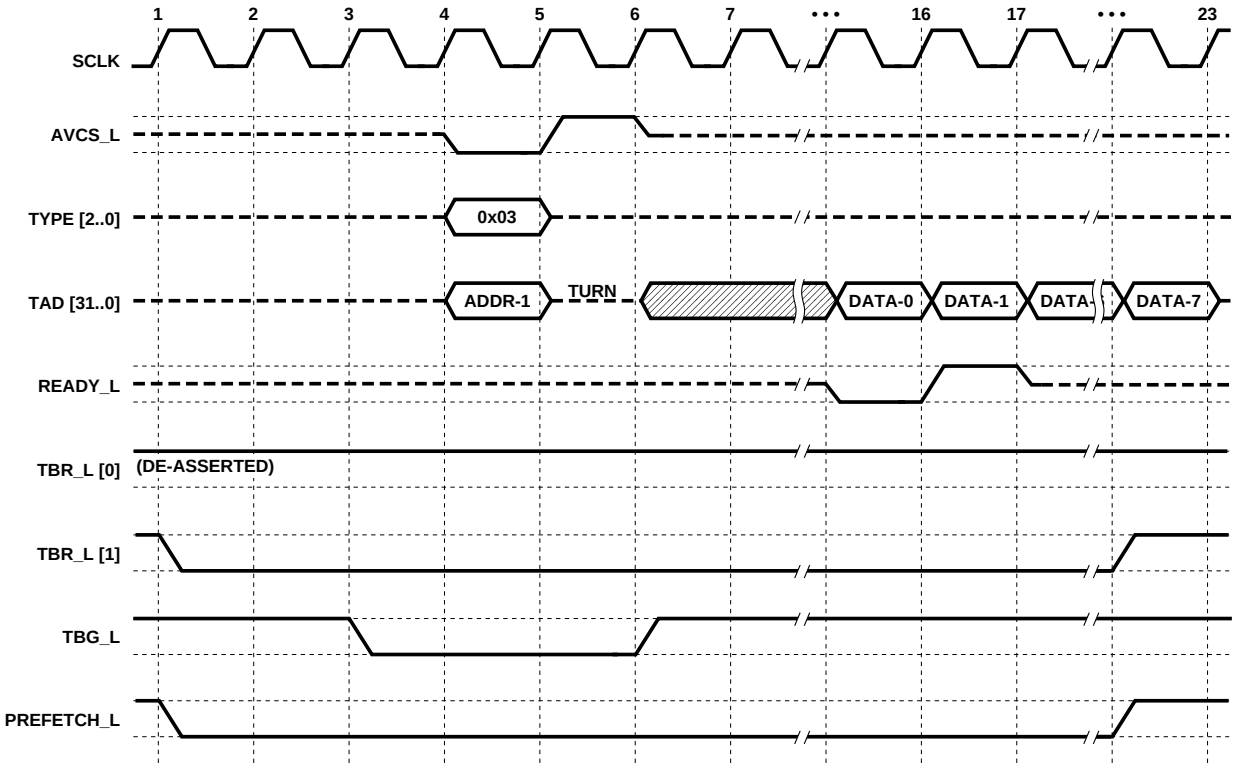


Figure 6.11 DMA Read Prefetching, READ8 at ADDR-1.

The READ8 at address ADDR-1 is the first transaction of a block of 64 bytes that is read from contiguous locations. As the bus is requested for this transaction, PREFETCH_L is also asserted, indicating that the next Read on this channel is sequential to the current 32 bytes. A large number of wait states are needed, due to the latency of the host memory, in this example.

As the host interface retrieves the Read data for the first transaction memory, it may want to act upon the prefetch-indication that is given during the first transaction and valid during the address cycle. If the host wants to act upon the prefetch-indication, it should retrieve and buffer the next 32 bytes sequential to the first transaction's data, since it is guaranteed that Tachyon requests this data on the next TBR_L [1] bus tenancy.

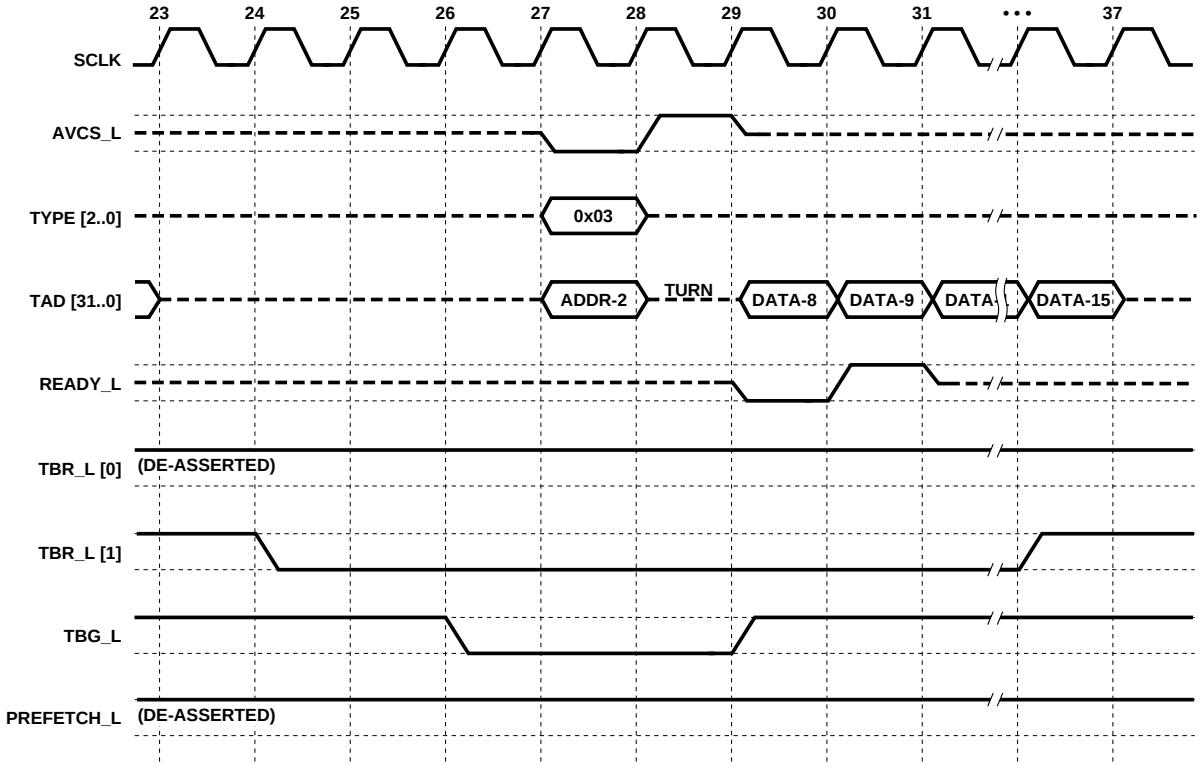


Figure 6.12 DMA Read Prefetching, READ8 at ADDR-2.

When the second transaction has started, the host interface has already successfully prefetched the next block of 32 bytes, so the data cycles for the second transaction may start as soon as one cycle after the address cycle, as shown above. A turn cycle is always required immediately following the address cycle in any Read transaction.

In this example, ADDR-2 = ADDR-1 + 32 bytes.

6.2.6 DMA Read Channels

When outbound data (headers and EDBs) are DMAed from host memory, Tachyon always requests the host bus using the prefetch read channel, TBR_L[1]. For all other data that is read from host memory, such as ODBs or inbound buffer blocks, Tachyon requests the host bus using the non-prefetch read channel, TBR_L[0].

This example shows the interaction between the two different read channels, TBR_L[0] and TBR_L[1], using the following transactions:

1. A READ8 at address ADDR-1 using the prefetch channel.

2. A non-contiguous READ8 at address ADDR-X using a non-prefetch channel.

3. A final READ8 at address ADDR-2 using the prefetch channel, where ADDR-2 = ADDR-1 + 32 bytes.

These transactions are shown in the following three figures.

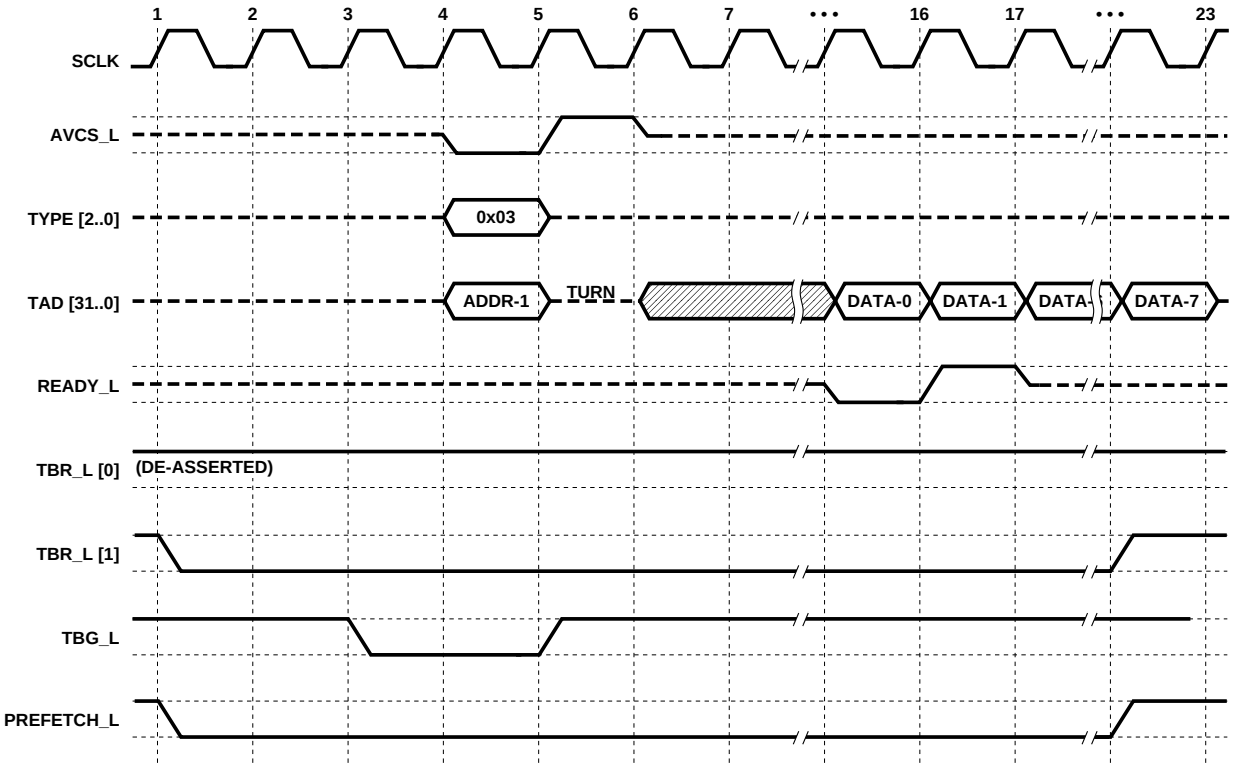


Figure 6.13 DMA Read Channels, READ8 at ADDR-1.

This is a READ8 transaction at ADDR-1, using the prefetch channel, TBR_L [1].

As in the previous example, prefetching is indicated during the first transaction, so the next transaction on the TBR_L[1] channel (the READ8 at ADDR-2) is a Read to an address sequential to the current read data.

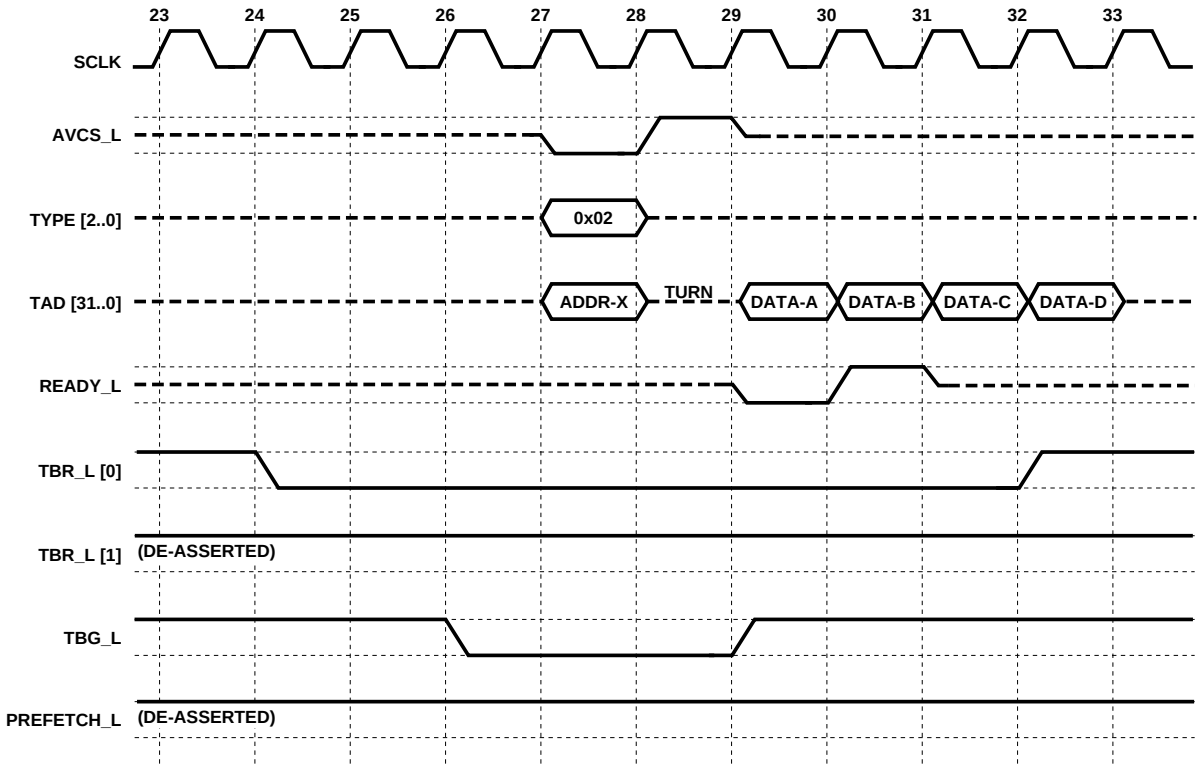


Figure 6.14 DMA Read Channels, READ8 at ADDR-X.

The second transaction (a READ8 at ADDR-X) is non-sequential to the first and is read using the non-prefetched channel, TBR_L[0].

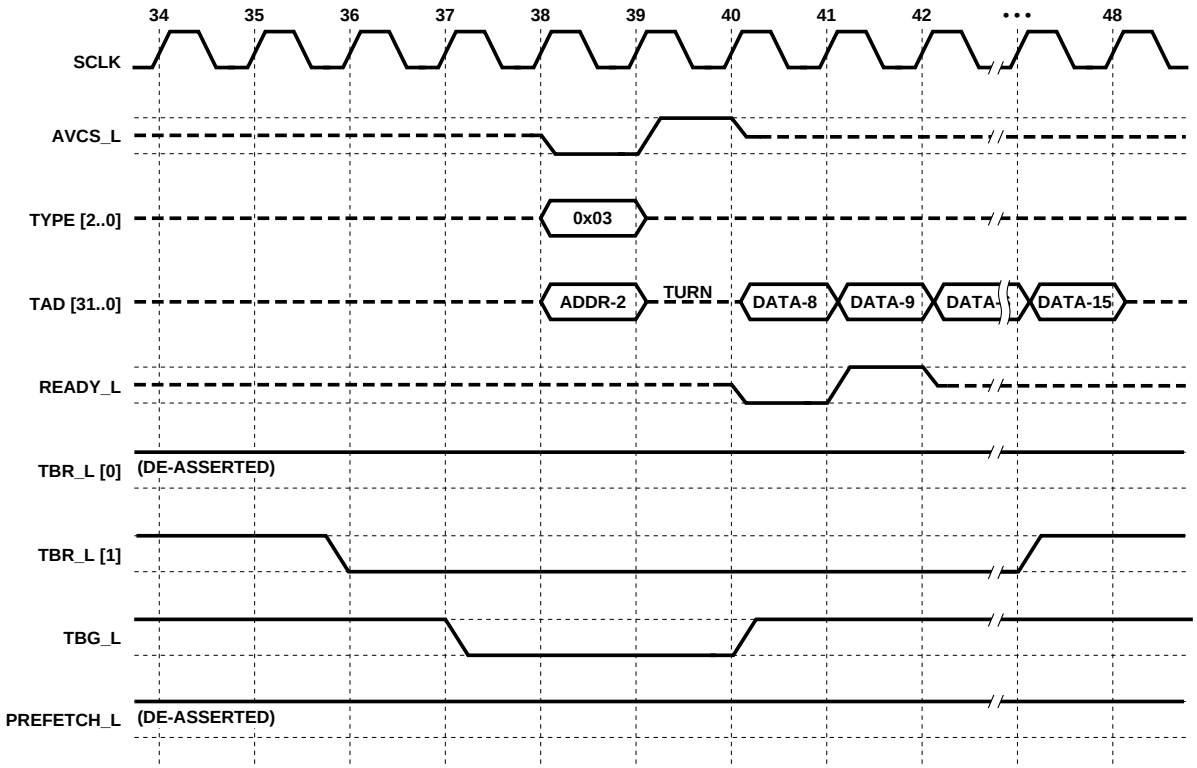


Figure 6.15 DMA Read Channels, READ8 at ADDR-2.

Like the first READ8 transaction, the third READ8 transaction uses the prefetch read channel, TBR_L[1].

Because this transaction was prefetch-indicated during the first transaction, the data was buffered on the host interface and is readily available when requested. Also, because this was the last of the 64-byte block to read, PREFETCH_L is not asserted during the address cycle of the third transaction.

In this example, ADDR-2 = ADDR-1 + 32 bytes.

6.2.7 Streamed Block Reads

In this example, Tachyon reads a block of 96 bytes from host memory. Tachyon reads this block in three 32-byte transactions; READ8 at ADDR-1, READ8 at ADDR-2, and READ8 at ADDR-3 shown in the following three figures.

Tachyon has been configured to allow at least four Read transactions per bus tenancy, and therefore, can stream the first block of data, i.e., Tachyon can read all 96 bytes in one bus tenancy.

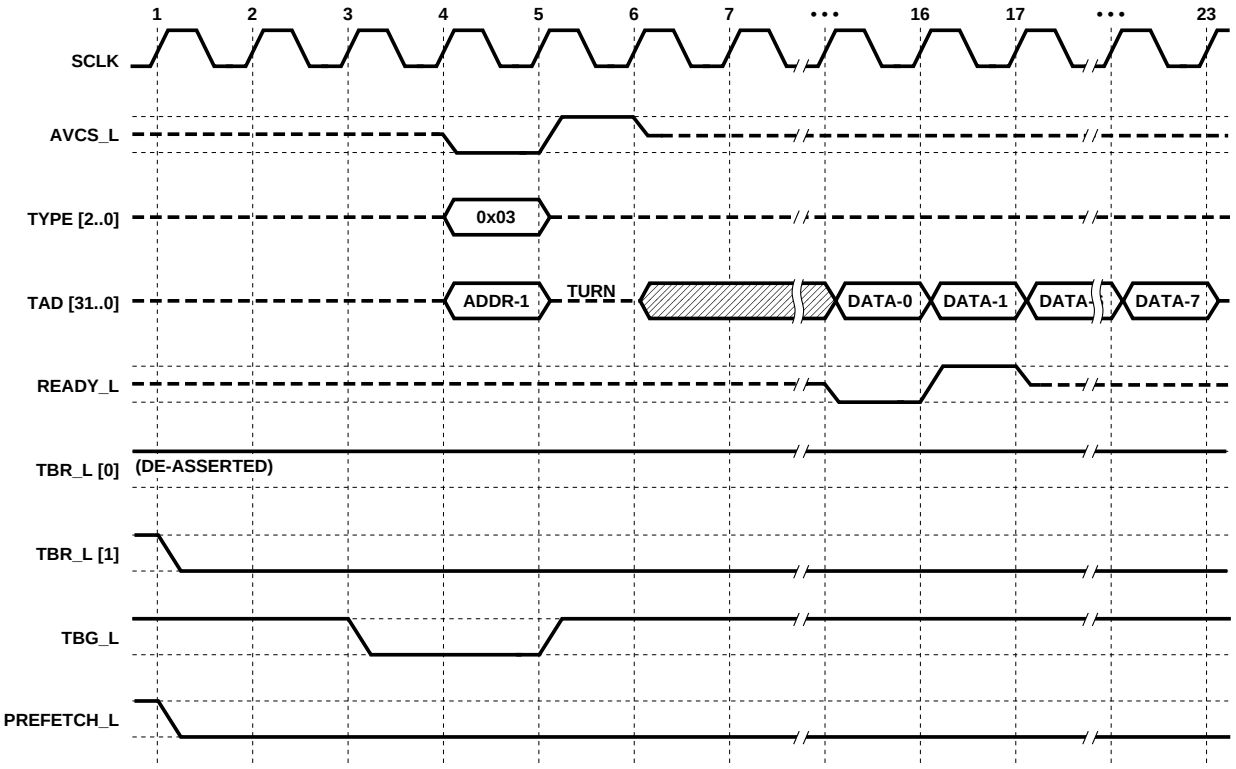


Figure 6.16 Streamed Block Read, READ8 at ADDR-1.

Address ADDR-1 incurs a large number of wait states due to latency of the host memory.

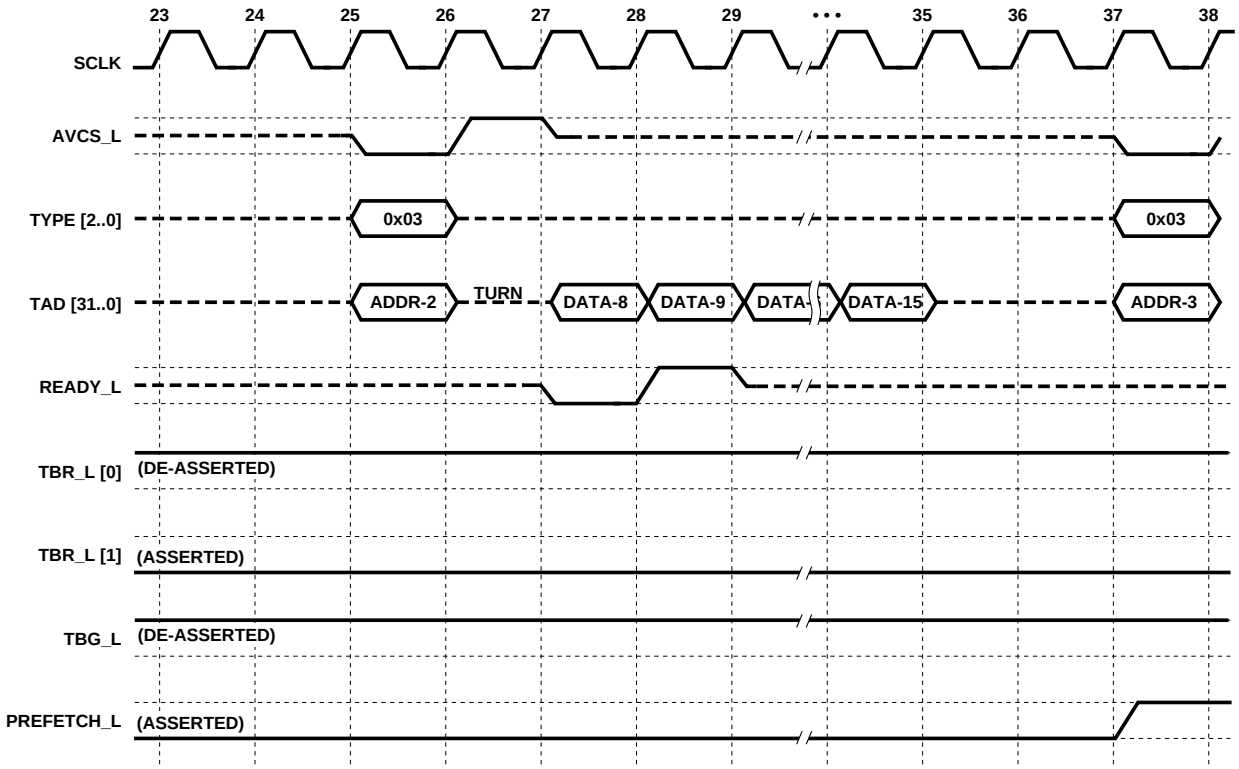


Figure 6.17 Streamed Block Read, READ8 at ADDR-2 and ADDR-3.

Since PREFETCH_L is sampled during the address phase of the first transaction (ADDR-1), the data associated with address ADDR-2 can be prefetched and ADDR-2 does not incur many wait states while the read data returns.

The data associated with address ADDR-3 can also be prefetched, since PREFETCH_L is sampled during the address phase of the first transaction (ADDR-1). ADDR-3 does not incur many wait states while the read data returns. However, since the ADDR-3 transaction represents the last data in this block, PREFETCH_L is de-asserted prior to the address phase of the third transaction.

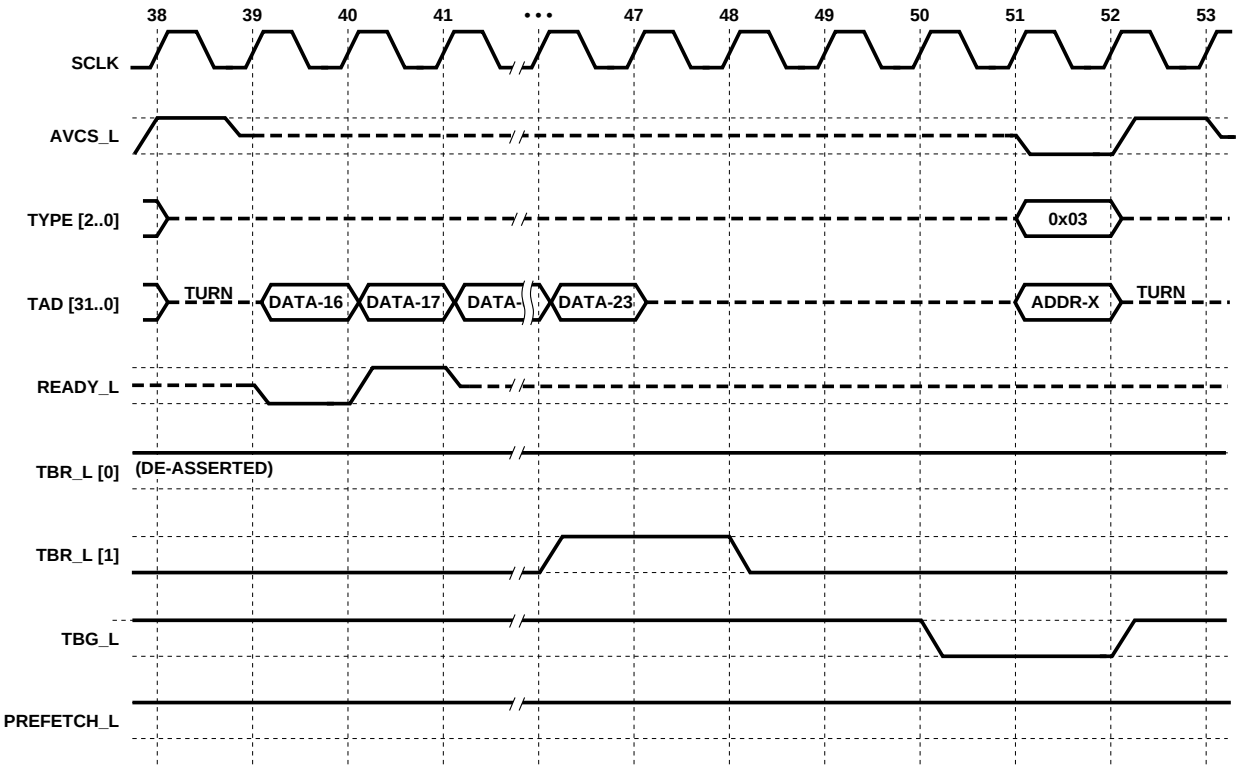


Figure 6.18 Streamed Block Read, READ8 at ADDR-3 and ADDR-X.

On the last data cycle of the third transaction (ADDR-3), Tachyon ends the bus tenancy by de-asserting TBR_L[1].

Tachyon always begins a new bus tenancy when starting on a new block of data as shown here starting at address ADDR-X.

ADDR-X does not equal ADDR-3 + 32 bytes.

6.2.8 Prefetching Across Back-To-Back Read Streams

In this example, Tachyon reads a block of data from memory with streaming on and prefetching active, similar to the previous example. The Back-to-Back Stream is depicted in the following transactions, READ8 at ADDR-1, READ8 at ADDR-2, READ8 at ADDR-3, shown in the following three figures.

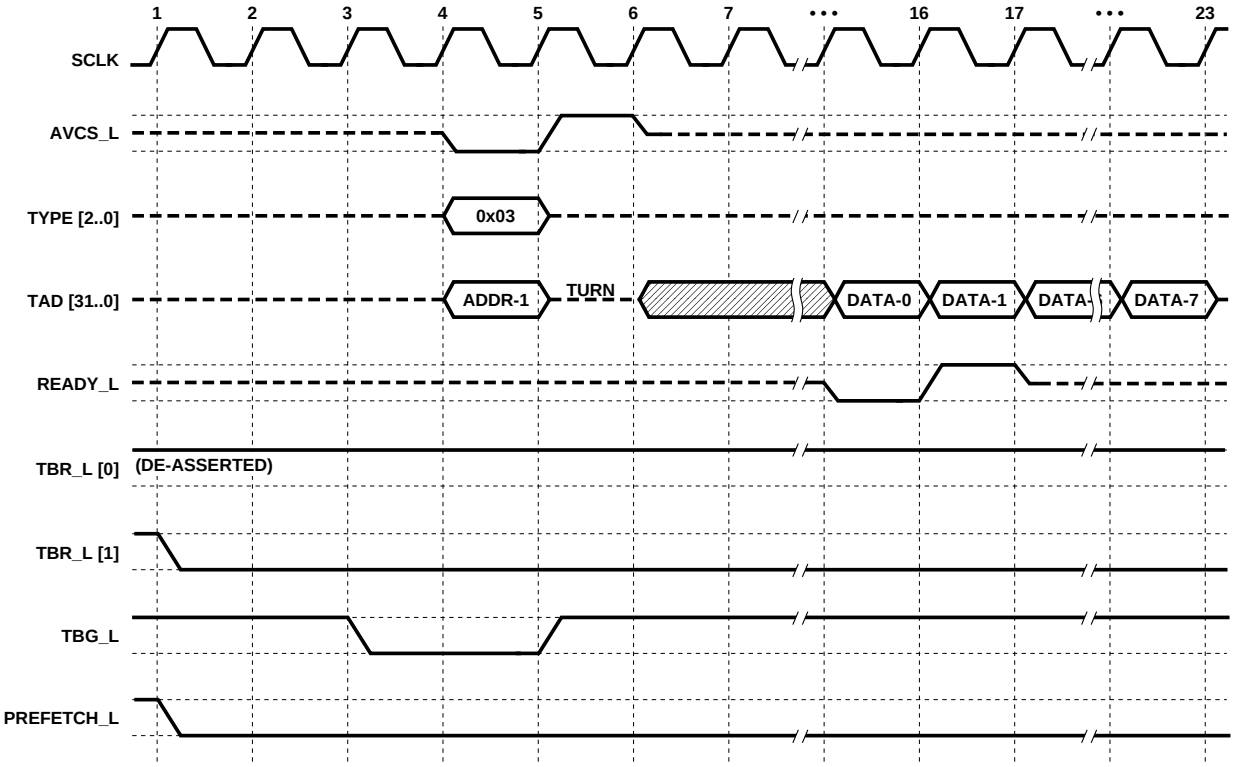


Figure 6.19 Prefetching Across Back-to-Back Read Stream, ADDR-1.

Address ADDR-1 incurs a large number of wait states due to latency of the host memory.

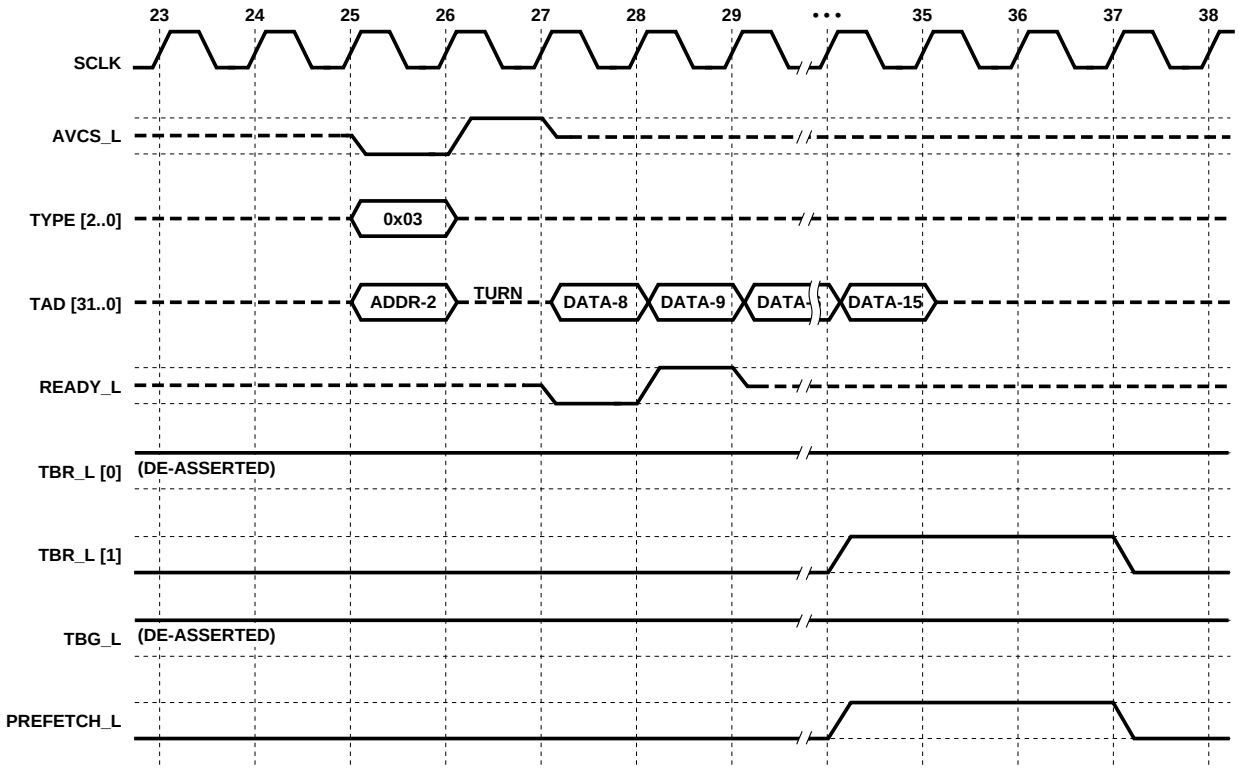


Figure 6.20 Prefetching Across Back-to-Back Read Stream, ADDR-2.

Since PREFETCH_L is sampled before the address phase of the first transaction, the data associated with address ADDR-2 can be prefetched, therefore ADDR-2 does not incur many wait states while the read data returns.

In this example, tenancy is not lost and Tachyon knows that it has more sequential Reads to follow, so it gives a prefetch-indication with ADDR-2, even though it is going to lose tenancy.

PREFETCH_L and TBR_L[1] are de-asserted just before the last data cycle of the ADDR-2 transaction. Then, Tachyon immediately requests the bus again. ADDR-3 is the next sequential address, the subject of the prefetch-indication of the second transaction.

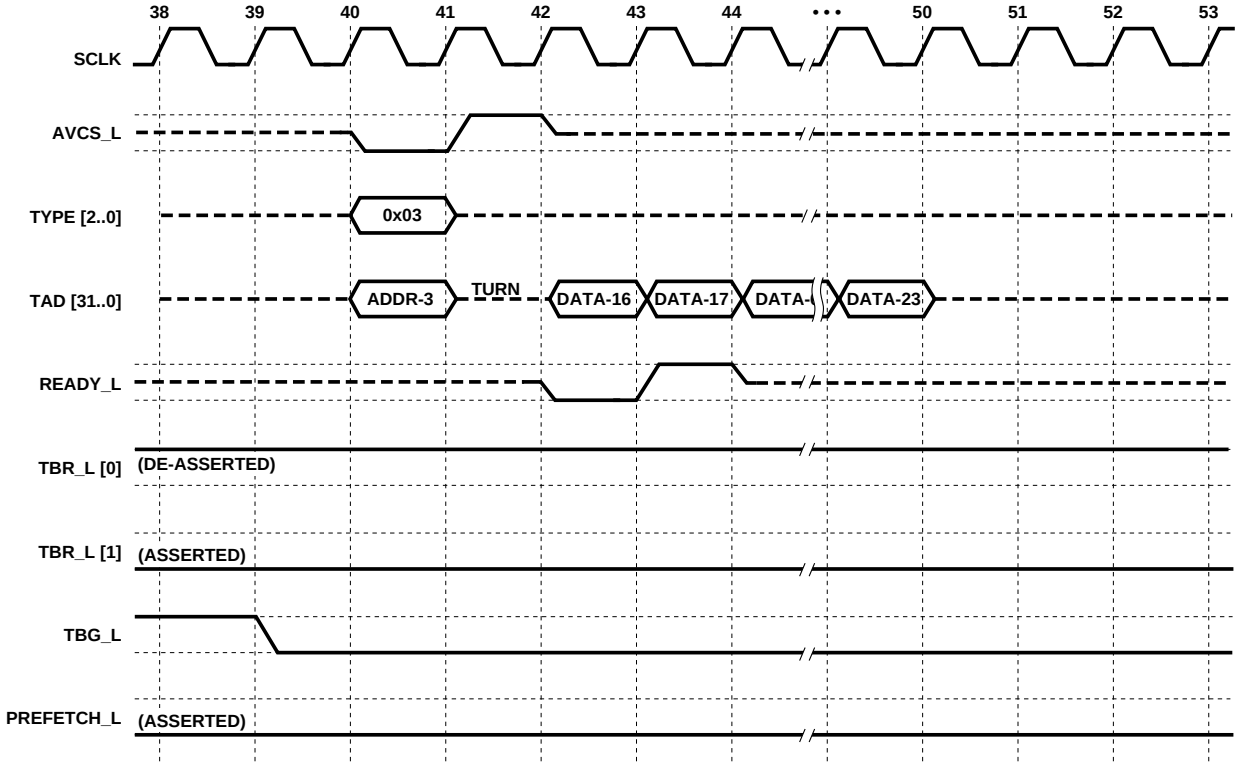


Figure 6.21 Prefetching Across Back-to-Back Read Stream, ADDR-3.

The data associated with address ADDR-3 can be returned quickly because of its prefetch-indication in ADDR-2. Since the ADDR-3 transaction is the continuation of sequential accesses, PREFETCH_L is asserted for this transaction.

6.2.9 Retried Read Transaction

In this example, Tachyon retries a READ8 transaction. This is shown in the following two figures.

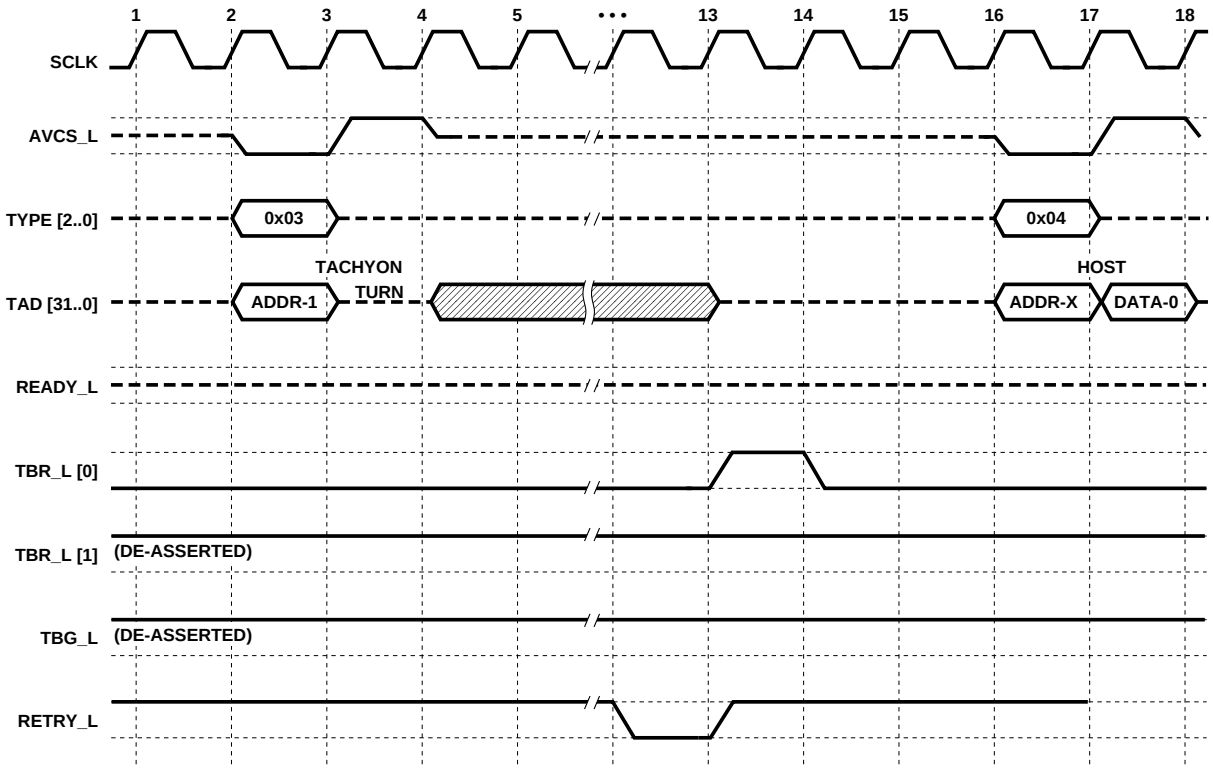


Figure 6.22 Retried Read Transaction, READ8 at ADDR-1 Attempted.

When Tachyon requests the bus and attempts to perform a Read transaction at address ADDR-1, the host determines that it does not want to service the Read transaction at this time. As such, the host asserts RETRY_L, which instructs Tachyon to terminate both the transaction and the bus tenancy. Tachyon de-asserts the bus request line, but then immediately re-asserts it to retry the Read transaction.

The second transaction is a slave Write (WRITE1) to Tachyon, which, in this example, may have been deadlocked with the first transaction, which forces the retry.

Note If Tachyon asserts the PREFETCH_L signal concurrently with the TBR_L[1] signal and the host then decides to retry the read transaction using the RETRY_L signal, then the PREFETCH_L signal will remain asserted even after Tachyon has given up the bus.

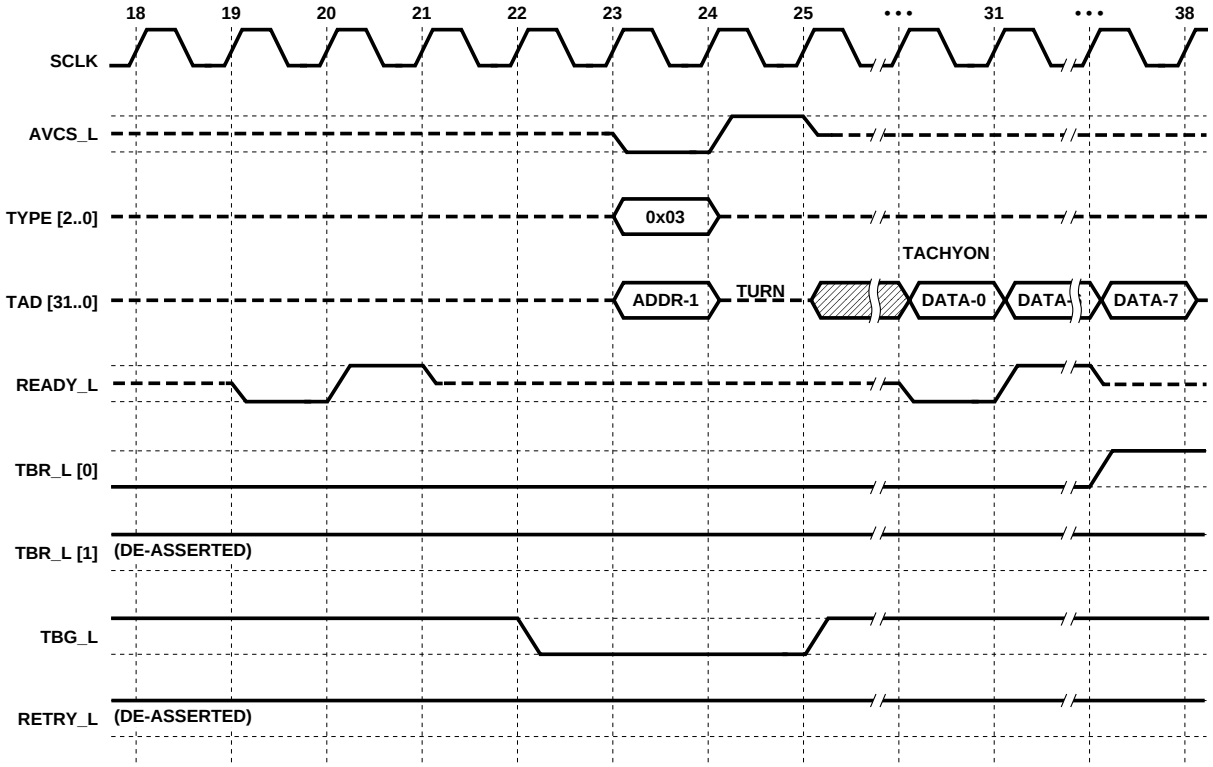


Figure 6.23 Retried Read Transaction, READ8 at ADDR-1 Retried.

When the host grants Tachyon the bus again, Tachyon immediately attempts the Retried Read transaction at the same address, ADDR-1. No other Tachyon-mastered transaction may occur until the Retried Read transaction is completed.

6.2.10 Interrupt Signal

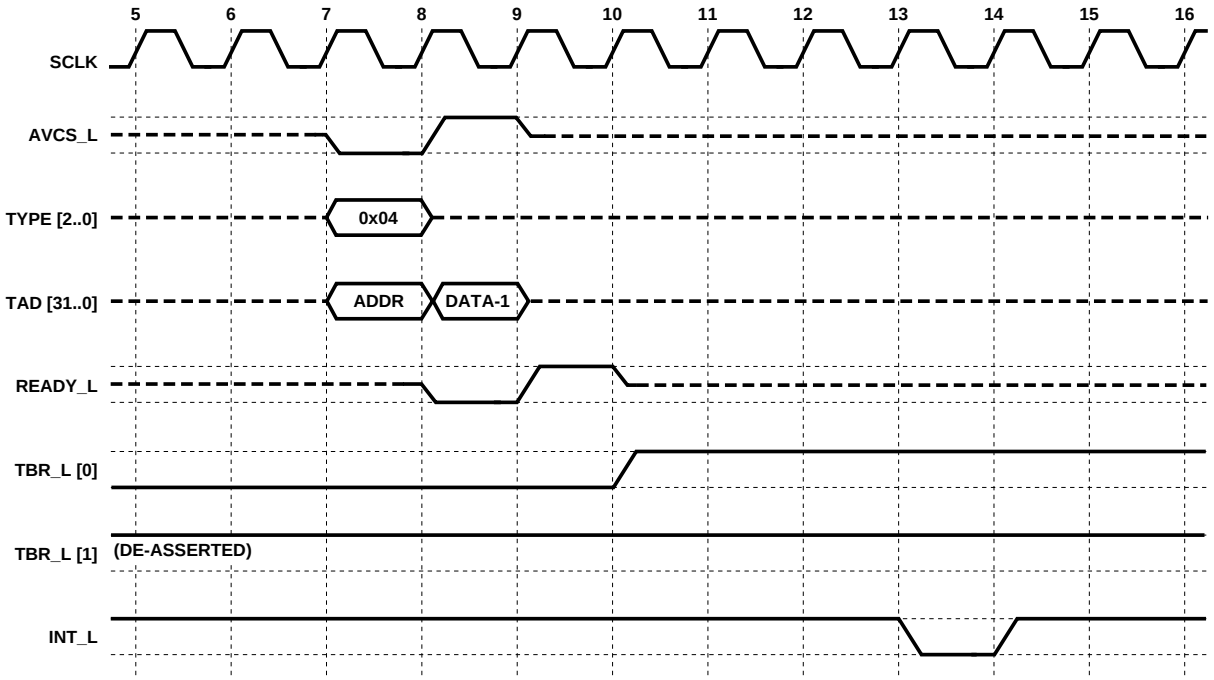


Figure 6.24 Interrupt Signal.

This figure shows Tachyon generating an interrupt by asserting the INT_L signal for one clock cycle. The INT_L cannot be asserted if TBR_L [0] or TBR_L [1] is asserted.

6.3 TSI Timing Requirements

6.3.1 TSI Input Signal Timing Requirements

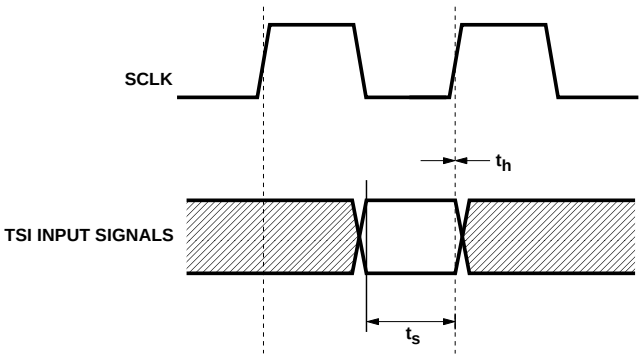


Figure 6.25 TSI Input Signal Timing.

Signal	Minimum Setup Time to the Rising Edge of SCLK (t_s)	Minimum Hold Time with respect to the Rising Edge of SCLK (t_h)	Units
Ready	12.5	0	ns
AVCS_L	12.5	0	ns
TYPE [2..0]	12.5	0	ns
TAD [31..0]	12.5	0	ns
PARITY	12.5	0	ns
RESET_L	14.0	0	ns
RETRY_L	12.5	0	ns
TBG_L	12.5	0	ns

Table 6.3 TSI Input Signal Timing Requirements.

The minimum setup time (t_s) applies from the signal being valid to the rising edge of SCLK. The minimum hold time (t_h) applies from the rising edge of SCLK to the signal becoming invalid. There is no hold requirement at the rising edge of SCLK in which a signal is undriven.

6.3.2 TSI Output Signal Timing Requirements

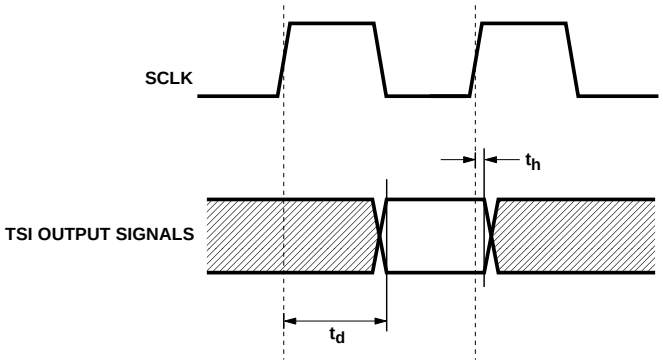


Figure 6.26 TSI Output Signal Timing.

Signal	Maximum Delay from the Rising Edge of SCLK (t_d)		Minimum Delay from the Rising Edge of SCLK (t_h)	Units
	25 pF	50 pF	0 pF	
READY_L	11.5	12.5	1.0	ns
AVCS_L	11.5	12.5	1.0	ns
TYPE [2..0]	11.5	12.5	1.0	ns
PREFETCH_L	11.5	12.5	1.0	ns
ERROR_L	11.5	12.5	1.0	ns
INT_L	11.5	12.5	1.0	ns
TBR_L [1..0]	11.5	12.5	1.0	ns
TAD [31..00]	13.0	14.0	1.0	ns
PARITY	16.75	17.75	1.0	ns

Table 6.4 TSI Output Signal Timing Requirements.

All delays are from the rising SCLK edge to the signal being valid or undriven. Uni-directional signals, i.e., PREFETCH_L, ERROR_L, and TBR_L[ ], are never undriven. AVCS_L and READY_L are always driven low, then driven high, then undriven.

Conditions for Minimum Delays:

1. Loading capacitance = 0 pF
2. Best-case chip process

Conditions for Maximum Delays:

1. Loading capacitance = 50 pF
2. Worst-case chip process

6.4 GLM Signal Information

6.4.1 GLM Transmit Signals

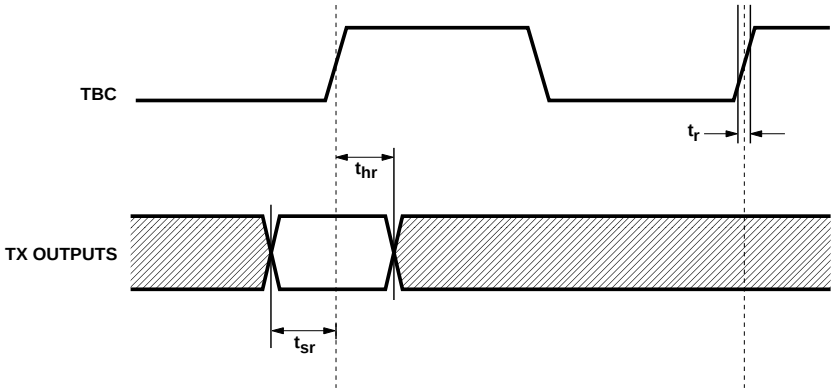


Figure 6.27 GLM Transmit Signal Information.

Label	Description	At 26.56 MHz	At 53.13 MHz	Units
C	Capacitance (Refer to Table Note 1, below)	10 / 25 (min / max)	10 / 25 (min / max)	pF
dc_{TBC}	Duty Cycle of TBC	40 / 60	45 / 55	%
t_{sr}	GLM Setup to Rising Edge TBC	6.0	2.0	ns
t_{hr}	GLM Hold from Rising Edge TBC	3.3	3.3	ns
t_r	Rise Time of TBC from 0.8 V to 1.5 V	1.4	1.4	ns
j_{TBC}	Maximum Jitter of TBC	0.005	0.005	% of frequency

Table 6.5 GLM Transmit Signal Information.

GLM Transmit Signal Information Table Notes

1. Tachyon meets GLM specifications; therefore a 10 pF output loading is assumed.

2. Table information assumes that transmit signals meet the conditions stated in the “Adapter Board Layout Requirements” section. Refer to “A.3 PCB Layout Suggestions”.

6.4.2 GLM Receive Signals

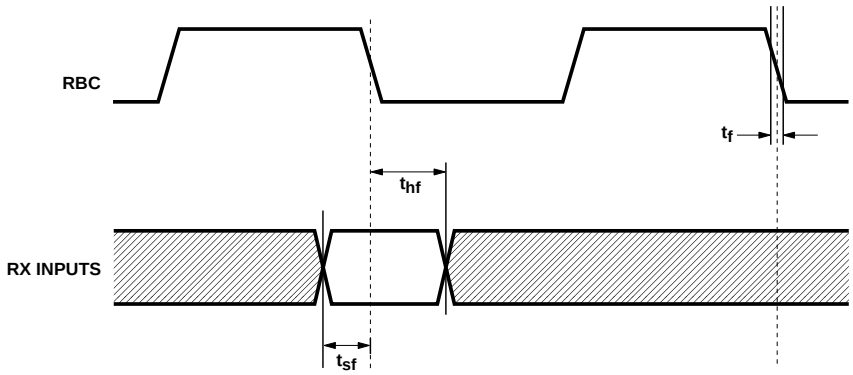


Figure 6.28 GLM Receive Signal Information.

Label	Description	At 26.56 MHz	At 53.13 MHz	Units
dc_{RBC}	Duty Cycle of RBC	40 / 60	45 / 55	%
t_{sf}	GLM Setup to Falling Edge RBC	2.5	2.5	ns
t_{hf}	GLM Hold from Falling Edge RBC	6.0	6.0	ns
t_f	Fall Time of RBC from 2.0 V to 1.5 V	1.2	1.2	ns
j_{RBC}	Maximum Jitter of RBC	0.01	0.01	% of frequency

Table 6.6 GLM Receive Signal Information.

GLM Receive Signal Information Table Note

1. Table information assumes that receive signals meet the conditions stated in the “Adapter Board Layout Requirements” section. Refer to “A.3 PCB Layout Suggestions”.

7. Electrical Descriptions

7.1 Absolute Maximum Ratings

Label	Parameter	Minimum	Maximum	Units
Vdd	Absolute Supply Voltage (Refer to the Warning below)	-0.3	+3.9	Volts
T_{op}	Ambient Operating Temperature (Refer to "A.1 Limited Airflow Applications" on page 103.)	0	+50 (0 m/s airflow) +70 (1.5 m/s airflow)	° C
T_{stg}	Storage Temperature	-40	+100	° C

Table 7.1 Absolute Maximum Electrical Ratings.

WARNING The Absolute Minimum/Maximum Supply Voltage (Vdd) specification should not be used as a limit for normal device operation. Sustained operation exceeding the limits of the Recommended Supply Voltage (Refer to "Table 7.2 Recommended Operating Conditions".) could result in permanent device damage or impaired device reliability.

7.2 Recommended Operating Conditions

Label	Parameter	Minimum	Typical	Maximum	Units
Vdd	Recommended Supply Voltage	3.0	3.3	3.6	Volts
f_{clk}	TSI Clock Frequency, SCLK	24	-	40	MHz
dc_{clk}	Duty Cycle, SCLK (Refer to Note 1 below)	40	-	60	%
$t_{r/f}$	Rise/Fall Time, SCLK (Refer to Note 2 below)	-	2.5	3.5	ns
j_{clk}	Maximum Jitter of SCLK	-	-	100	ps
TBC_r	TBC Rise Time	0.5	-	2.8	ns
RBC_f	RBC Fall Time	0.7	-	2.4	ns

Table 7.2 Recommended Operating Conditions.

Recommended Operating Conditions Notes

1. For Duty Cycle for TBC and RBC:
   a. at 26 MHz, a maximum 40/60 Duty Cycle is allowed.
   b. at 53 MHz, a maximum 45/55 Duty Cycle is allowed.

2. The Rise/Fall Time of SCLK should be kept under 3.5 ns. A Rise/Fall Time at 2.5 ns or lower is preferred to minimize insertion delays and phase error.

7.3 Electrical Parameters

Label	Parameter	Signal (S)	Condition	Min.	Typ.	Max.	Units
Vdd	Supply Voltage	Vdd	-	3.0	3.3	3.6	V
I_{dd}	Supply Current	Vdd	SCLK = 33 MHz RBC = 53 MHz TBC = 53 MHz Vdd = 3.6 V T_{amb} = 50° C	-	-	1.0	A
V_{il}	Input Low Voltage	All Inputs	-	Vss -0.5	-	0.8	V
V_{ih}	Input High Voltage	All Inputs	-	2.0	-	5.5	V
I_{in}	Input Current	PLL_RSTN (pin 44)	V_{in} = Vss or Vdd	-35	-115	-214	µA
I_{in}	Input Current	PLL_IDD_TEST (46)	V_{in} = Vss or Vdd	-35	-115	-214	µA
I_{in}	Input Current	PLL_TEST_DATA (47)	V_{in} = Vss or Vdd	-35	-115	-214	µA
I_{in}	Input Current	IDD_TEST (pin 55)	V_{in} = Vss or Vdd	-35	-115	-214	µA
I_{in}	Input Current	TCK (pin 122)	V_{in} = Vss or Vdd	-35	-115	-214	µA
I_{in}	Input Current	TMS (pin 124)	V_{in} = Vss or Vdd	-35	-115	-214	µA
I_{in}	Input Current	RSTN (pin 125)	V_{in} = Vss or Vdd	-35	-115	-214	µA
I_{in}	Input Current	TDI (pin 126)	V_{in} = Vss or Vdd	-35	-115	-214	µA
I_{in}	Input Current	PLL_TEST_MODE (48)	V_{in} = Vss or Vdd	35	115	222	µA
I_{in}	Input Current	SCAN_EN (pin 136)	V_{in} = Vss or Vdd	35	115	222	µA
I_{in}	Input Current	TEST_MODE (pin 140)	V_{in} = Vss or Vdd	35	115	222	µA
I_{in}	Input Current	All Other Inputs	V_{in} = Vss or Vdd	-10	± 1	+10	µA
V_{oh}	Output High Voltage	All Outputs	I_{ol} = -6 mA	2.4	-	Vdd	V
V_{ol}	Output Low Voltage	All Outputs	I_{ol} = 6 mA	-	-	0.4	V
I_{oz}	3-State Output Leakage Current	-	V_{oh} = Vss or 5.5 V	-10	± 1	+10	µA
I_{os}	Output Short Circuit Current	-	V_{out} = Vdd	-	-	140	mA
I_{os}	Output Short Circuit Current	-	V_{out} = Vss	-	-	-40	mA
C_{in}	Pin Input Capacitance	-	-	3.0	-	5.0	pF
C_{out}	Pin Output Capacitance	-	-	3.0	-	5.0	pF

Table 7.3 Electrical Parameters.

7.4 Pull-Up Values

The following table lists the TSI signals that require pull-up resistors. All signals listed here must be pulled up to Vdd. A recommended resistor value is listed. Tolerances for these resistors are all 10%, unless stated otherwise.

TSI Signal Name	Pull-Up Value (Ω)
TAD[31..0]	10K x 32
PARITY	10K
AVCS_L	10K
TYPE[2..0]	10K x 3
READY_L	10K
RETRY_L	10K
PREFETCH_L	10K
ERROR_L	10K
INT_L	10K
TBR_L[1..0]	10K x 2

Table 7.4 Pull-up Values.

7.5 Pull-Down Value

The following test pin must be pulled down to ground via a pulldown resistor.

Test Signal Name	Pin #	Pull-Down Value (Ω)
TEST_MODE	140	4.7K

Table 7.5 Test Mode Pin.

7.6 External PLL Components

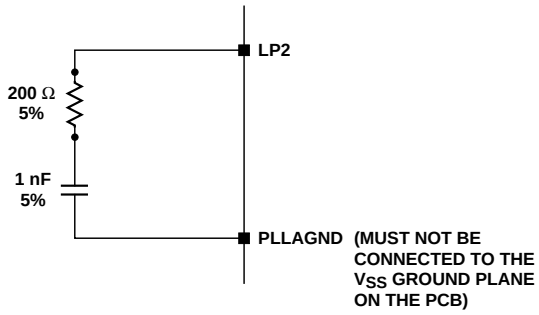


Figure 7.1 External PLL Components.

8. Mechanical Descriptions

8.1 General Information

Package Type	208 Metal Quad Flat Pack (MQUAD)
Power Dissipation	3.5 Watts
Airflow Requirements	1.5 Meters/second

Table 8.1 Mechanical Information.

8.2 Thermal Specifications

Conditions for Thermal Specifications:

1. No heat sink
2. Power dissipation = 3.5 Watts
3. Tj (max) = 110 º C

Parameter	Conditions				Units
Airflow	0.0	1.0	2.0	3.0	meters/second
Package Thermal Resistance (θja)	15	12	11	10	ºC/Watt
Package Thermal Resistance (θjc)	2.6	2.6	2.6	2.6	ºC/Watt
Maximum Ambient Temperature	58	68	72	75	ºC

Table 8.2 Thermal Specifications.

8.3 Dimensions

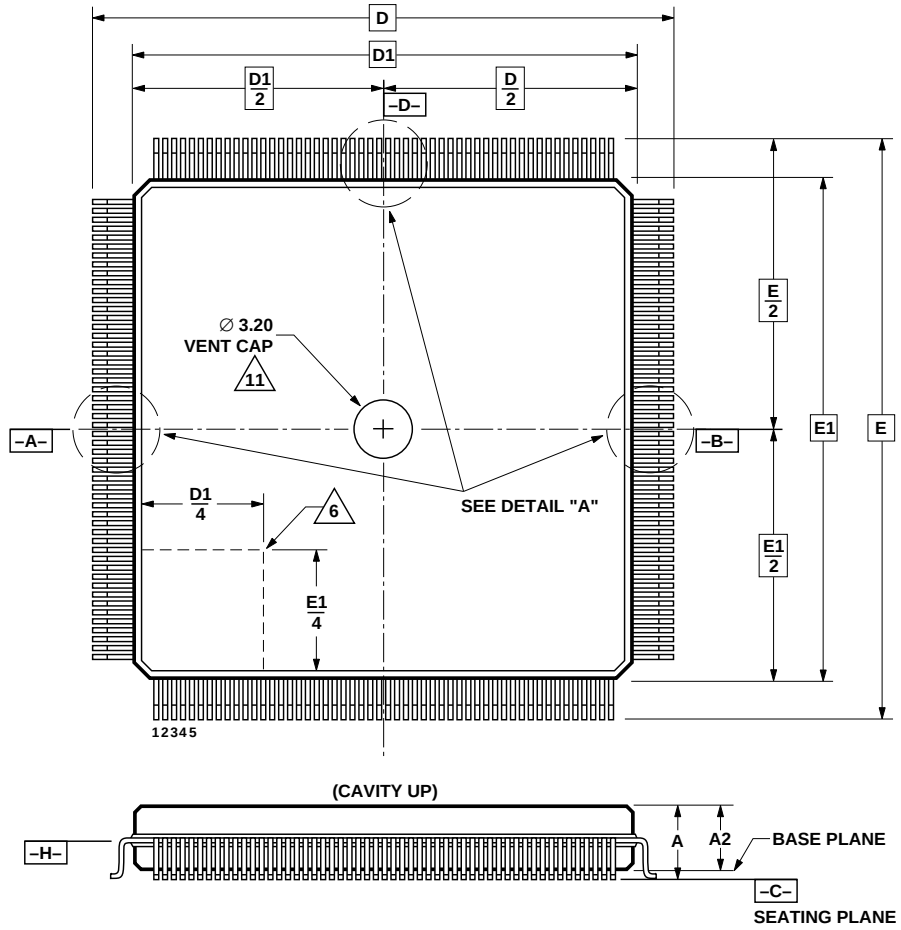


Figure 8.1 Side View and Top View.

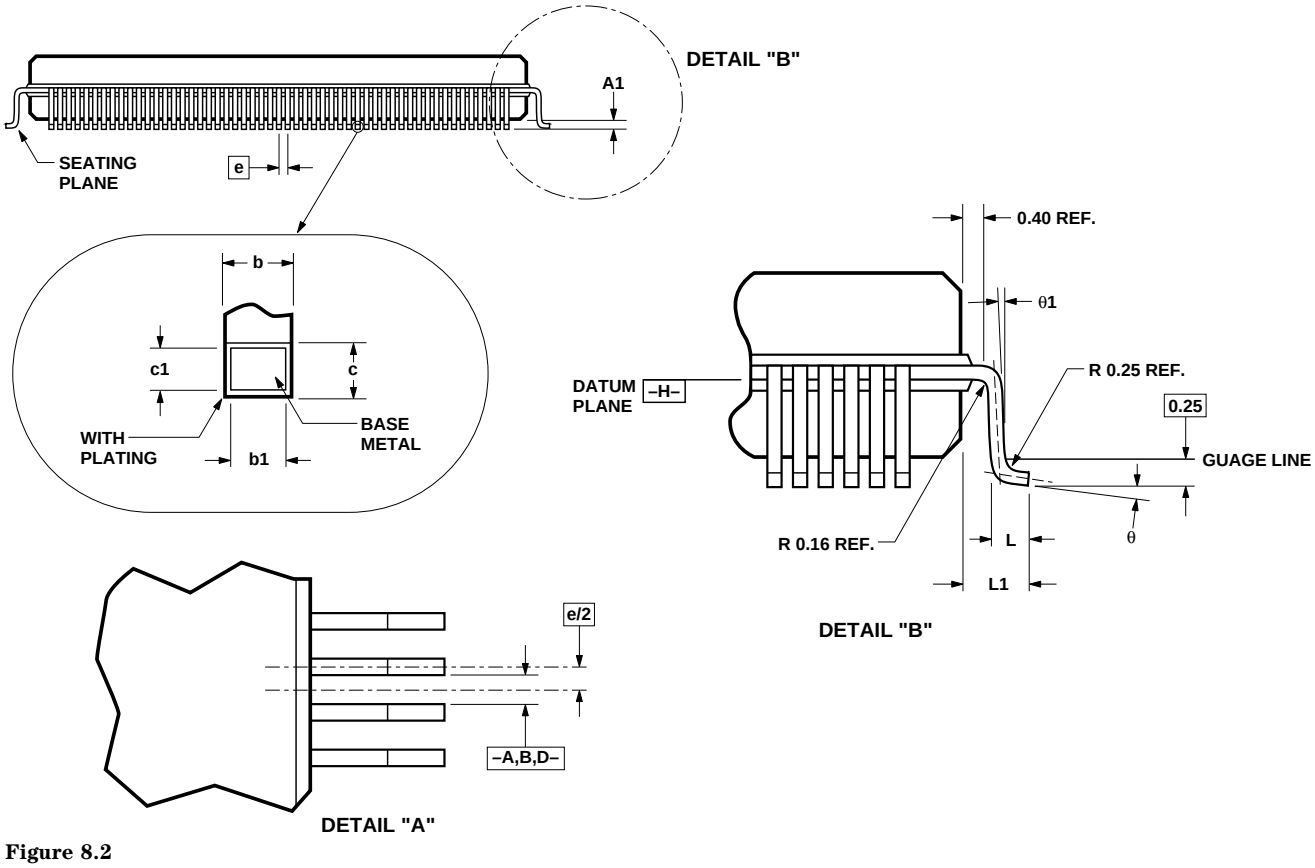


Figure 8.2

Dimensions in mm				Notes
Sym	**Minimum**	**Nominal**	**Maximum**	
A			4.10	
A1	0.25			
A2	3.17	3.30	3.45	
D	30.40	30.60	30.80	4
D1	27.56	27.64	27.72	5
E	30.40	30.60	30.80	4
E1	27.56	27.64	27.72	5
e	0.50 BSC			
b	0.17	0.18	0.27	8.10 (Plated lead width)
b1	0.16		0.24	
c	0.12		0.20	8.10
c1	0.15 ± 0.03			
L	0.50	0.60	0.70	
L1	1.30 REF.			
N	208			
θ	0		7	Lead foot angle
θ1	0		7	
Tolerances of Form and Position				
aaa	0.20			
bbb	0.20			
ccc	0.08			Coplanarity of leads
ddd	0.08			Lead position tolerance

Table 8.3 Side View and Top View Dimensions.

8.4 Recommended Handling Precautions

The MQUAD® package has an open cavity, internally; hence ultrasonic cleaning will damage the device. DO NOT USE ultrasonic cleaning process with this device. Additional circuitry is built into the various input and output pins on this chip to protect them against low level electrostatic discharge, however, they are still ESD sensitive and standard procedures for static sensitive devices should be used in handling and assembly of this chip.

*MQUAD® is a registered trademark of Olin Corporation.

A.1 Limited Airflow Applications

When using Tachyon in applications where airflow is less than 1.5 meters/sec, careful attention must be given to ensure that Tachyon junction temperatures remain below 110° C. If junction temperatures exceed 100° C then the functional lifetime of the device may be reduced and/or potential data loss may result.

Junction Temperature Calculation

$T_{junction} = T_{ambient} + (P_{maximum} * \theta_{ja})$

$T_{junction}$ = The calculated junction temperature in °C.

$T_{ambient}$ = The ambient air temperature around device in °C.

$P_{maximum}$ = The maximum power dissipation of device in Watts. For Tachyon this is 3.5 Watts.

θ_{ja} = The package thermal resistance in °C/Watt.

Package Thermal Resistance

The package thermal resistance, with respect to ambient air temperature, is highly dependent upon the airflow. The following table shows how the thermal resistance of the Tachyon package changes with respect to airflow. The table includes values with and without a heat sink attached.

Parameter	Conditions				Units
Airflow	0.0	1.0	2.0	3.0	meters/sec
208 MQuad	15.0	12.0	11.0	10.0	θ_{ja} – °C/Watts
208 MQuad w/Heat Sink	13.0	9.0	7.5	6.5	θ_{ja} – °C/Watts

Table A.1.1 Package Thermal Resistance for 208 MQuad.

Example Heat Sink:

Thermaloy P/N 18455B Black Anodize Aluminum Omni-directional Post Type

Dimensions : width 18 mm, length 21 mm, height 10 mm

Posts : 42 @ 1.2 mm x 1.2 mm x 8 mm

Approximate Effective Surface Area: 1990 mm sq.

The heat sink mentioned above is for reference only and is not available from Agilent Technologies.

Examples

With an airflow of 1.5 meters/sec and an ambient air temperature of 70 °C, the junction temperature is calculated:

$T_{junction}$ = 70 °C + (3.5 * 11.5) = 110.25 °C

If the ambient air temperature is greater than 70 °C or airflow is less than 1.5 meters/sec then a heat sink may be needed. The dimensions and surface area of the heat sink can be tailored to the specific application requirements.

An example of an application which requires special attention is where airflow is 0 meters/sec. There are two solutions to this problem:

1. Put an upper limit on the ambient air temperature: 110 °C = $T_{ambient}$ + (3.5 * 15), solving the $T_{ambient}$ yields: $T_{ambient}$ = 110 °C - (3.5 * 15) = 57.5 °C.

2. Reduce θ_{ja} by using a heat sink which provides the required thermal resistance: 110 °C = 70 °C + (3.5 * θ_{ja}) solving for θ_{ja} yields: θ_{ja} = (110° - 70°) / 3.5 8.5 °C per Watt.

A.2 Implementing Tachyon with Little Endian System

To use Tachyon with a little endian system, implement the following steps:

Step 1:

Connect:

Tachyon's TAD pin 31 to bit 31 of the little endian system

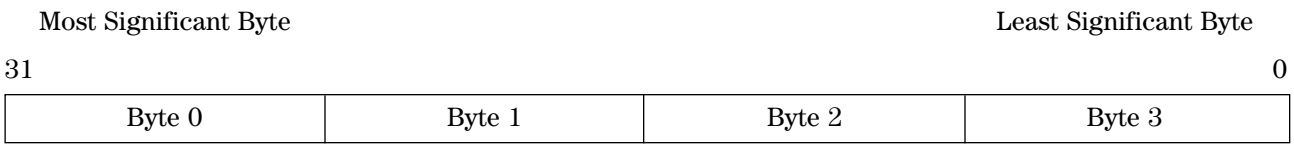
Tachyon's TAD pin 30 to bit 30 of the little endian system

... ...

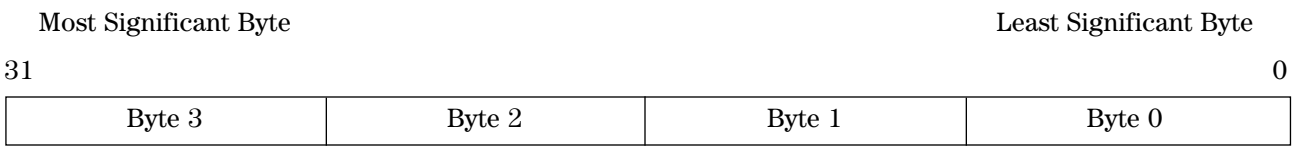
Tachyon's TAD pin 0 to bit 0 of the little endian system

For a 32-bit word, bit 31 is the most significant bit and bit 0 is the least significant bit.

Big Endian:



Little Endian:



By connecting Tachyon's TAD 31 to Little Endian's bit 31, the most significant byte of the Tachyon bus gets tied to the most significant byte of the Little Endian bus and the least significant byte of the Tachyon bus gets tied to the least significant byte of the Little Endian bus in a 32-bit transfer. Tying these buses together allows Tachyon to place any address that it wants to access on the correct byte lane (MSB to MSB, etc.). This causes a byte swap on all byte-wide transfers. 32-bit transfers are not swapped.

Step 2:

Implement a Hardware swap of all data for DMA transfers. This should only be done on DMA transfers where Tachyon masters the bus and either reads or writes data to host memory.

Slave reads and writes should not be swapped and addresses should not be swapped.

All data transferred serially is transferred byte by byte. Therefore, data going out on the link is transferred byte-wide. For byte-wide transfers, the data was byte-swapped in Step 1 and must be swapped back.

Slave accesses are not byte-wide transfers and a byte swap is not needed. Slave accesses are 32-bit transfers and the byte lanes match.

DMA transfers may be byte-wide (data to be sent out on the link) or 32-bit (Tachyon control structure) transfers. However, the type of DMA transfer is indistinguishable and therefore all DMA transfers must be considered byte-wide. For byte-wide transfers, the data was byte-swapped in Step 1 and must be swapped back.

Step 3:

Host software must do a byte swap on all of Tachyon's DMA'd control structures. Anything Tachyon DMA's to or from the host must be swapped in software so Tachyon interprets it correctly. Data that is sent out on the link does not have to be swapped in software.

In Step 2, DMA link data and control structures transfers were byte-swapped. Either all the link data or all the control structures need to be swapped in software. Because there are fewer control structures than link data, it is more efficient to swap all the control structures rather than all of the data. To ensure that Tachyon can interpret its DMAed control structures properly, all the control structures must be swapped in software.

Step 4:

Since Slave reads and writes are not swapped by the Hardware swap (refer to 'Step 2:' above), the information written to Tachyon in Slave reads and writes does not have to be software swapped to be interpreted correctly by Tachyon.

Refer to Step 2 explanation on why Slave reads and writes do not need to be swapped.

Step 5:

Swapping is defined as follows:

Byte 0 is swapped with Byte 3

Byte 1 is swapped with Byte 2

This example attempts to explain the reasons the changes are necessary for Tachyon to be used with a Little Endian System.

There are three different types of data which move across the backplane both to and from Tachyon:

1. Slave reads and writes / 32-bit wide transfer
2. Link data (data that is sent over the link) / byte-wide transfer
3. Tachyon control structures / 32-bit wide transfer

A.3 PCB Layout Suggestions

Introduction

This application note provides suggestions on the physical layout of a Printed Circuit Board (PCB) containing Tachyon and a Gigabit Link Module (GLM).

PCB Layers and Signals

The following PCB layers are suggested:

Layers	Description
Layer 1	Signal (Side A)
Layer 2	Ground
Layer 3	Signal
Layer 4	Signal
Layer 5	Power
Layer 6	Signal (Side B)

Table A.3.1 Layer Descriptions.

Signal Routing

- The signals from Tachyon to the GLM should be routed on Layers 1 and 6.
- All transmit signals (i.e. TBC, TX [20..0]) should be routed on Layer 1. All receive signals (i.e. RBC, RX [20..0]) should be routed on Layer 6. Trace widths of these signals should be 6 mils with an 8 mil gap between them. Routing this way reduces the risk of crosstalk between transmit and receive.
- The Tachyon System Interface (TSI) side of Tachyon may be routed on all signal layers. Trace widths should be 8 mils with a gap of 8 mils.
- There is only a single plane for ground (Layer 2). All the Tachyon Vss signals connect to this plane, including the PLLVss signal.

Adapter Board Requirements

Delay Specifications

1. The maximum delay of the traces is 78.74 ps/cm (200 ps/in)
2. The minimum delay of the traces is 55.12 ps/cm (140 ps/in)

Receive Trace Specifications

1. RBC trace maximum length = [shortest RX trace + 3.81 cm]
2. RBC trace minimum length = [longest RX trace - 1.27 cm]

Transmit Trace Specifications

1. TX trace maximum length = 8.26 cm (3.25 in)
2. TX trace minimum length = 3.81 cm (1.50 in)
3. On all TX outputs, specifically TX [19..0], LCKREF_L, and EWRAP, Tachyon requires a minimum capacitance of 10 pF (GLM specification assumes a 10 pF load is present on Tachyon) and a maximum capacitance of 25 pF.

Clock Generator Trace Specifications

1. Clock Generator trace to Tachyon < [Clock Generator trace to GLM + 7.62 cm]
2. Clock Generator Rise Time = 2.8 ns

SCLK Routing to Tachyon and to the GLM

SCLK should be routed on Layer 1 with an 8 mil trace width. This trace must be as short as possible and have Tachyon as its only load. The trace should have guard traces along it.

Tachyon's GLM interface receives its transmit clock from an on-board oscillator. The output of this oscillator has two loads, Tachyon's TBC pin and the GLM interface's TBC pin. Thus the oscillator output must be split with one route through a 10 Ω resistor going to Tachyon, and the other route through another 10 Ω resistor going to the GLM pin. The route length to Tachyon and to the GLM transceivers should be equal. Also, the 10 Ω resistors should be near the oscillator output. These traces should be on Layer 1 and have guard traces along their length.

The 10 Ω resistor may have to be increased or reduced depending on signal quality at the load.

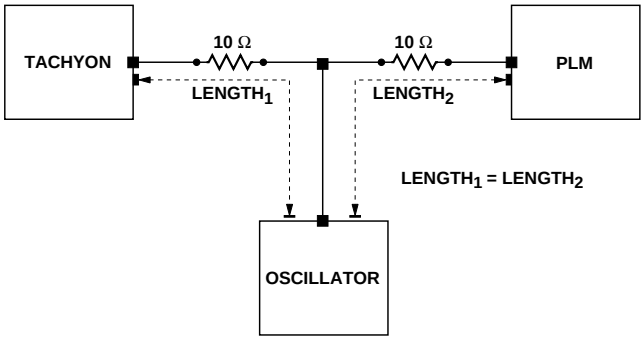


Figure A.3.1 SCLK Routing to Tachyon and to the GLM.

Calculation of Pull-Up Resistor on the Tri-Stated I/O of Tachyon

Calculation for maximum pull-up resistor that can be used on the Tri-stated I/O of Tachyon:

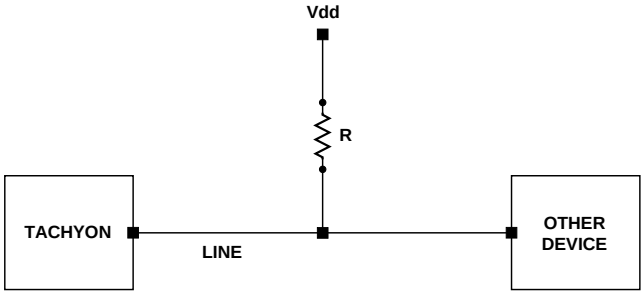


Figure A.3.2 Pull-Up Resistor on the Tri-Stated I/O of Tachyon.

Values:

Ioz for Tachyon	= 10 uA
Ioz for Other Device	= 10 uA
Vdd minimum low	= 3.00 V
Vih minimum	= 2.00 V

Using the values above, the maximum value of R when the line is tri-stated to keep Vih at the minimum level is:

R = (3-2) Volts / 20 uA = 50 kΩ (this includes resistor tolerance)

GLM Signal Strappings Requirements

- TX_SI must be tied low with a maximum resistor value of 1 kΩ
- EN_CDET must be tied high with a maximum resistor value of 1kΩ

GLM Placement Recommendation

For optimal results, place Tachyon on the opposite side of the printed circuit board and behind the GLM Samtec connector. This GLM and Tachyon locality optimizes trace length and routing.

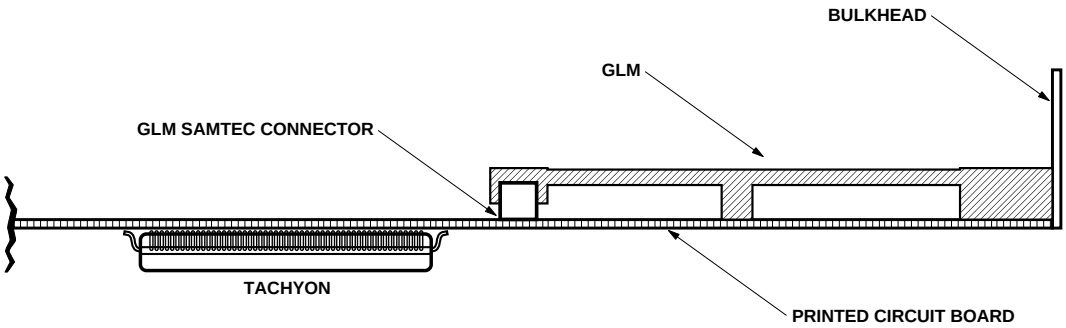


Figure A.3.3 GLM and Tachyon Locality for Trace Length and Routing Optimization.

Power Connections

A continuous ground plane (Vss) should be provided for the entire PCB. The power plane (Vdd_Other) should be split into different regions to reduce noise and increase isolation between Tachyon and other components. Three methods are suggested:

1. **Ferrite Beads Method**
   This was the original recommendation for power connections and is adequate for existing designs.

VddTAC is the region for Tachyon power. This region receives its power through a ferrite bead from Vdd_Other and requires decoupling capacitors. All of the Tachyon Vdd and Vdd2 pins connect directly to VddTAC, with the exception of PLLVdd, which connects to VddTAC through another ferrite bead. A 0.01 µf decoupling capacitor should be placed near the PLLVdd pin to provide decoupling to the ground plane. The ferrite beads should have a minimum saturation current of 2 Amps. A 25 mil trace (minimum, 100 mil preferred) should be used to connect PLLVdd through the ferrite bead to VddTAC. Tachyon Vss and PLLVss are both connected to the PCB ground plane.

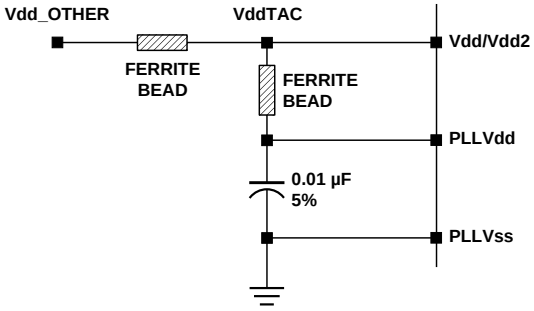


Figure A.3.4 Ferrite Beads Method.

The VddTAC plane resides under the Tachyon part as follows:

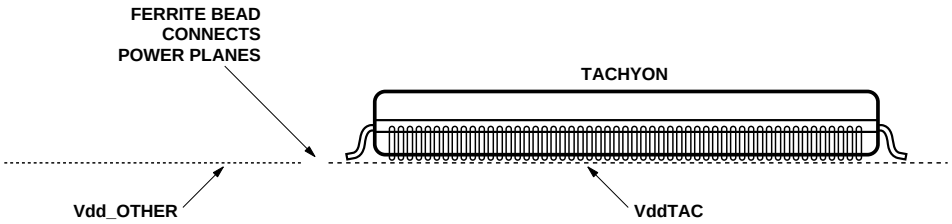


Figure A.3.5 Power Plane Regions.

Power (Vdd and Vdd2) should be routed with a 100 mil trace width through fuses or ferrite beads prior to connecting into the plane through vias. Multiple vias are needed to meet current requirements for bringing power onto the plane.

2. PLL Ferrite Bead Alternative Method

This is the current recommendation due to its optimal noise immunity to Tachyon's internal PLL circuitry.

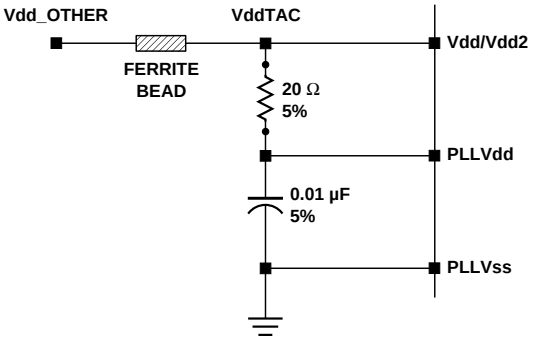


Figure A.3.6 PLL Ferrite Bead Alternative Method.

3. Multiple Ferrite Beads for Maximum Isolation Method

This is recommended for systems that measure a large amount of noise on their circuits when using method 2 (PLL Ferrite Bead Alternative Method).

Tachyon has been designed with multiple internal power planes with separate input pins to isolate the output buffer/drivers, central core functions, and PLL oscillator. These power inputs are referenced as Vdd, Vdd2, and PLLVdd. In a typical situation, Vdd and Vdd2 are connected at the board level, with additional filtering for PLLVdd. Some applications may require additional isolation and improved noise immunity between Vdd and Vdd2. This alternative may be obtained by using multiple ferrite beads connecting each of the power regions (Vdd, Vdd2, PLLVdd) to Vdd_Others and additional decoupling capacitors for each region.

Separate low-inductance power regions for both Vdd and Vdd2 need to be provided on the PCB under the Tachyon package, separated from each other with multiple layers. The preferred arrangement is to have the Vdd and Vdd2 power regions on opposite sides of the PCB ground plane.

Because PLLVdd is a single input into Tachyon, only a short, low-inductance trace needs to be provided from the ferrite bead to the PLLVdd pin. Decoupling capacitors for all three power regions should be located close to the Tachyon power input pins.

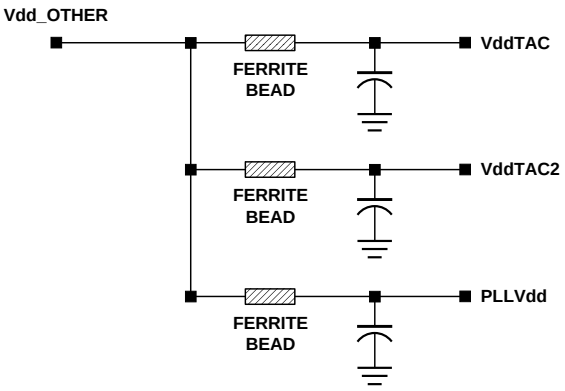


Figure A.3.7 Multiple Ferrite Beads for Maximum Isolation Method.

Document Conventions

Length of Queues

The length of a queue is actually the number of entries in a queue. Since a queue is zero-based, the programmed value for the length field of a queue length register must be the number of entries minus one. Refer to “Table 5.2 Length Registers Information’ on page 27.

Reserved

All fields labeled “Reserved”, “Reserve”, “Rsvd”, “Res” or “R” should not be used and should be initialized to zero.

Remote Node

Remote Node means the same as a destination node, a responder node, or a client.

Set and Clear

“Set” implies “set to binary one”. “Clear” implies “clear to binary zero”. When a bit is discussed without a “set” or “clear” indication, then the bit is set to one.

Word

A “word” is 4 bytes (32 bits) long.

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Technical Support

Telephone: 1-800-TACHYON (1-800-822-4966).
E-mail: tachyon@agilent.com

Homepage

View Tachyon World Wide Web homepage: http://tachyon.rose.agilent.com/

Pricing and Delivery

Contact your local HP Component Sales Representative.

Tachyon C Code

Sample Tachyon C Code is available via anonymous ftp over the Internet. The C code is available in two formats:

1. UNIX (shar) Format

   Filename - ProgGuideCode.shar

   This is a UNIX shar file of the C code .c and .h files. Instructions for unpacking the sample code files are included at the beginning of the shar file.

2. ASCII Text Format

   Filename - ProgGuideCode

   This is a concatenated ASCII file of all the .c and .h sample files. Each file is delimited by:
   `/*  End of C file  */`

To access the files,

On your system, type: ftp rosegarden.external.agilent.com

You will get a connect notice.

At the name prompt, type: ftp

At the password prompt, type your Internet e-mail address, for example,

username@hostname.somewhere.companyname.com

At the ftp prompt, type: cd pub/tachyon

At the ftp prompt, type: get ProgGuideCode.shar (or get ProGuideCode)

At the ftp prompt, type: quit

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