EMG2DXV5T1, EMG5DXV5T1

Preferred Devices

Product Preview

Dual Bias Resistor Transistors

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SOT−553 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Moisture Sensitivity Level: 1
- Available in 8 mm, 7 inch Tape and Reel
- Lead−Free Solder Plating

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	230 (Note 1) 338 (Note 2) 1.8 (Note 1) 2.7 (Note 2)	mW °C/W
Thermal Resistance − Junction-to-Ambient	$R_{\theta JA}$	540 (Note 1) 370 (Note 2)	°C/W
Thermal Resistance − Junction-to-Lead	$R_{\theta JL}$	264 (Note 1) 287 (Note 2)	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ Minimum Pad
2. FR−4 @ 1.0 x 1.0 inch Pad

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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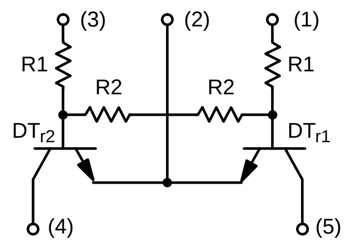
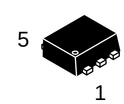
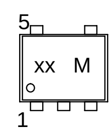
NPN SILICON BIAS RESISTOR TRANSISTORS





SOT−553
CASE 463B

MARKING DIAGRAM



xx = Specific Device Code
UF = EMG5
UP = EMG2
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
EMG2DXV5T1	SOT−553	4 mm pitch 4000 / Tape & Reel
EMG2DXV5T5	SOT−553	2 mm pitch 8000 / Tape & Reel
EMG5DXV5T1	SOT−553	4 mm pitch 4000 / Tape & Reel
EMG5DXV5T5	SOT−553	2 mm pitch 8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking	R1 (K)	R2 (K)
EMG2DXV5T1	SOT−553	UP	47	47
EMG5DXV5T1	SOT−553	UF	10	47

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Q1 & Q2)						
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	−	−	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	−	−	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	EMG2DXV5T1 EMG5DXV5T1	I_{EBO}	− −	− −	0.1 0.2	mAdc
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	−	−	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	−	−	Vdc
ON CHARACTERISTICS (Q1 & Q2) (Note 3)						
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	EMG2DXV5T1 EMG5DXV5T1	h_{FE}	80 80	140 140	− −	
Collector-Emitter Saturation Voltage (IC = 10 mA, I_B = 0.3 mA)		$V_{CE(sat)}$	−	−	0.25	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	 EMG2DXV5T1 EMG5DXV5T1	V_{OL}	 − −	 − −	 0.2 0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)		V_{OH}	4.9	−	−	Vdc
Input Resistor	EMG2DXV5T1 EMG5DXV5T1	R_1	32.9 7.0	47 10	61.1 13	kΩ
Resistor Ratio	EMG2DXV5T1 EMG5DXV5T1	R_1/R_2	0.8 0.17	1.0 0.21	1.2 0.25	

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

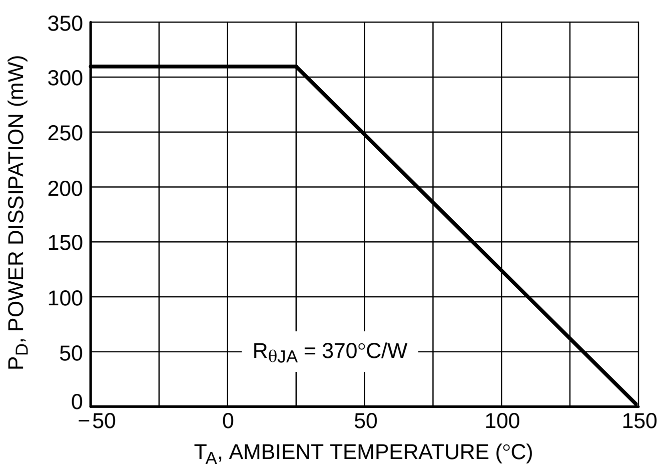


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS — EMG2DXV5T1

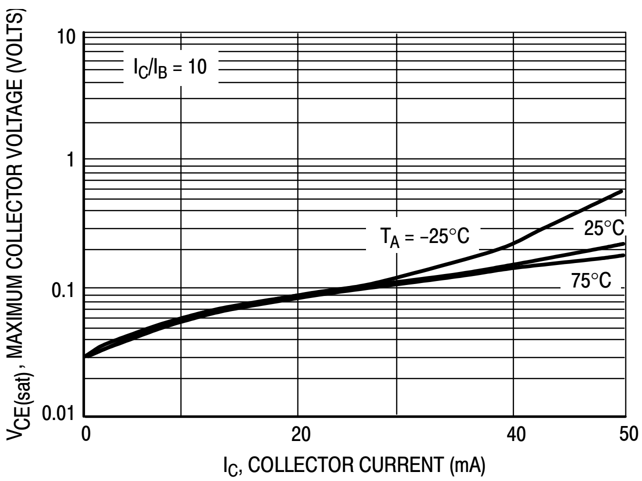


Figure 2. $V_{CE(sat)}$ versus I_C

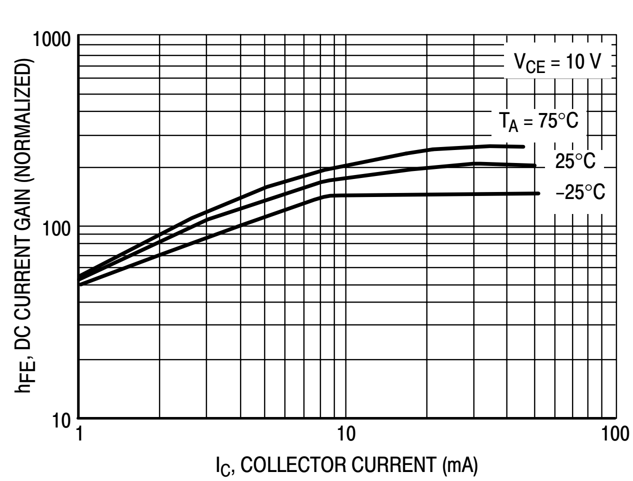


Figure 3. DC Current Gain

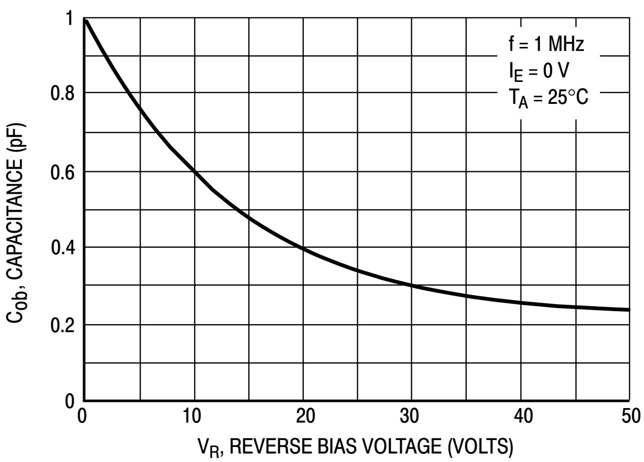


Figure 4. Output Capacitance

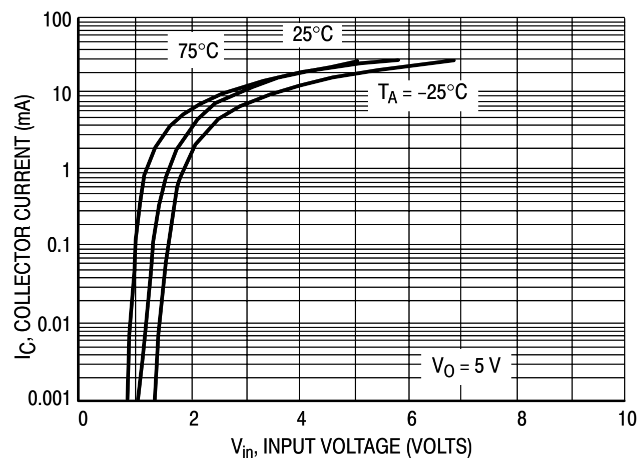


Figure 5. Output Current versus Input Voltage

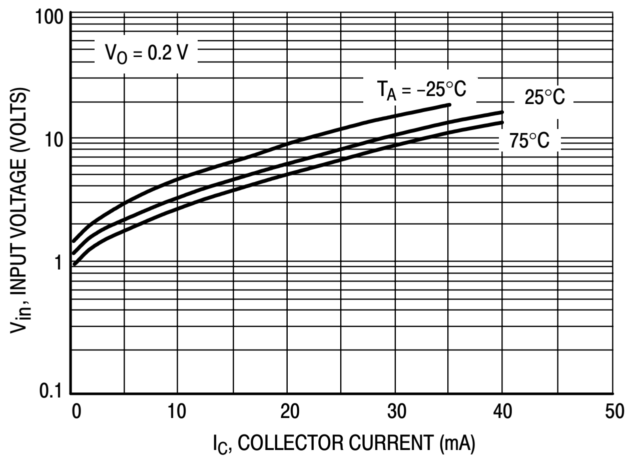


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − EMG5DXV5T1

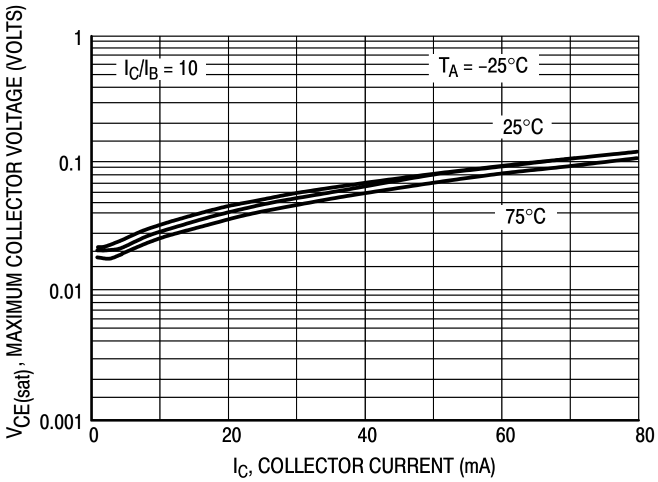


Figure 7. $V_{CE(sat)}$ versus I_C

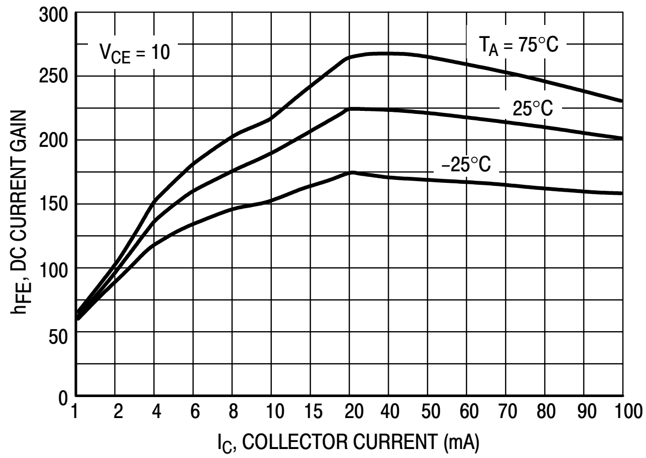


Figure 8. DC Current Gain

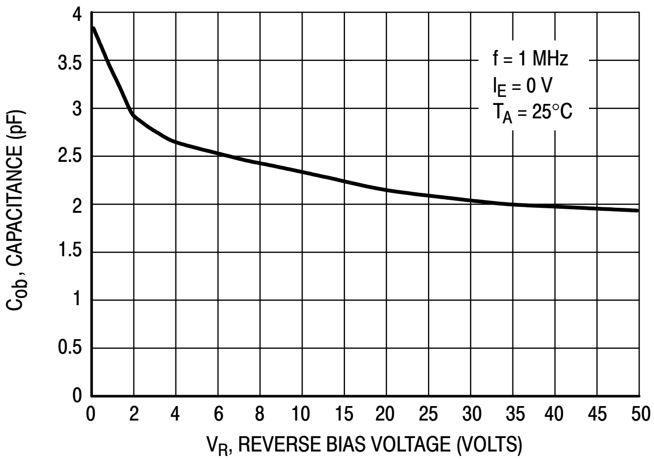


Figure 9. Output Capacitance

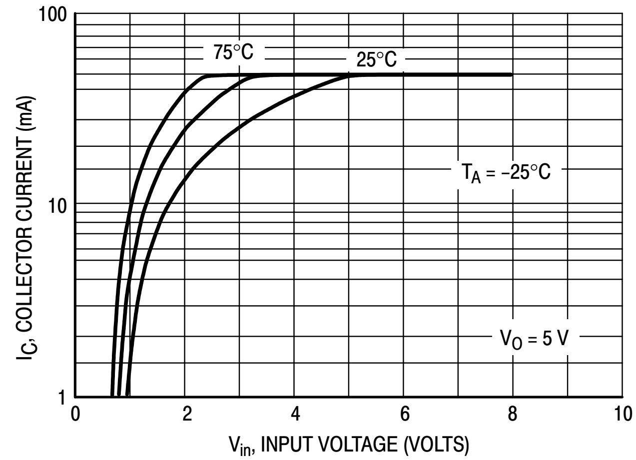


Figure 10. Output Current versus Input Voltage

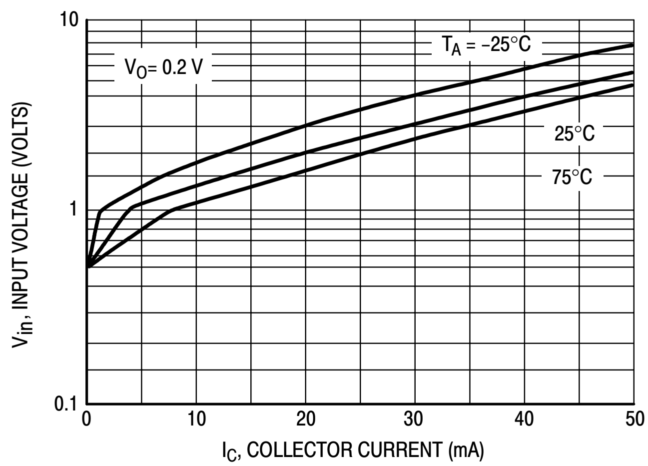


Figure 11. Input Voltage versus Output Current

TYPICAL APPLICATIONS FOR NPN BRTs

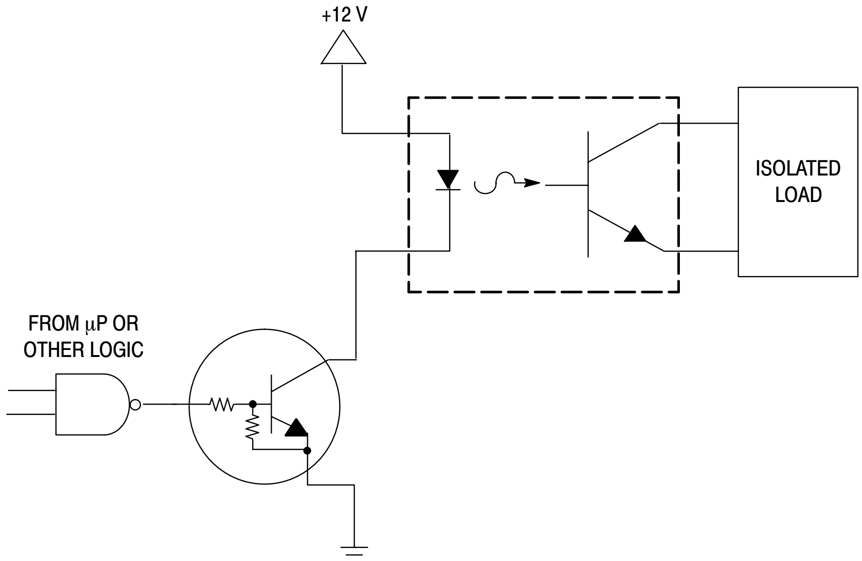


Figure 12. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

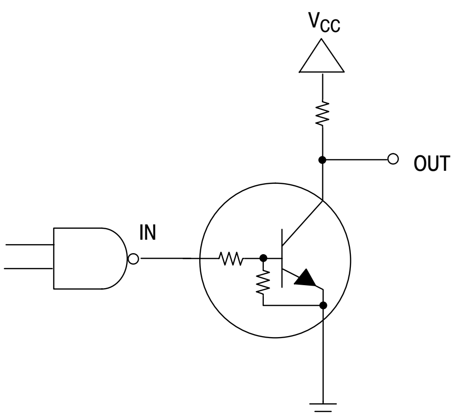


Figure 13. Open Collector Inverter: Inverts the Input Signal

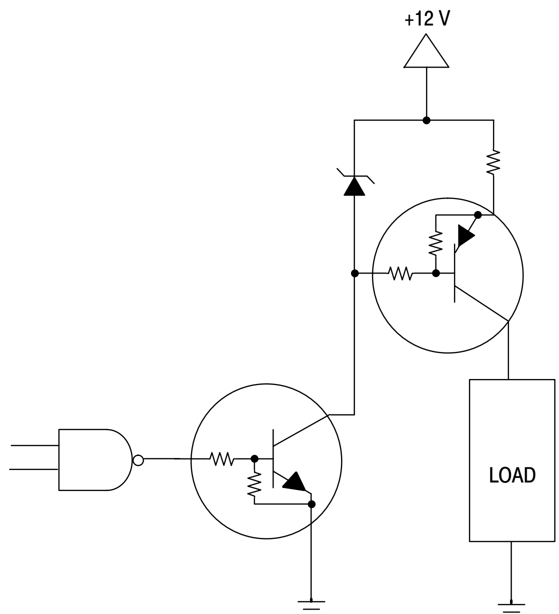
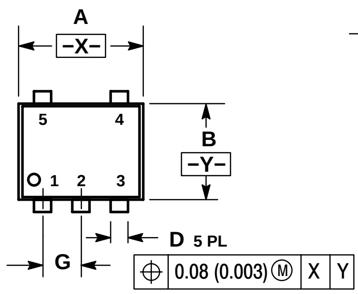


Figure 14. Inexpensive, Unregulated Current Source

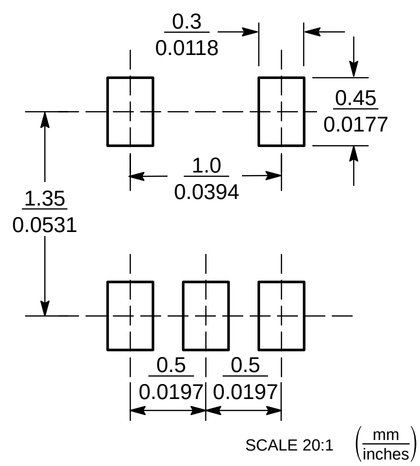
PACKAGE DIMENSIONS

SOT−553
XV5 SUFFIX
5−LEAD PACKAGE
CASE 463B−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067



SOT−553

Figure 15. SOT−553 POWER DISSIPATION

*For information on soldering specifications, please refer to our Soldering Reference Manual, SOLDERM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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