

RoHS Compliant & Pb-Free Product  
Package Style: QFN, 12-Pin, 3 x 3

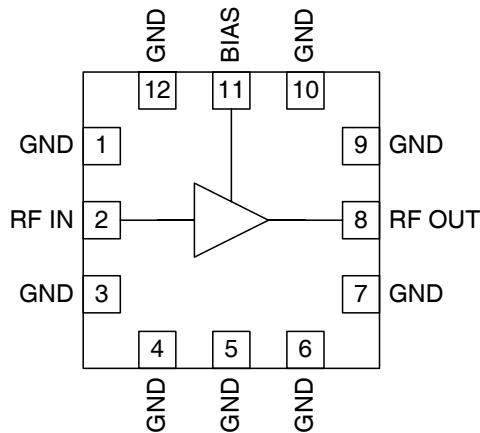


## Features

- 500MHz to 2GHz
- +40.8dBm Output IP3
- +14.2dB Gain at 1850MHz
- +12.4dBm Input P1dB at 1850MHz
- 2.8dB Noise Figure at 1850MHz
- Single 5V Power Supply

## Applications

- Basestation Applications
- Cellular and PCS Systems
- CDMA, W-CDMA Systems
- GSM/EDGE Systems
- Final PA for Low-Power Applications



Functional Block Diagram

## Product Description

The RF3220 is a high-efficiency GaAs Heterojunction Bipolar Transistor (HBT) amplifier packaged in a low-cost surface-mount package. This amplifier is ideal for use in applications requiring high-linearity and low noise figure over the 500MHz to 3GHz frequency range. The RF3220 operates from a single 5V power supply, and is assembled in an economical 3mmx3mm QFN package.

## Ordering Information

RF3220                    High Linearity/Driver Amplifier  
RF3220PCBA-41X        Fully Assembled Evaluation Board

## Optimum Technology Matching® Applied

<input checked="" type="checkbox"/> GaAs HBT	<input type="checkbox"/> SiGe BiCMOS	<input type="checkbox"/> GaAs pHEMT	<input type="checkbox"/> GaN HEMT
<input type="checkbox"/> GaAs MESFET	<input type="checkbox"/> Si BiCMOS	<input type="checkbox"/> Si CMOS	
<input type="checkbox"/> InGaP HBT	<input type="checkbox"/> SiGe HBT	<input type="checkbox"/> Si BJT	

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## Absolute Maximum Ratings

Parameter	Rating	Unit
RF Input Power	+20	dBm
Device Voltage	-0.5 to +6.0	V
Device Current	250	mA
Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



Caution! ESD sensitive device.

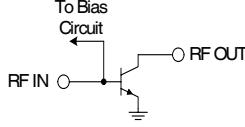
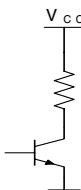
Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

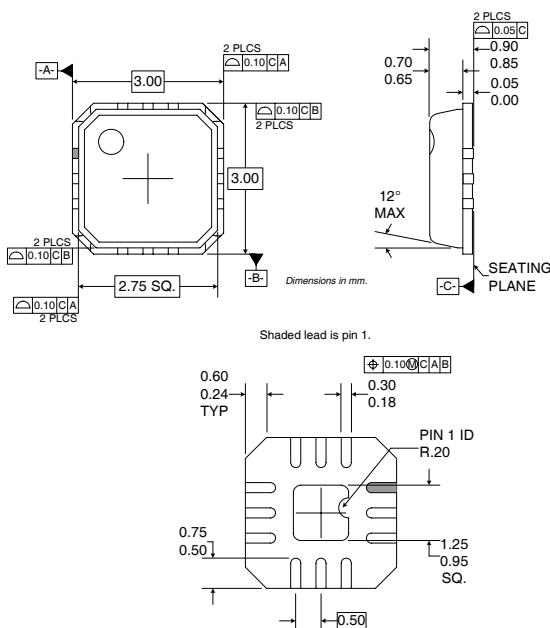
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					$V_{CC}=5V$ , $RF_{IN}=-10\text{ dBm}$ , $\text{Freq}=1850\text{ MHz}$ , with $\text{Temp}=25^\circ\text{C}$ unless otherwise noted.
<b>AC Specifications</b>					
Frequency	500		2000	MHz	
Gain	12	14.2	15.5	dB	
Input VSWR		1.2	1.5	SWR	
Output VSWR		1.7	2.0	SWR	
Reverse Isolation	20	23			
Output IP3	36	40		dBm	$F_1=1850\text{ MHz}$ , $F_2=1851\text{ MHz}$
Output P1dB	23	+25.5		dBm	
Noise Figure		2.9	3.3	dB	
<b>Thermal</b>					
Theta <sub>JC</sub>		76		°C/W	
Maximum Measured Junction Temperature at DC Bias Conditions		153		°C	$T_{CASE}=+85^\circ\text{C}$
Mean Time To Failures		5800		years	$T_{CASE}=+85^\circ\text{C}$
<b>DC Specifications</b>					
Device Voltage	4.5	5.0	5.5	V	$I_{CC}=160\text{ mA}$
Operating Current Range	110	145	170	mA	$V_{CC}=5V$

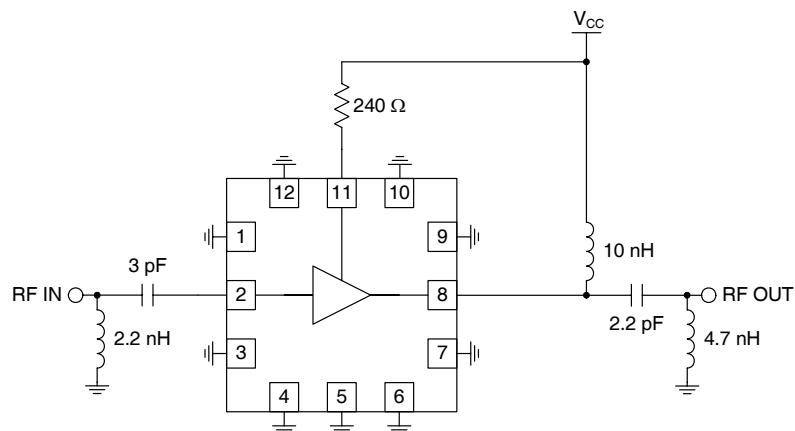
Note: The RF3220 must be operated at or below 175mA in order to achieve the thermal performance listed above. While the RF3220 may be operated at higher bias currents, 175mA is the recommended bias to ensure the highest possible reliability and electrical performance.

Pin	Function	Description	Interface Schematic
<b>1</b>	<b>GND</b>	Ground connection.	
<b>2</b>	<b>RF IN</b>	RF input pin. This pin is not internally DC-blocked. A DC blocking capacitor suitable for the frequency of operation should be used.	
<b>3</b>	<b>GND</b>	Ground connection.	
<b>4</b>	<b>GND</b>	Ground connection.	
<b>5</b>	<b>GND</b>	Ground connection.	
<b>6</b>	<b>GND</b>	Ground connection.	
<b>7</b>	<b>GND</b>	Ground connection.	
<b>8</b>	<b>RF OUT</b>	Amplifier output pin. This pin is an open-collector output. It must be biased to $V_{CC}$ through a choke or matching inductor. This pin is typically matched to $50\Omega$ with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	See pin 2.
<b>9</b>	<b>GND</b>	Ground connection.	
<b>10</b>	<b>GND</b>	Ground connection.	
<b>11</b>	<b>BIAS</b>	This pin is used to control the bias current. An external resistor may be used to set the bias current for any $V_{PD}$ voltage. Allows for trade-offs between IP3 versus noise figure and $T_{MAX}$ .	
<b>12</b>	<b>GND</b>	Ground connection.	
<b>Pkg Base</b>	<b>GND</b>	Ground connection. Vias to ground required under the package base.	

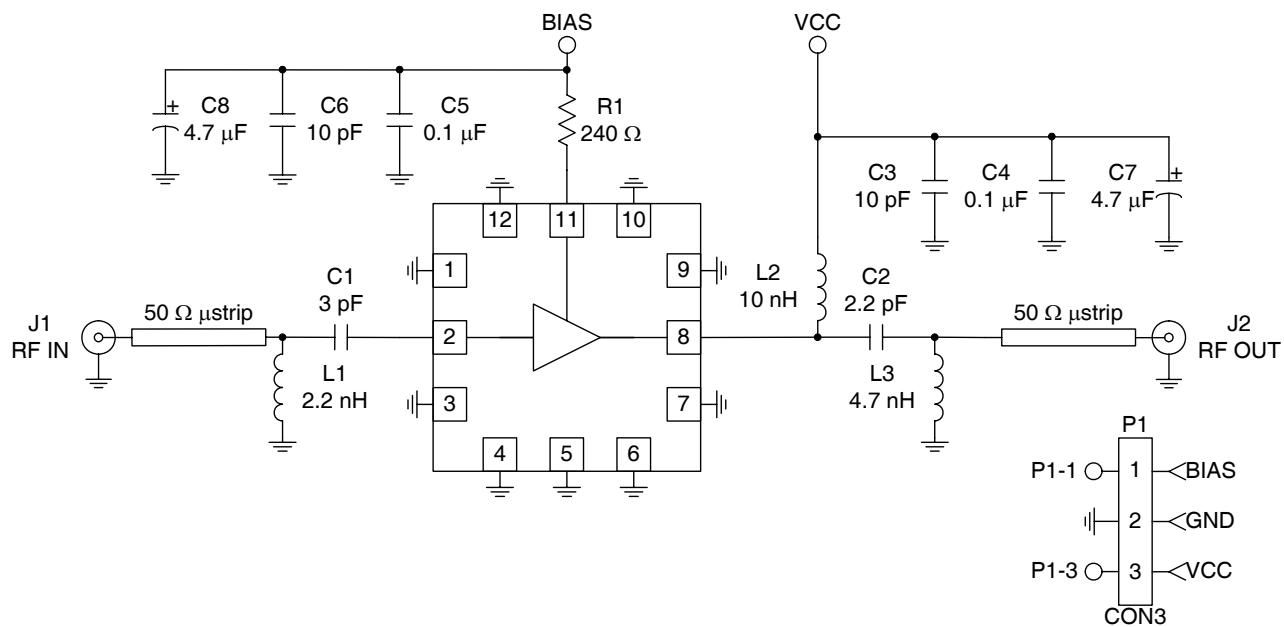
### Package Drawing



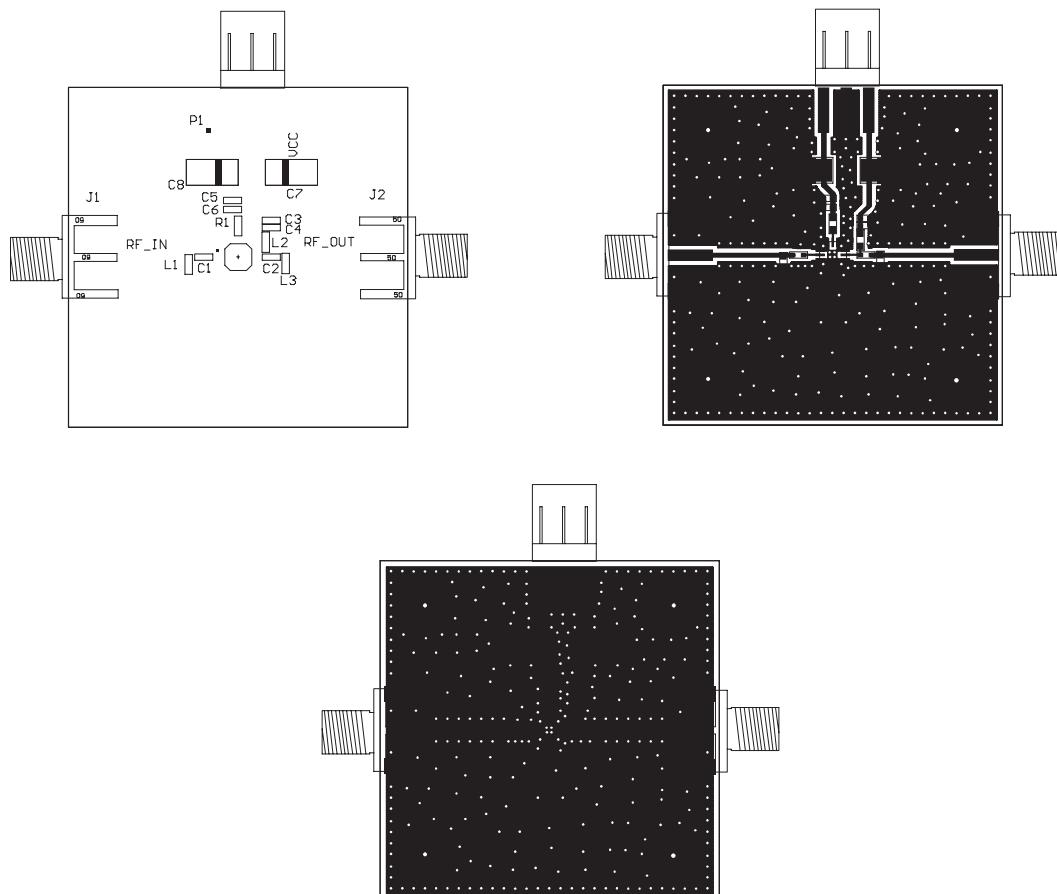
## Application Schematic - 1850 MHz

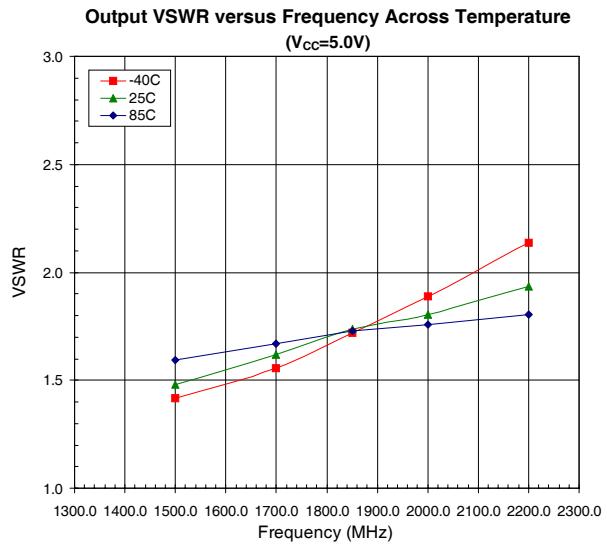
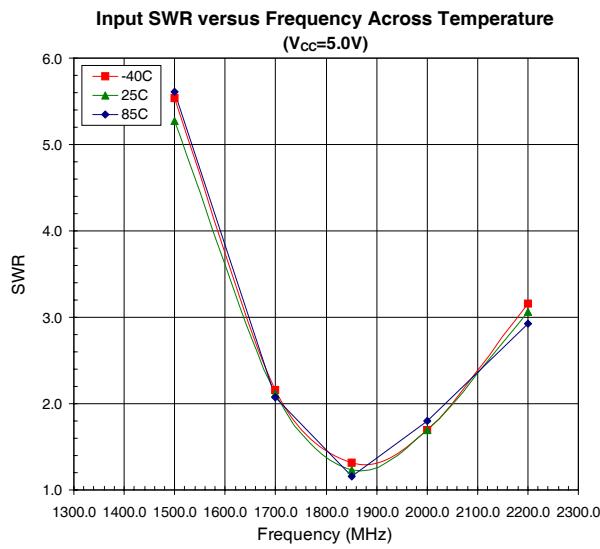
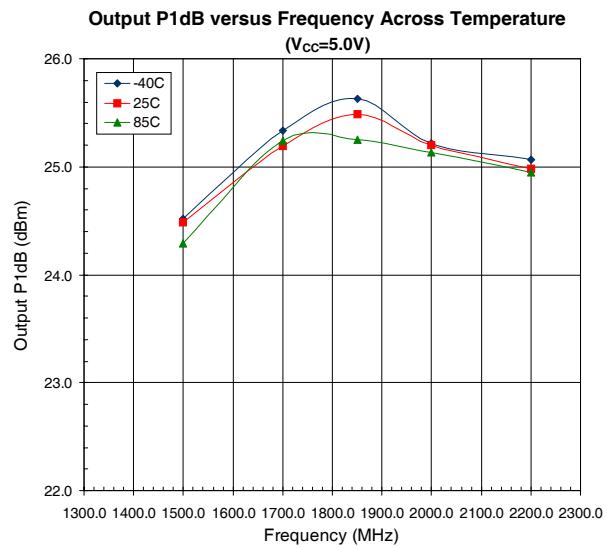
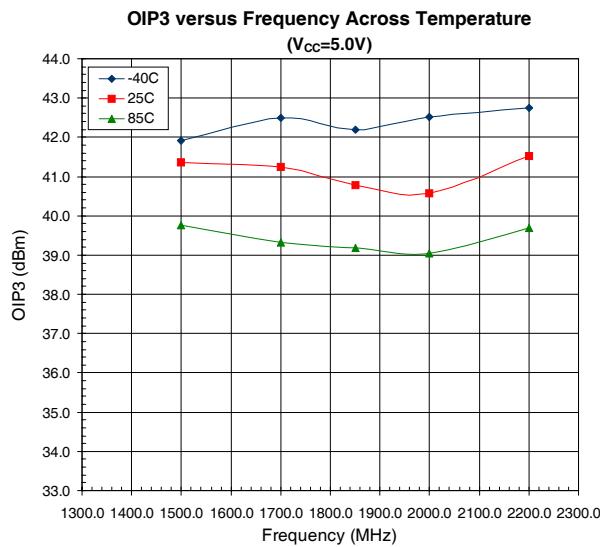
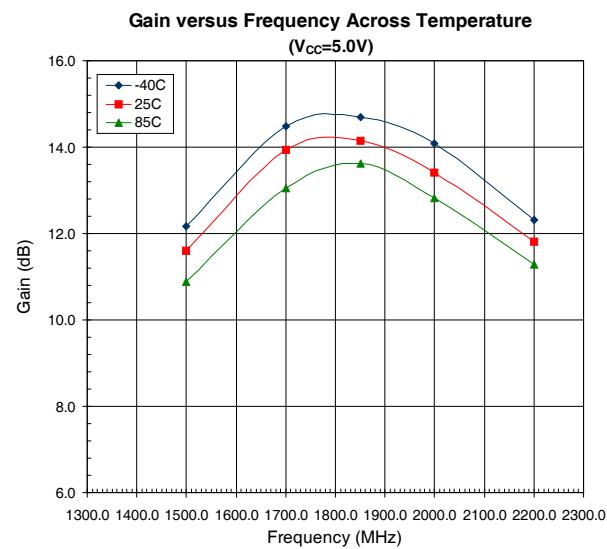
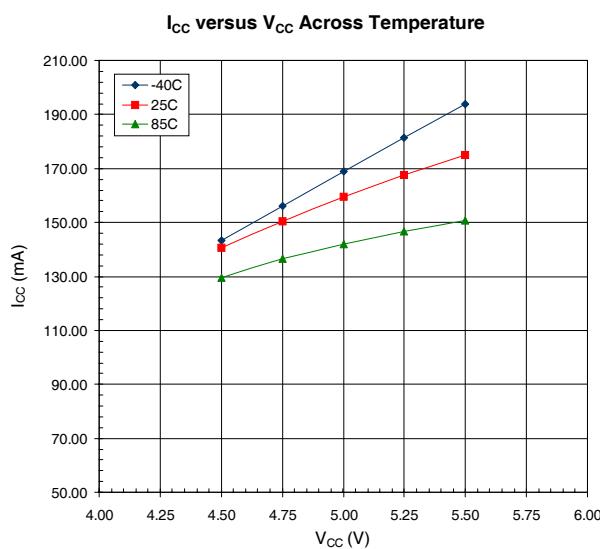


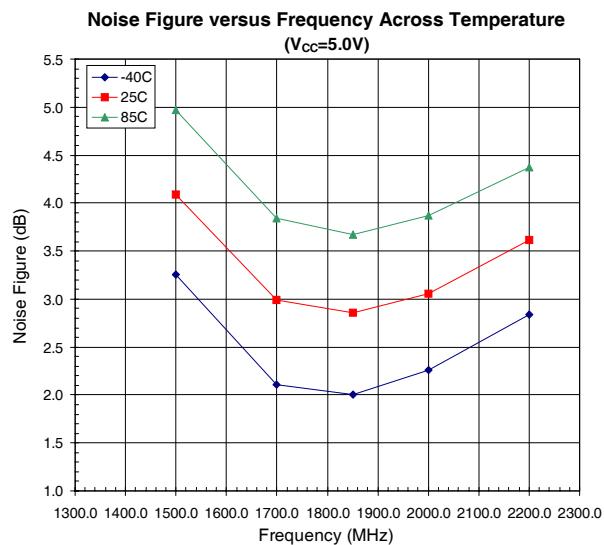
## Evaluation Board Schematic



**Evaluation Board Layout**  
**Board Size 1.5" x 1.5"**  
**Board Thickness 0.032", Board Material FR-4**







## PCB Design Requirements

## PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3  $\mu$ inch to 8  $\mu$ inch gold over 180  $\mu$ inch nickel.

## PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

## PCB Metal Land Pattern

$$A = 0.90 \times 0.28 \text{ (mm) Typ.}$$

$$B = 0.28 \times 0.90 \text{ (mm) Typ.}$$

$$C = 1.10 \text{ (mm) Sq.}$$

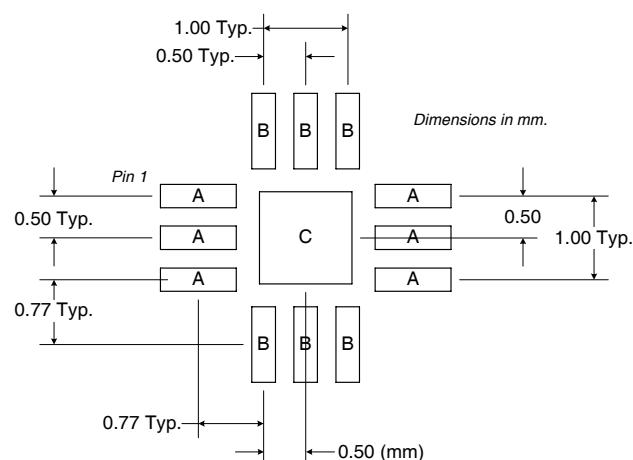


Figure 1. PCB Metal Land Pattern (Top View)

## PCB Solder Mask Pattern

PCB Solder Mask Pattern  
Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

## Thermal Pad and Via Design

The PCB metal land pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

Dimensions in mm.

Top View:

- Horizontal distance between outer edges of two 'A' blocks: 1.00 Typ.
- Vertical distance between top of 'A' blocks and bottom of 'B' blocks: 0.50 Typ.
- Width of each 'B' block: 0.50
- Width of each 'A' block: 0.50
- Height of each 'A' block: 0.77 Typ.
- Height of each 'B' block: 0.77 Typ.
- Height of block 'C': 1.00 (mm) Sq.

Side View:

- Width of block 'C': 1.00 Typ.
- Width of each 'A' block: 0.50
- Width of each 'B' block: 0.50
- Height of each 'A' block: 0.77 Typ.
- Height of each 'B' block: 0.77 Typ.
- Vertical distance between top of 'A' blocks and bottom of 'B' blocks: 0.50

**Figure 2. PCB Solder Mask Pattern (Top View)**